

A500
Chassis Mount Controller
Standard Equipment

User Manual
A91M.12-279330.21-1191

Translation of the German Description
A91M.12-234802

Notes

Application Note



Caution The relevant regulations must be observed for control applications involving safety requirements.

For reasons of safety and to ensure compliance with documented system data, repairs to components should be performed only by the manufacturer.

Training

AEG offers suitable training that provides further information concerning the system (see addresses).

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Terminology



Note This symbol emphasizes very important facts.



Caution This symbol refers to frequently appearing error sources.



Warning This symbol points to sources of danger that may cause financial and health damages or may have other aggravating consequences.



Expert This symbol is used when a more detailed information is given, which is intended exclusively for experts (special training required). Skipping this information does not interfere with understanding the publication and does not restrict standard application of the product.



Path This symbol identifies the use of paths in software menus.

Figures are given in the spelling corresponding to international practice and approved by SI (Système International d' Unités).
I.e. a space between the thousands and the usage of a decimal point (e.g.: 12 345.67).

Objectives

This publication is the basic publication for the A500. It describes the scope of performance of the programmable controller and supplies the user with all the information which he requires in order to build it up so that he can start it for standard applications and begin with the programming. The following is described:

- ☐ Conciguration (combination of process, operating and programming peripherals)
- ☐ Hardware structure
- ☐ Port of the power supply
- ☐ Port of the cable leading to the process
- ☐ Procedure for the initial start-up

Cross references to the publications which involve special applications (e.g., system communication, process visualization, programming, ...) are also given at suitable places.

Arrangement of This Guide

Chapter 1 General

This chapter lights on the integration of the Modicon A500 programmable controller in its programming, operating, networking and I/O peripherals. The emphasis lies on the question, “What is possible with the A500 and where do its performance limits lie?” Concrete instructions for action are not given at this point; chapter 3 is concerned with these in a thorough way.

The following points are treated in detail:

- ❑ Structure (configuration limits, applicable hardware modules)
- ❑ Networking possibilities with other programmable controllers
- ❑ Connectable printers, programming and operating devices
- ❑ Survey of the available software

Chapter 2 Operating and Indicating Elements

This chapter is only concerned with the topics which are relevant for the operator of an A500 running in the process, divided according to operating and indicating elements as well as simple maintenance works. It shows the possibilities concerning the structure of an operator interface and supplies catch points which are significant for the compilation of system-/application-specific operating instructions and maintenance schedules for the Modicon A500.

Chapter 3 Configuration and System Start-Up

This chapter contains detailed configuration guides, hardware settings and installation guidelines with notes for the system start-up.

Chapter 4 Characteristic Data

All the specifications of the A500 are summarized in this chapter according to the VDI guideline 2880, page 1.

Chapter 5 Earthing and EMC Measures

This chapter imparts basic knowledge for earthing and EMC measures.

Appendix A Programming in Dolog B

This chapter dealt with the generation and entry of Dolog B programs. It deals with the following topics with special emphasis:

- ❑ Program structure and program generation
- ❑ Program entry
- ❑ Operating time calculation

Appendix B Module Descriptions

The descriptions of those modules which are used in the controller of the A500 can be found in the appendix. The module descriptions of the I/O modules are summarized in the user manual of the I/O peripherals with front connection.

Related Documents

AEG offers a family of open-loop controllers which increase in the performance level and are compatible in hardware and software over a wide range with the chassis mount controllers A130, A350 and A500. These facts are taken into account in the documentation concept shown on the next page. The concept is divided into the four following main areas.

Programmable Controllers

One user manual is provided for each controller of the individual programmable controllers. The user finds all the necessary information in this publication in order to prepare the programmable controller so that he can start it up and begin the programming.

Process Peripherals

Concrete information concerning the structure of the process peripherals are given in a total of three publications (linking the I/O subracks to the controller, linking the I/O subracks to each other, etc.). The description of those modules which are used to build up the I/O peripherals (I/O modules, secondary subracks, power supplies, cables, ...) are also summarized in the appendix.

Firmware

The software integrated in the central processing unit is documented in these publications.

Software for Programming Panels

The program packages which can be run on PCs and are obtainable as an option for the programming and as a start-up aid of the PLC are described here. The relevant software kits are sold as 3 1/2" and 5 1/4" diskettes.

Automation device (central part)	A130 Modular Automation Device A91V.12-234 585		A350 Modular Automation Device A91V.12-234 678		A500 Modular Automation Device A91M.12-279 330	
	DEA-H1, DEA-K1 Decentralized Extension Assembly for A030, A130 / A350 / A500 A91V.12-234 820		Process Peripherals Front Connection Technology for A130 / A350 / A500 A91V.12-271 613		Process Peripherals Rear Connection Technology for A350 / A500 A91V.12-	
Software incorporated in devices	Programming Dolog A for A030 / A130 A91V.12-		Operating Functions Bsdol B2 for A350 / A500 A91V.12-234 730			
	Dolog B Basic Module for A350 / A500 A91V.12-234 731	Mass Flow, Sequence Control System for A350 / A500 A91V.12-234 561	MMI Module and Function for A350 / A500 (TESY) A91V.12-232 026	Device Couplings for A350 / A500 A91V.12-232 028	Dolog B Regulations for A350 / A500 A91V.12-232 260	
Programming device software	Dolog AKF for A030 / A130 E-Nr. 424-247 139	Dolog AKF for A350 / A500 E-Nr. 424-	Dolog B for A350 / A500 E-Nr. 424-	SW - Archiving for A350/A500 Systems (Archives) E-Nr. 424-	EDITOR for A350 / A500 Systems E-Nr. 424-	
	MMI Editor for A350 / A500 (TESY) E-Nr. 424-	Designed Device Coupling for KOS 130 COM E-Nr. 424-	Designed Device Coupling for A350 / A500 COM E-Nr. 424-	Initial Operation Assistance for A350 / A500 SETUP LOOP CTRL. E-Nr. 424-	INSTAL for Programming Unit E-Nr. 424-	

The following publication is not yet finished:

Process Peripherals
Rear Connection Technology
for A350 / A500

You only can obtain the German Edition with the No. A91M.12-234 780 or you must order the predecessor:

Systemdescription
A500
Part 1-19
A91V.12-232 021

Table of Contents

Chapter 1	General	1
1.1	Introduction	2
1.2	Compatibility	2
1.3	General Mode of Operation	3
1.3.1	Memory	3
1.3.2	Central Processing Unit	4
1.3.3	I/O Modules	4
1.3.4	Busses	5
1.4	Structure	6
1.4.1	Standard Equipment for the Controller	6
1.4.1.1	STA 501, STA 551	7
1.4.1.2	STA 503, STA 553	7
1.4.1.3	STA 557	7
1.4.1.4	STA 505, STA 555	7
1.4.2	Structure of the I/O Peripherals	8
1.4.3	Configuration Limits	10
1.5	Recommended Peripherals	11
1.5.1	Usable Programming Panels	11
1.5.2	Usable Printers	11
1.5.3	Devices to Program EPROMs	11
1.6	Programming	12
1.6.1	Program Generation	12
1.6.2	Programming Panels	12
1.6.3	Special Programming Languages	13
1.6.4	Principle Structure of a Dolog AKF Program	14
1.6.5	Principle Structure of a Dolog B Program	15
1.7	Networking	16
1.7.1	Overview	16
1.7.2	Modnet 1/SFB Communication	17
1.7.3	Modnet 1/N Communication	18
1.7.4	Modnet 1/F Communication	18
1.7.5	Modnet 2/NP Communication	19
1.8	Tesy	19
1.9	Survey of the Usable Software Packages	20
1.10	Module Survey	21

Chapter 2 Operating 25

2.1	Indicating Elements	26
2.2	Switches, Contact Sockets, Push Buttons	28
2.2.1	Switches	28
2.2.2	Contact Sockets	28
2.2.3	Push Buttons	28
2.3	Changing the Rechargeable Battery (Maintenance)	29
2.4	Setting Up an Operator Interface	30
2.5	Switching the Supply Voltage On and Off	31
2.5.1	The System is Switched On and Off by the User	31
2.5.2	The System is Switched On and Off by a Powerfail	31
2.5.3	Check Measures (Inspection)	31

Chapter 3 Configuration 33

3.1	Configuration of the Hardware	34
3.1.1	Structure of the Controller	34
3.1.1.1	Structure of the Controller with the STA 501 / STA 551	35
3.1.1.2	Structure of the Controller with the STA 503 / STA 553	36
3.1.1.3	Structure of the Controller with the STA 505 / STA 555	37
3.1.1.4	Structure of the Controller with the STA 557	38
3.1.2	Structure of the I/O Peripherals	39
3.1.2.1	Structure of the I/O Peripheral with Front Connection	39
3.1.2.2	Structure of the I/O Peripherals with Rear Connection	42
3.1.2.3	Mixed Structure	45
3.1.3	Configuration Limits (Maximum Expansion)	46
3.1.4	Specifying the I/O Equipment	48
3.1.5	Specifying the Slot References	48
3.1.5.1	Specifying the Slot References with Front Connection	48
3.1.5.2	Specifying the Slot References with Rear Connection	49
3.1.5.3	Example for a Mixed Structure (Front and Rear Connection)	51
3.1.6	Assignment of the Signal Addresses to the Signals (Addressing)	52
3.1.6.1	Addressing According to DIN	52
3.1.6.2	AEG Addressing	54
3.1.6.3	Symbolic Addressing	55
3.2	Structure of the Power Supplies	56
3.2.1	Supplying the Supply and Working Voltages for I/O Modules with Rear Connection .	58
3.2.2	Port Diagram of the UB Supply (24 VDC for Modules and Sensors) with I/O Modules with Front Connection	58
3.2.3	Port Figure of the Working Voltage Supply (US = 24 VDC / L = 230 VAC) for I/O Modules with Front Connection	65
3.3	Switching Off Mode of the Binary Outputs with Malfunctions on the Power Supply ..	70
3.3.1	Switching Off Mode for Modules with Rear Connection	70
3.3.2	Switching Off Mode for Modules with Front Connection	71
3.4	Synchronization of the Power Supplies	72
3.5	PEAB Monitoring	72
3.6	Start-Up Characteristics	74
3.6.1	Start-Up Characteristics when Using the ALU 011	74
3.6.2	Start-Up Characteristics when Using the ALU 061	74
3.6.3	Start-Up Characteristics when Using the ALU 150	75

3.7	Installation	76
3.7.1	Settings for Modules	76
3.7.2	Mounting and Equipping the Subracks	79
3.7.3	Discharge Measures	80
3.7.3.1	Discharge Measures for Analogue Shielded Cables	80
3.7.3.2	Discharge Measure for the Modnet 1/SFB	81
3.7.3.3	Improving the EMC Immunity for the Modules	83
3.7.3.4	Overvoltage Protection for SFB Lines: Outside Buildings	84
3.7.4	Connecting Peripherals	86
3.8	Addressing the Memory	88
3.8.1	Address Capacity	88
3.8.2	Dividing the Memory into Segments, Memory Areas	89
3.8.3	Occupation of the Segments when Using ALU 150	90
3.8.4	Occupation of the Segments when Using the ALU 011 or ALU 061	90
3.8.5	Segments 1 and 2, Signal Memory	91
3.8.6	Special Marker Area	92
3.8.7	Special Word, Double Word and Floating Point Word Area	93
3.9	Check List for the Initial Start-Up and Test	95
3.9.1	Settings, Ports, Equipment	95
3.9.2	Information About the Initial State Disable (G Plug-In Jumper on the UKA)	96
3.9.3	Initial Start-Up	97
3.10	Further Information	98
3.10.1	Information to Enter the Equipment in the Equipment List	98
3.10.2	PEAB Time Error	99
3.10.3	Watchdog Display - Signal Relay - Marker 60	100
3.10.4	Setting the Transmission Rate with the Software	100
3.11	Documentation and Archiving	101
3.11.1	Documentation of the Hardware Settings	101
3.11.2	Documentation of the User Program with Additional Information	104
3.11.3	Program Archiving	104

Chapter 4 Specifications 105

4.1	User Program	106
4.2	Interfaces	107
4.2.1	Supply Interface	107
4.2.2	Process Interfaces	107
4.2.2.1	Configuration Limits	107
4.2.2.2	Inputs	108
4.2.2.3	Outputs	109
4.2.3	Data Interface	110
4.2.3.1	RS 232 C (V.24) Programming Interface	110
4.2.3.2	Communications Port (RS 232 C / Current Loop / Telecontrol Mode)	110
4.2.3.3	RS 485 Communications Port (Modnet 1/SFB)	111
4.2.3.4	PMB (Parallel Microprocessor Bus)	111
4.2.3.5	PEAB (Parallel I/O Bus)	111
4.2.3.6	PAB 1 (Parallel System Bus)	111
4.2.3.7	PLB (Parallel Local Bus)	112
4.3	Processor	112
4.4	Processing Times	113
4.5	Memories	113
4.5.1	Signal and System Memory	113
4.5.2	Memory for the Basic Software	113
4.5.3	Memory for the User Program	113
4.5.4	Backup Rechargeable Battery	114

4.6	Physical Characteristics	114
4.6.1	Design Data	114
4.6.2	Permitted Line Lengths	115
4.6.3	Connection Mode	115
4.7	Environmental Data	116
4.7.1	Climatic (According to DIN 40 040, Page 1/6.70)	116
4.7.2	Mechanical (Shocks and Vibrations)	116
4.7.3	Electrical	117

Chapter 5 Earthing and EMC-Measures 119

5.1	Earth Grounding and Earthing (Installation Guidelines)	120
5.1.1	Earth Grounding All Inactive Metal Parts	120
5.1.2	Protective Earthing According to VDE 0100	120
5.1.3	Functional Earthing	121
5.1.4	Reference Conductor System	121
5.1.5	Earthing System Measures for the Cabinet Structure	123
5.2	EMC Measures	124
5.2.1	Measures for the Installation and Wiring	124
5.2.1.1	Within a Cabinet	124
5.2.1.2	Outside Cabinets in Closed Buildings	126
5.2.1.3	Outside Buildings	126
5.2.2	Measures for the Power Supply	127
5.2.3	Measures Against Direct Noise Interference	127
5.2.4	Measures for the Sources of Interference	127
5.3	Interference Suppression	128
5.4	Technique of Peripheral Ports	128
5.4.1	Protective Circuits for Actuators	128
5.4.2	Wiring the Reference Conductor in an Isolated Structure	129
5.5	Protective Logic and Safety Interlocks	130

Appendix A Programming in Dolog B 131

A.1	Construction of a Dolog B Program (VList Wiring/Connection List)	132
A.1.1	Construction of a Linear VList	132
A.1.2	Structure of a VList With Jumps	133
A.1.2.1	A Part of the VList is Skipped Depending on a Condition	133
A.1.2.2	A Part of the VList is Run Depending on a Condition	134
A.1.3	Construction of a VList with Subroutines	135
A.1.4	Interrupt VList	136
A.2	Program Input	137
A.3	Measures to Take when the Program Crashes	138
A.4	List of Bsdol Functions (in order of their logical use)	139
A.4.1	Online Parameters	139
A.4.2	Online Programming	140
A.4.3	Online Testing	141
A.4.4	Online Documenting	141
A.5	List of the Bsdol Functions (sorted topicwise)	143
A.6	List of Dolog B Blocks	145

A.7	Cycle Time	151
A.7.1	Structure of the Program Cycle	151
A.7.2	Delay Time of the END Block (or Program End in Dolog AKF)	152
A.7.3	Delay Time of Direct Binary and Analogue I/O on the Modnet 1/SFB	153
A.7.4	Processing of the END block for Dolog B or of the program end for Dolog AKF ...	154
A.7.5	Notes on the Regulating Delay Time System	155
A.7.6	Delay Times of the Dolog B Blocks (for ALU 150)	156

Appendix B Module Descriptions 165

ALU 011, ALU 012, ALU 021 Central Processing Unit	167
ALU 061, ALU 071 Central Processing Unit	155
ALU 150 Central Processing Unit	177
BATT 3.6 - 1.8 Ah Rechargeable Battery	221
BIK 151 Modnet 1/SFB Interface for Central Processing Units	225
COP 82Coproprocessor	235
DKV 023 PEAB Network	243
DNO 028 24 VDC Power Supply	249
DNP 023 220 VAC Power Supply	257
DNP 023-1, DNP 023-2 Power Supply	265
DNP 023-3, DNP 023-4 Power Supply	275
DNP 028 220 VAC Power Supply	285
DTA 024 Subrack	293
DTA 27.1 Subrack	301
DTA 028 Subrack	313
DTA 101 Subrack	323
DTA 107 Subrack	333
KOS 152 Modnet 1N Interface	347
KOS 882 Communication Processor	361
LLB Air Guide	369
MAT 827 Arithmetic Processor	373
SAE 2 Cabinet Connection Unit	379
SC 8128 / SC 8256 Memory Module (RAM)	385
SF 8512 Memory Module (EPROM)	391
UKA 024 Monitoring Module	397
UVL 841, UVL 842 Interface Converter	413

Chapter 1

General

This chapter lights on the integration of the Modicon A500 programmable controller in its programming, operating, networking and I/O peripherals. The emphasis lies on the question, “What is possible with the A500” and where do its performance limit lie?”. Concrete instructions for action are not given at this point; chapter 3 is concerned with these in a thorough way.

- The following points are treated in detail:
- Structure (configuration limits, applicable hardware modules)
- Obtainable standard versions
- Networking possibilities with other programmable controllers
- Connectable printers, programming and operating devices
- Survey of the available software

1.1 Introduction

Modicon A500 is a chassis mount controller for medium to larger automation tasks. It allows the following automation functions depending on the configuration degree:

- ☐ Control
- ☐ Closed-loop control
- ☐ Computing
- ☐ Processing the measured values
- ☐ Signalling, monitoring
- ☐ Log
- ☐ Visual display (Viewstar 200 / Viewstar B500)
- ☐ Text dialogue (Tesy)
- ☐ Communication

Modicon A500 is mounted in subracks which are designed for applications with poor ambient conditions (rigid structure). Slots are prepared on them in which the individual modules are inserted via guide rails. The chassis earth is connected and the modules are connected to the bus system of the A500 automatically here.

Subracks with a breadth of $1\frac{1}{2}$ 19" and 19" are available. The installed height of all the subracks amounts to 6 height units for all of them whereby 1 height unit is 44.45 mm high.

The A500 can have a front connection or a rear connection. All the ports are on the front of the modules for the front connection. This allows the subracks to be mounted on a wall as well as in 19" holders. The ports are on the rear of the subracks for the rear connection. The subracks are then to be fixed in 19" holders.

The subracks with front connection include front covers which can be swung to both sides and removed completely and which allow a view of the LED indicators of the modules and can be individually fitted with insertable fill-in labels for the terminal assignment. The labelling is maintained when the modules are changed.

1.2 Compatibility

Hardware

The intelligent function module ZAE 105 and VIP 101 can also be inserted in A250 and A350; I/O modules with front connection can also be inserted in A130, A250 and A350.

The prerequisite for uniform I/O peripherals from A130 to A500 was thus fulfilled. The user now has the possibility to retrofit his machine from A130 via A250 and A350 to A500 by changing the controllers without having to change the I/O peripherals.

Software

The performance of the basic software integrated in Modicon A350 is upwards compatible with Modicon A500. The software for programming panels which can be obtained as an option is identical for both programmable controllers.

1.3 General Mode of Operation

The mode of operation of the A500 (cf. Figure 1) is greatly determined by the combination of:

- ❑ Memory
- ❑ Central processing unit
- ❑ I/O modules

The flow of information between these components is safeguarded by busses.

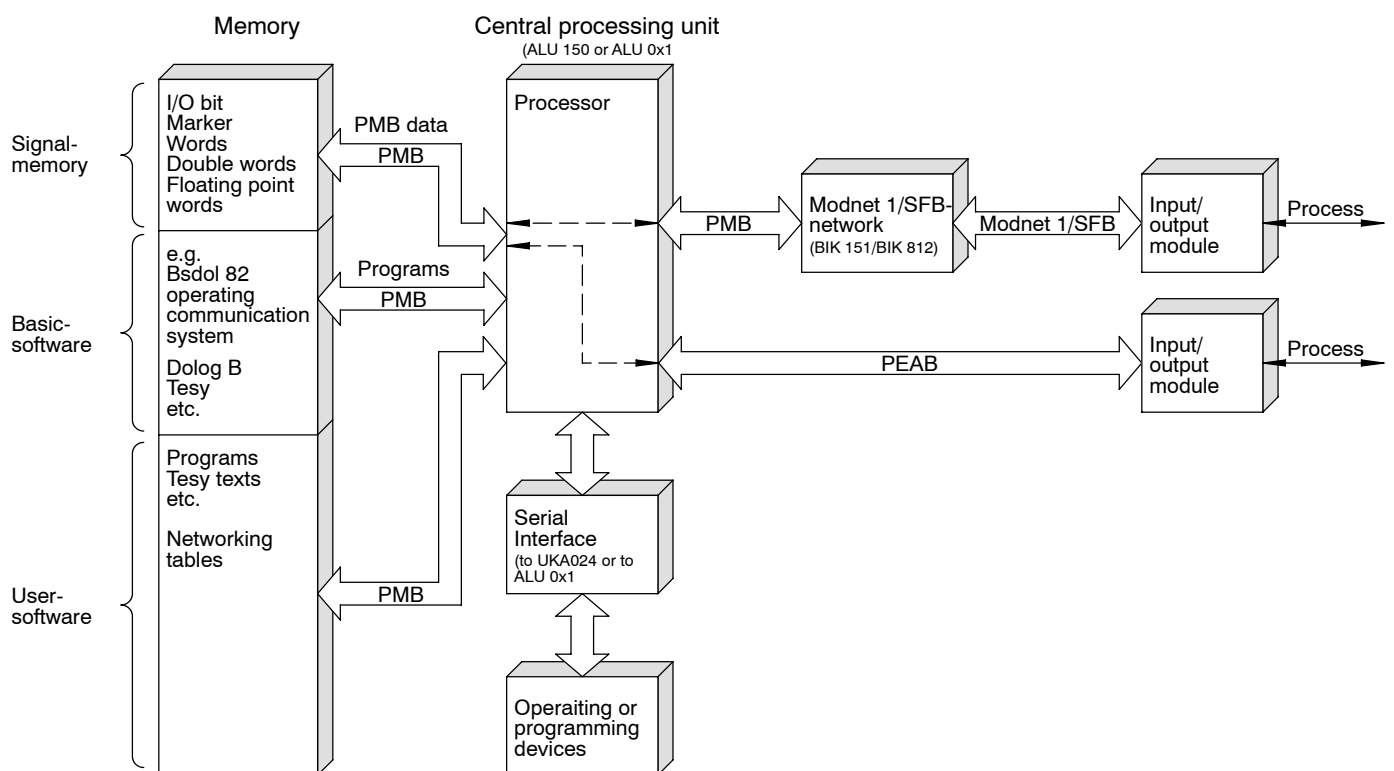


Figure 1 Mode of Operation of the A500 (Diagrammatic Representation)

1.3.1 Memory

The memory has an address space of 1 mbyte. A distinction is made here between 3 areas:

- ❑ User memory (RAM or EPROM)
- ❑ Signal memory (RAM)
- ❑ Basic software (EPROM)

The user memory makes available the memory space for the user program, for special functions and for the system RAM. The user program can be saved on EPROM or on RAM selectively.

The central processing unit itself is the carrier modules for the user memory when the ALU 0x1 is used. Separate memory modules (SF 8512 (EPROM) or SC 8128 or SC 8256 (RAM)) are necessary when the ALU 150 is used.

The process image (I/O bits, markers, words, double words and floating point words) are saved in the signal memory. User programs always work with the data from the signal memory and not with the input and output signals themselves.

The basic software is located on EPROMs in the central processing unit. It includes all the programs necessary for the programming and operation. This includes the Bsdol operating communication system and the Dolog programming language, for example (in the Dolog B programming type, i.e., log programming).

1.3.2 Central Processing Unit

The central processing unit is the processor of the A500. It controls the functions of the entire system and executes the individual instructions of a program in accordance with the rules pre-given by the basic software. It organizes the reading in of external data and signals into the signal memory, processes these data and performs design calculations, continually deposits processing results in the signal memory and realizes the output of the results.

User programs are always processed cyclically in the A500. The valences of the input signals are read into the signal memory once at the end of each program cycle and the valencies of the output signals output from the signal memory to the peripherals. The user program always works with the data from the signal memory, i.e., with the process images, only during the remainder of the program cycle.

This can be changed with the hardware module SES 2 (rear connection), for example. A spontaneous entry, i.e., roughly free if delay, of preferably time-critical process signals can be forced with it using interrupt. Another possibility for a delay-free input/output is supplied by the software blocks of "AUS", "EIN", "BAUS" and "BEIN".

1.3.3 I/O Modules

All modules which have a direct effect on the process are I/O modules. This includes the following:

- Input/output modules for processing binary signal statuses
- Input/output modules for processing analogue signals
- Intelligent modules (partly autonomous I/O modules with an integrated processor, e.g., back-up controller, positioning device, counter modules, etc.)

A distinction is to be made for the I/O modules:

- Modules with front connection:
The process signals and the supply of the sensors and actuators are connected via screw/plug-in terminals with front connections.
- Modules with rear connection:
The process signals and the supply of the sensors and actuators are connected via 48 pole connectors which are located on the rear of the module.

A summary of all the modules which can be used for A500 and therefore also all the I/O modules which can be used divided according to front and rear connection is given by section 1.10.

1.3.4 Busses

The modules communicate with the central processing unit (ALU) via busses. The modules contact the bus/busses automatically when the modules are engaged via connectors arranged on the rear of the module board.

The **PMB** is a parallel microprocessor bus (memory bus) which is located on the rear wall of the primary subrack. The central processing units (e.g., ALU 150), the memory modules (SC 8256, SF 8512), the monitoring module (UKA 024) and the interface modules (BIK, KOS, KP, ...) are connected to it. Each PMB node occupies a certain part of the available address space (memory). The definition of which addresses are assigned to the respective node is given on the individual modules by the hardware via jumper settings (no referencing). The jumper settings are to be taken from the individual module descriptions.

The **Modnet 1/SFB** is a serial data bus which creates the connection between the controller and the remote I/O peripherals. The modules with front connection (binary I/O, analogue I/O and intelligent modules) can be operated using it.

A fixed slot reference is assigned to each I/O slot via jumpers. The addressing is therefore independent of the module with which the respective slot is equipped (referencing).

This bus has another field of application as a link. It can be used here to construct a data path between two systems to be linked.

The **PEAB** is a parallel I/O bus which is located on the rear wall of the primary subrack and of the secondary subrack, DTA 025. PEAB nodes are UKA 024, ALU 011, ALU 061, ALU 150 and the I/O modules designed with rear connection and listed in table Table 8. The I/O slots for the PEAB are located in the secondary subracks, DTA 025 and in the primary subracks DTA 024 and DTA 028.

A fixed slot reference must be assigned to each PEAB slot. The addressing is therefore independent of the module with which the respective slot is equipped (referencing). The addresses for ALU and UKA are given automatically by the system.

1.4 Structure

The Modicon A500 consists of a **controller** and the **I/O peripherals**, i.e., one of a number of I/O modules depending on the task. It can be put together in a specific way for the relevant application due to its modular structure.

The following pages help to clarify the construction principle of the A500. Section 3.1 gives more detailed information.

The controller of an A500 consists of a primary subrack which can be equipped with modules which have the following functions:

- ❑ Power supply (DNP ...)
- ❑ Central processing unit (ALU 150, ALU 011 or ALU 061)
- ❑ Monitoring module UKA 024 (only required with ALU 150)
- ❑ Memory module (SF, SC, only required with ALU 150)
- ❑ PMB node such as BIK, KOS, KP1-..., ... (optional, depends on the task)

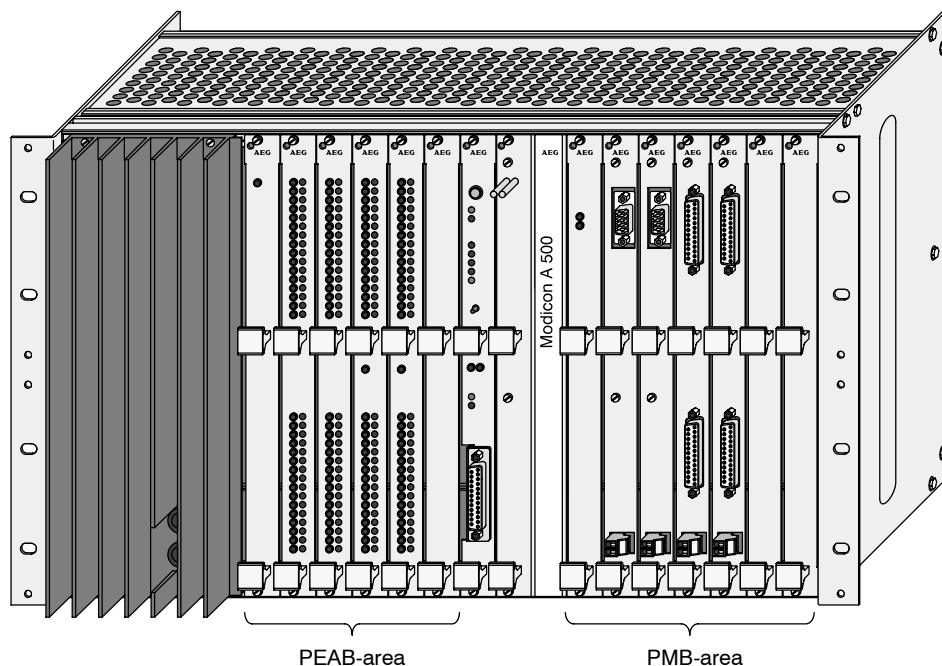


Figure 2 Modicon A500 with Rear Connection, Equipped with PMB and PEAB Nodes

1.4.1 Standard Equipment for the Controller

Partly equipped standard equipment which is to be expanded with memory modules and the I/O peripherals can be obtained for standard applications. They are ready for the connection, i.e., preset and inspected both module by module and as a complete unit.

The standard equipment can be supplied selectively with German or English basic software. Only the standard equipment with German basic software is described in this manual.

A selection can be made between the following pieces of standard equipment depending on the task. Features in common and differences are summarized in Table 1.

1.4.1.1 STA 501, STA 551

The standard equipment of STA 501 and STA 551 can be used for A500 systems which require many PMB slots. They differ from each other due to the primary voltage of the power supply (24 VDC for the STA 501, 230 VAC with the STA 551).

1.4.1.2 STA 503, STA 553

The standard equipment of STA 501 and STA 551 is meant for A500 systems which require a low number of PMB slots. They differ from each other due to the primary voltage of the power supply (24 VDC with the STA 503, 230 VAC with the STA 553). The STA 553 has 3 PEAB slots less than the STA 503 due to the wider power supply.

1.4.1.3 STA 557

The standard equipment of STA 557 can be used when B500 is to be employed. It consists of the DTA 27.1 subrack with an unplugged PMB in order to accept A500 and B500 modules. The position of the isolation point must be pre-given by the user when he orders the device. 12 PMB slots can be segmented in 5 to 12 connected P500 slots and correspondingly 0 to 7 A500 slots. The 13th PMB slot (on the right-hand side next to the ALU) should preferably be used for a memory module.

1.4.1.4 STA 505, STA 555

The standard equipment of STA 505 and STA 555 can be used when B500 is to be employed and differ from each other only due to the primary voltage of the power supply. They consist of the DTA 107 subrack with an unplugged PMB in order to accept A500 and B500 modules. The position of the isolating point must be given by the user when he orders the device. 11 PMB slots can be segmented in 5 to 11 connected B500 slots and correspondingly 0 to 6 A500 slots. The 12th PMB slot (on the right-hand side next to the ALU) should preferably be used for a memory module.

Table 1 Survey of the Standard Equipment

Standard Equipment	STA 501 / STA 551	STA 503 / STA 553	STA 557	STA 505 / STA 555
Connection mode	Rear connection	Rear connection	Rear connection	Front connection
Primary voltage	24 VDC / 230 VAC	24 VDC / 230 VAC	230 VAC	24 VDC / 230 VAC
not used PMB slots	7	3 / 3	13	12
not used PEAB slots	6	13 / 10	-	-
PEAB extension possible	yes	yes	yes	no
Subrack	DTA 024	DTA 028	DTA 27.1	DTA 107
equipped with				
Power supply	DNP 023-1 / DNP 023	DNO 028 / DNP 028	DNP 023	DNP 023-1 / DNP 023
Central processing unit	ALU 150	ALU 150	ALU 150	ALU 150
Monitoring module	UKA 024	UKA 024	UKA 024	UKA 024
Modnet 1/SFB network	optional	optional	optional	BIK 151

1.4.2 Structure of the I/O Peripherals

The I/O peripherals consist of a number dependent on the task of I/O modules which are collected in subracks and coupled to the controller via **PEAB** and/or **Modnet 1/SFB**. These modules process up to 32 process signals and thus form the interface to the process. A survey of all available modules is given in the tables in section 1.10. The connection of the I/O peripherals to the controller is described in section 3.1.2.

Linking the I/O Peripherals via Modnet 1/SFB

An expansion via **Modnet 1/SFB** (distributed expansion) consists of:

- DTA 102 or DTA 112 secondary subrack with max. 4 I/O modules with **front connection** and a DEA as a Modnet 1/SFB connection.
or
- DTA 103 or DTA 113 secondary subrack with max. 9 I/O modules with **front connection** and a DEA as the Modnet 1/SFB connection.
or
- 1 DEA-H1 or DEA-K1 compact device with an integrated Modnet 1/SFB connection and 24 inputs and 16 outputs in semiconductor type or in relay type.

Either DEA 106, DEA 116 or DEA 156 (known in the following as DEA 1x6) serve as the Modnet 1/SFB connection depending on the subrack and I/O equipment.

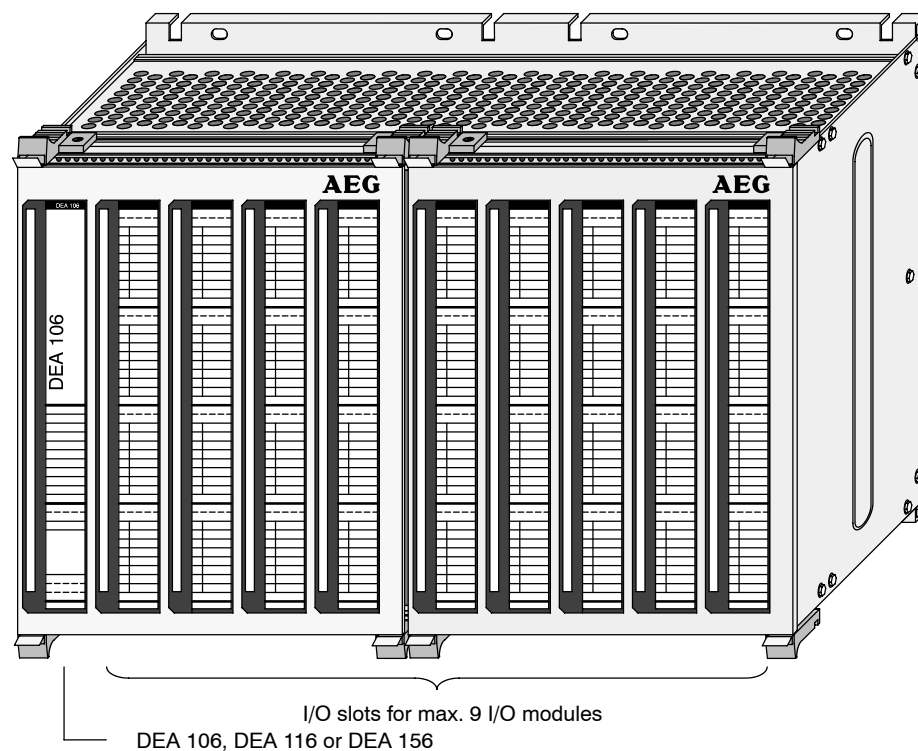


Figure 3 Secondary Subrack DTA 113



Warning The DEA 116 cannot be used in any subrack! Exact details about which DEA is suitable for which subrack can be found in table Table 16 on page 1.

Connecting the I/O Peripherals via PEAB

The I/O modules with rear connection are connected to the PEAB (cf. survey in table Table 8). Their construction width amounts to 4T or 8T.

An expansion via **PEAB** (primary expansion) exists of:

- DTA 025 secondary subrack with DNP 025 or DNP 026 power supply, DUV 025 connection printed board, PEAB connection of DKV 022 and max. 16 I/O modules with **rear connection**. DNP, DKV and DUV are not required in certain secondary sub-racks (cf. section 3.1.2.2 for details); their slots then remain unequipped.

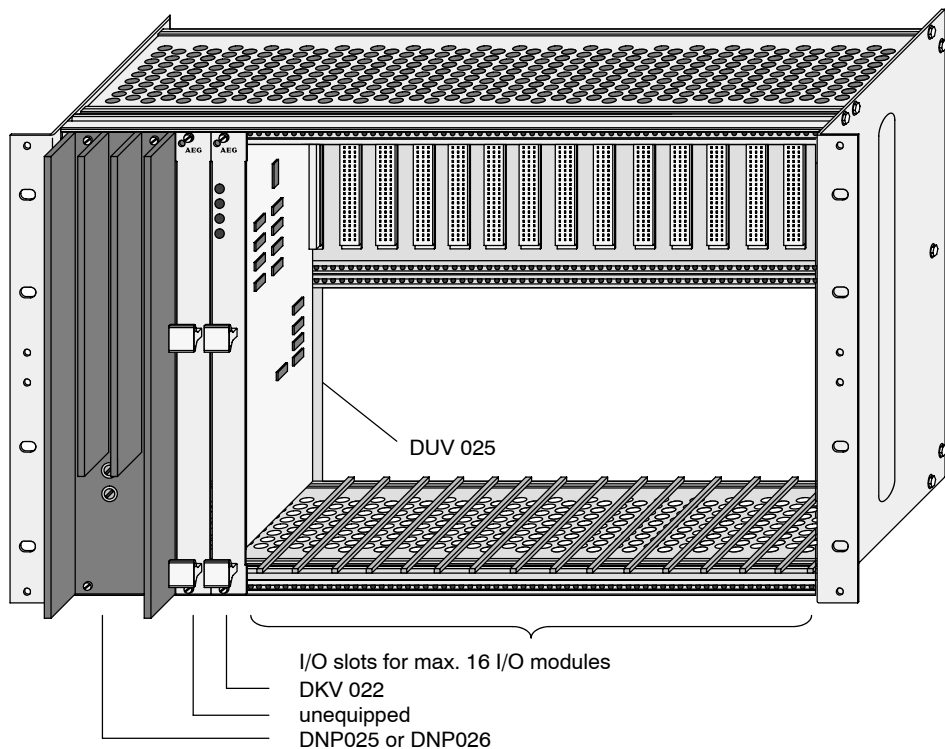


Figure 4 DTA 025 Secondary Subrack

The PEAB transmission paths can be monitored optionally for line fracture, connector or PEAB driver malfunctions. The DKU 022 is required for the hardware here.

The maximum expansion of the A500 via PEAB depends on the type of subrack of the controller and is given in section 1.4.3.

1.4.3 Configuration Limits

The following configuration limits are valid for the A500:

- distributed expansions (Modnet 1/SFB) for each programmable controller
 - BIK 151 / BIK 812 for I/O for each programmable controller 3
 - distributed expansions (DEA ...) for each BIK 151 / BIK 812 16
 - distributed expansions (Modnet 1/SFB) for each A500 48 = 3 x 16
- primary expansions (PEAB) for each A500 and programmable controller
 - Controller mounted with DTA 024 or DTA 028 9
 - Controller mounted with DTA 27.1 9
- Expansions (Modnet 1/SFB **and** PEAB) for each programmable controller
 - Controller mounted with DTA 024 or DTA 028 48 + 9
 - Controller mounted with DTA 27.1 48 + 9
 - Controller mounted with DTA 101 or DTA 107 48 + 0

The maximum numbers for the I/O slots and for the I/O points cannot be derived here..The following limits are valid for them:

Table 2 Configuration Limits of the A500

Configuration	I/O Slot	Binary I/O Points (max.) ¹⁾
DTA 024 primary subrack	6 ²⁾	192
DTA 027.1 primary subrack	-	-
DTA 028 primary subrack with DNP 028	10 ²⁾	320
DTA 028 primary subrack with DNO 028	13 ²⁾	416
DTA 101 primary subrack	4	128
DTA 025 secondary subrack	16	512
DTA 102/DTA 112 secondary subracks	4	128
DTA 103/DTA 113 secondary subracks	9	288
DTA 024 with max. I/O configuration via PEAB	149 = 9 x 16 + (6 - 1)	4768
DTA 27.1 with max. I/o configuration via PEAB	142 = 8 x 16 + (16 - 2)	512
DTA 028 with DNP 028 and max. I/O configuration via PEAB	153 = 9 x 16 + (10 - 1)	4896
DTA 028 with DNO 028 and max. I/O configuration via PEAB	156 = 9 x 16 + (13 - 1)	4992
max. I/O configuration via Modnet 1/SFB	159 ³⁾	5088
max. I/O configuration via PEAB and Modnet 1/SFB	159	5088



Note The configuration for the maximum values resulting from pure calculations are not obtained in practice through the use of intelligent function modules and analogue I/O modules.

1) 1) A basis of I/O modules with 32 I/O points is used. The given maximum value is reduced accordingly if modules with fewer I/O points are used (analogue I/O, relay output, ...).

2) If PEAB expansions are configured, an I/O slot must be reserved in the primary subrack for the DKV 023.

3) Each DEA-H1 and each DEA-H1 "uses" 2 I/O slots.

1.5 Recommended Peripherals

1.5.1 Usable Programming Panels

The A500 can generally be programmed with IBM compatible PCs (P...) as well as with a limited number of video terminals (DSG ...). Section 1.6.2 gives further details. The following is recommended:

- | | | | |
|--|--------------------------------|-------------------------|-----------|
| <input type="checkbox"/> P125 | with 240 x 75 mm LCD display, | 80 characters per line, | 25 lines |
| <input type="checkbox"/> P300 | with 231 x 97 mm LCD display, | 80 characters per line, | 25 lines |
| <input type="checkbox"/> P510 | with 198 x 132 mm LCD display, | 80 characters per line, | 25 lines |
| <input type="checkbox"/> P610 | with 216 x 144 mm LCD display, | 80 characters per line, | 25 lines |
| <input type="checkbox"/> DSG 110 ⁴⁾ | with 14 inch screen, | 80 characters per line, | 25 lines. |

Software kits (see section 1.9) can be received for the programming and as a start-up aid. The selection of the programming panels can be limited by these. You will find a survey of which software can be run on which programming panel in section 1.6.2

1.5.2 Usable Printers

All the following printers can be connected to the A500:

- | | | |
|------------------------------------|-----------------------|--|
| <input type="checkbox"/> DRU 292 E | DIN A4 matrix printer | with DRI 29 S/DRI 29 P (serial/parallel interface) |
| <input type="checkbox"/> DRU 293 E | DIN A3 matrix printer | with DRI 29 S/DRI 29 P (serial/parallel interface) |
| <input type="checkbox"/> DRU 1200 | DIN A4 laser printer | with an integrated serial and parallel interface |

The port of the printers to the programming panels and the functions of the individual printers together with the software running on the programming panel is to be taken from the relevant programming panel documentation.

1.5.3 Devices to Program EPROMs

The following is required to burn EPROMs:

- | | |
|---|------------------------------------|
| <input type="checkbox"/> when using ALU 011 or ALU 150: | EPS 2000 EPROM programming station |
| <input type="checkbox"/> when using ALU 061: | EPS 386 EPROM programming station |

It is possible to write programs for the A500 EPROMs with these devices. They can be inserted on the ALU 0x1 or on the SF 8512 when using the ALU 150 so that the programs then run from the EPROM and no longer from the RAM. This can be used to protect the program from an inadmissible change, for example. Another application can be to work without the battery backup of the RAM.

4) The DSG 110 is a "still in sales" model; a successor is not foreseen. The VT 320 device type from DEC can be used if required as a VT 100 compatible video terminal. This is to be ordered directly from Digital Equipment GmbH.

1.6 Programming

1.6.1 Program Generation

The user program can be generated **off-line** or **on-line**. The Bsdol operating communication system integrated in the basic software is used during the on-line programming so that a video terminal (cf. 1.6.2) is sufficient for the programming in this case. The programming panel must be connected to the A500 during the programming.

The program is generated on an IBM compatible PC (cf. 1.6.2) during the off-line programming and the transferred to the PLC. A connection between the programming panel and the PLC is not yet required here during the program generation as opposed to the on-line programming so that the programming can be carried out separately from the A500. However, a prerequisite is an off-line programming software which is to be ordered separately.

1.6.2 Programming Panels

The following are programming panels:

- The P125, P300, P510 and P610 devices with a 3 1/2" disk drive for **off-line programming**. The devices are IBM compatible PCs and are recommended by AEG. Other IBM compatible PCs can also be used if certain prerequisites are fulfilled. The customer services can give you more information about this. It is to be noted that **PCs without a hard disk can only be used in a limited way**. This is relevant for program kits, for example, which consist of more than one diskette. Detailed information about which software can be run on which programming panel is given in table Table 3 and Table 5.
- The DSG 110 video terminal for **on-line programming**. Other video terminals can also be used in the individual case with certain prerequisites. The personal computers mentioned above can also be used. These must then be connected passively with a special program (ARCHIVE → A350/A500).

Table 3 suitable Programming Panels for the Software Kits

Available Software	Suitable Programming Panel			
	P125	P300	P510	P610
Dolog AKF → A350/A500	no	yes	yes	yes
Dolog B → A350/A500	no	no	yes	yes
TESY → A350/A500 → Dolog B	no	no	yes	yes
EDITOR → A350/A500 → Dolog B	no	no	yes	yes
SETUP-LOOP-CTRL → A350/A500 → Dolog B	no	no	yes	yes
COM → AKF	no	no	yes	yes
COM → A350/A500 → Dolog B	no	no	yes	yes
Expert → VIP 101 → AKF35	no	no	yes	yes
Expert → ZAE 105	no	yes	yes	yes
ARCHIVE → A350/A500	yes	yes	yes	yes
PROM → EPS 386	yes	yes	yes	yes
PROM → EPS 2000	yes	yes	yes	yes
VIPIPC → SFB/1N	no	no	yes	yes

1.6.3 Special Programming Languages

The programming is carried out in the special languages of **Dolog AKF** or **Dolog B**. A series of support and start-up aid programs also exist. A survey is given by section 1.9.

Dolog AKF is an off-line programming software according to DIN 19239 (draft) in

- instruction list
- ladder diagram
- function block diagram

Prerequisites: Personal computer plus Dolog AKF → A350/A500 software kit

Performance Features:

- structured programming as an aid
- permits the definition of user function blocks
- offers a supply of standard function blocks
- executes a plausibility and syntax test during the program entry
- permits program changes with the programmable controller running
- permits symbolic programming, signal default and presetting
- permits a dynamic status display of the user program in the instruction list, ladder diagram and function block diagram
- supplies system documentation as an instruction list, ladder diagram and function block diagram with additional information, such as symbolic names, comments, local cross references and occupation lists

Dolog B permits programming in software blocks. Complex links can be programmed in a clear way as well as logic operations using these. Programming can be carried out off-line and also on-line with a limited function scope in Dolog B. The Dolog B → A350/A500 software package is required for off-line programming, the ARCHIVE → A350/A500 software kit for on-line programming on a personal computer. The software kit is not required for on-line programming with a video terminal.

Performance Features:

- structured programming as an aid
- generates programs with dialogue editors or text editors
- permits symbolic programming and signal default
- executes a plausability and syntax test through the compiler
- offers an on-line status display in the graphic function block diagram with an integrated search run and trigger functions
- supplies system documentation in the graphic function block diagram with automatically generated peripheral cross references, occupation lists, cross reference lists and output of the program as a VList.



Note It is stressed that the full scope of functions is not available with on-line programming. The generation of networking tables, for example, is only possible together with off-line program packages.

1.6.4 Principle Structure of a Dolog AKF Program

A Dolog AKF program consists of a succession of program blocks (PB) in its basic structure. These include a sequence of logic operations (selectively programmable in instruction lists, ladder diagrams or function block diagrams) and calling function blocks (FB). The user therefore has access to standard function blocks and can generate own function blocks as well. The program blocks are called by the organization block (OB) (cf. Figure 5). The hierarchical arrangement of organization, program and function blocks simplifies the structured programming.

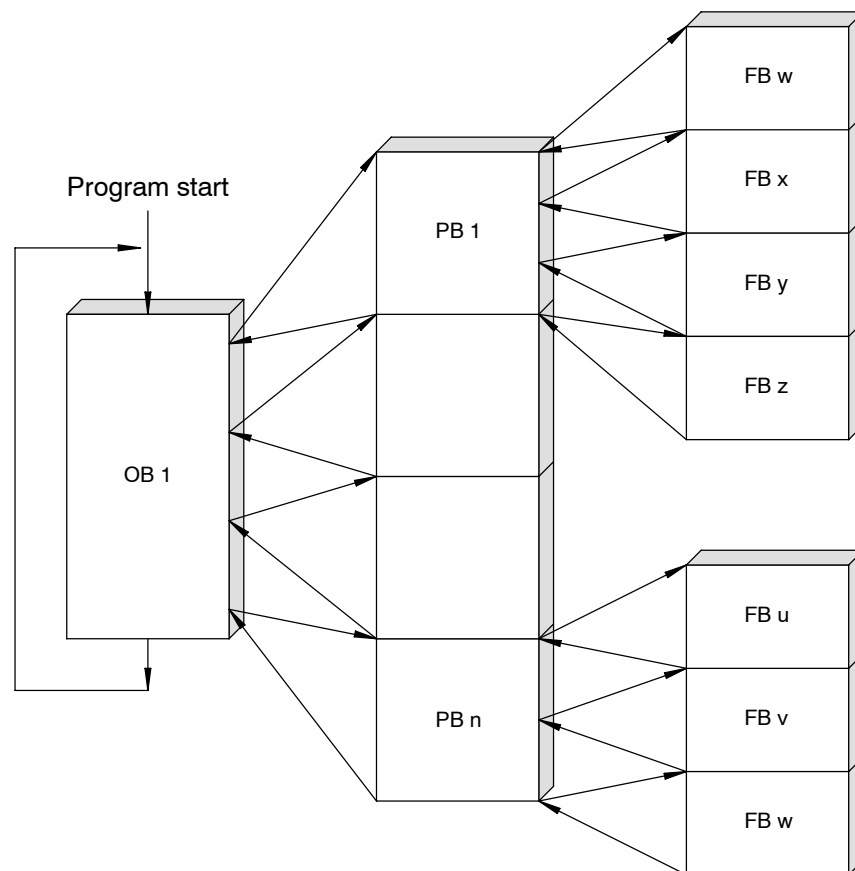


Figure 5 Basic Structure of a Dolog AKF Program

The basic structure can be modified. A program block can call other program blocks; function blocks can be called by the organization block directly or can call other function blocks; the same function block can be called in several program blocks or several times in one program block, etc. The program documentation is saved separately in data blocks.

The following is caused at the end of OB1:

- ☐ Output of the signals from the signal memory to the peripherals
- ☐ Reading in the signals from the peripherals to the signal memory
- ☐ Return to the start of OB1

The description of the Dolog AKF → A350/A500 software kit gives more details.

1.6.5 Principle Structure of a Dolog B Program

Dolog B programs (VLists) consist of a succession of block calls which the processor processes one after the other. Blocks can be: And/Or logic operations, time-counter modules, conditional/unconditional jump commands, etc. The last block in the VList must always be an end block. It causes:

- ❑ The output of the signals from the signal memory to the peripherals
- ❑ The reading in of the signals from the peripherals to the signal memory
- ❑ The return to the first block in the VList

VLists do not have to be structured as linear. Jump blocks (conditional jumps) permit the omission or the addition of individual program parts; subprogram blocks permit the structure of the VList with subprograms. Jump blocks and subprogram blocks permit the structure of a structured program.

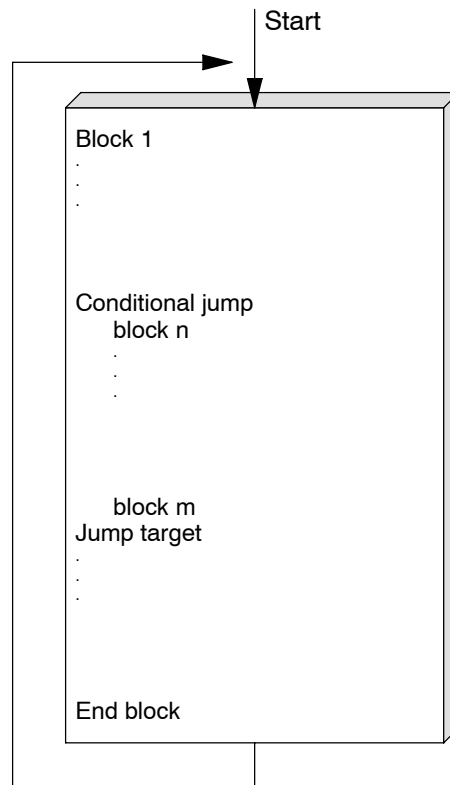


Figure 6 Schematic Structure of a Dolog B Program

Instructions for programming in Dolog B and a list of all Dolog B blocks can be found in appendix A.

1.7 Networking

1.7.1 Overview

The connection of two or more “intelligent units” (**networking nodes**) for the purpose of the data exchange is the general meaning of networking. The transmission path on which the data is exchanged is called a **Bus**. The data to be transferred (messages) are coded and transferred in the form of telegrams. The method of coding (telegram structure) and the type of transfer (serial/parallel) is called the **networking procedure**.

Telegrams can generally only be transmitted with a command. One node only is always justified in giving the command in the bus. it is known as the **master** and can communicate with all the other nodes. Whoever is master is defined by the hardware or software depending on the networking procedure. All the other networking nodes are called **slaves**. They can only communicate with the master and with each other via the master. Figure 7 gives 2 examples. A distinction is made between point-to-point, star or bus connection depending on the topology.

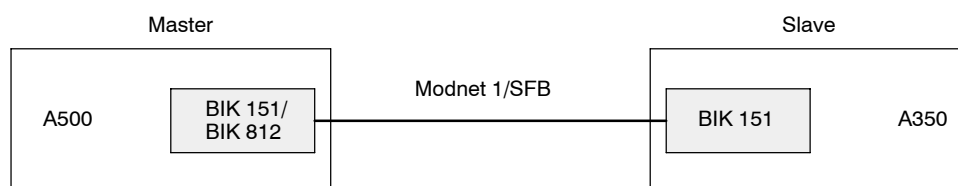


Figure 7 Example of a Point-To-Point Connection via Modnet 1/SFB (Schematic)

Various types of busses are used due to the different transmission requirements (e.g., data throughput, transmission speed) in the various hierarchy level of a networked automation system, whereby this assignment is not forced.

- Field communication → Modnet 1/SFB
- Process communication → Modnet 1/N, Modnet 1/F, Modnet 2/NP
- Process control level → MAP 3

Table 4 Survey of the Types of Networking Which can be Realized with A500

Bus Type	Networking Procedure / Interface	Master ↔ Slave	Required Hardware
Modnet 1/SFB	1N / RS 485	A500 ↔ A500 A500 ↔ A350 A500 ↔ A120 A500 ↔ E/A	BIK 151 / BIK 812 ↔ BIK 151 / BIK 812 BIK 151 / BIK 812 ↔ BIK 151 BIK 151 ↔ ALU 202 BIK 151 ↔ DEA 106 + E/A
	DEA / RS 485		
Modnet 1/N	1N / RS 232C	A500 ↔ A500 A500 ↔ A350	KOS 152 / KOS 882 ↔ KOS 152 / KOS 882 KOS 152 / KOS 882 ↔ KOS 152
Modnet 1/F	1F / RS 232C	A500 ↔ U120 A500 ↔ U130	KOS 152 / KOS 882 + Modem ↔ Modem KOS 152 / KOS 882 + Modem ↔ Modem
Modnet 2/NP	2NP / IEEE 802.4 (10 mm KOAX)	A500 ↔ Koppelpartner	KP1-xxx + Modem ↔ Modem

1.7.2 Modnet 1/SFB Communication

Modicon A500 can communicate with other devices via the BIK 151 / BIK 812 as a master or slave on the Modnet 1/SFB (see Figure 8). 1N and DEA logs can be run via this bus. The interface used for the communication is an RS 485 interface which is located on the BIK.

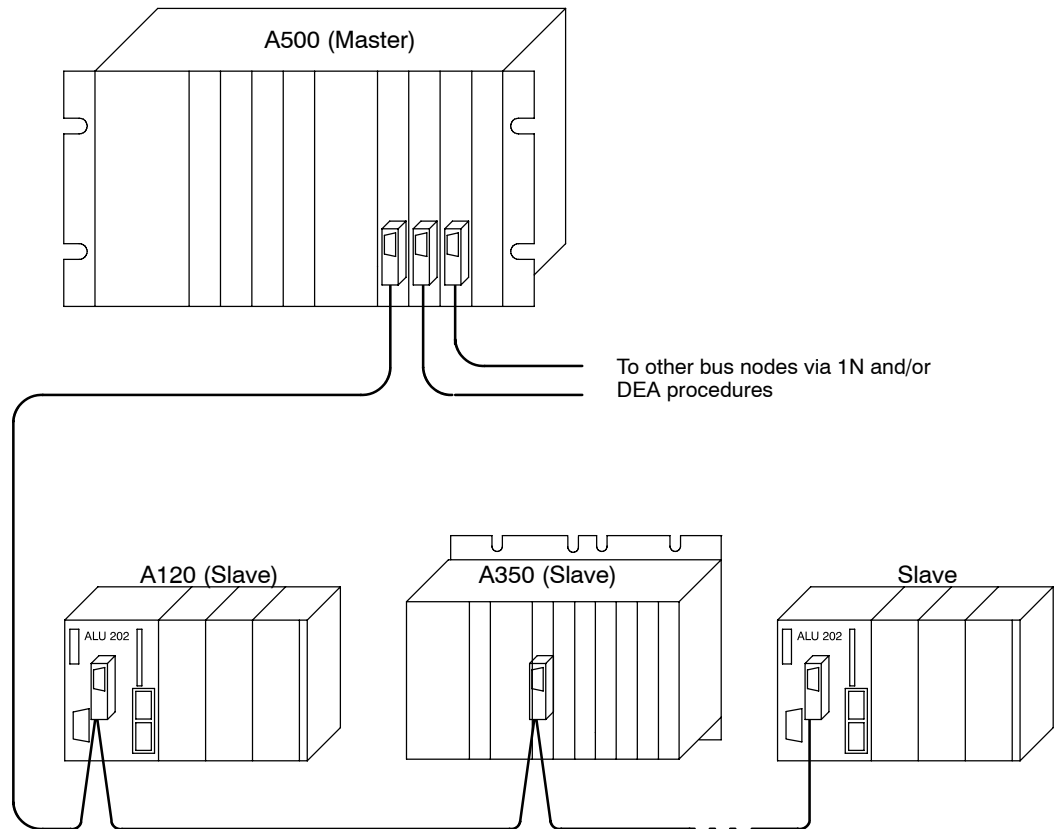


Figure 8 Example of a communication between A500 (Master) and A350 and A120 (Slaves)

The Following is Possible as a Master:

- ❑ BIK 151 or BIK 812 interface module in an A500
- ❑ BIK 151 interface module in an A350

The Following is Possible as Slaves:

- ❑ BIK 151 or BIK 812 interface module in an A500
 - ❑ BIK 151 interface module in an A350
 - ❑ ALU 202 in an A120
 - ❑ I/O bus link to DEA 106, DEA 116
 - ❑ I/O bus link to DEA-H1, DEA-K1
- } for 1N logs
 } for DEA logs

The following configuration limits are valid for the Modnet 1/SFB communication:

- ❑ 4 BIK modules per A350/A500, including max. 3 for 1N procedures
- ❑ 28 slaves per master (BIK ...), including max. 16 I/O bus links (DEA ...)

More detailed information can be found in the module descriptions of the interface modules (ALU 202, BIK 151, BIK 812).

1.7.3 Modnet 1/N Communication

Modicon A500 can be connected to other programmable controllers (e.g., A500) or to a superior process control system, such as, e.g., Viewstart B500 or to a process control computer of the Modcomp family. There are the following hardware prerequisites for A500:

- KOS 152 with Modnet 1N / Tesy firmware or with Modnet 1F / 1N firmware
or
- KOS 882 with DSW 088/99 (bus networking) or DSW 078/99 (star network) firmware

The functions available for the networking are included in the basic software belonging to the delivery scope and can be executed on-line. Only the networking tables must be generation off-line. These are then stored in the RAM of the SC 8128 or SC 8256 or on EPROM of the SF 8512. The COM → A350/A500 software kit required here is therefore only necessary in the configuration stage of the link-up.

A detailed description of the networking configuration is given in a separate document (see documentation catalogue) and the documentation enclosed with the communications software kits.

1.7.4 Modnet 1/F Communication

Modicon A500 can be connected to a telecontrol line as a telecontrol station via the Modnet 1/F bus. There are the following hardware prerequisites for A500:

- KOS 152 with Modnet 1F / Modnet 1N firmware
or
- KOS 882 with DSW 188/99 firmware

A detailed description of the networking configuration is given in a separate document (see documentation catalog).

1.7.5 Modnet 2/NP Communication

Modicon A500 can be connected to other programmable controllers (e.g., A500), to a superior process control system or to a process control computer of the Modcomp family via Modnet 2/NP.

The Modnet 2/ NP system bus (topology: bus) is connected by the KP1 ... communication module with an integrated modem and a coax port. The Modnet 2/NP operates with the token access method and therefore guarantees interference-free access for all nodes.

It is used where message transmissions with a medium distance, a large number of nodes and a very high data transmission volume must be set up.

The Modnet 2/NP can also be expanded in the future to the system operating which is a great improvement on the performance of the remote diagnosis. This means that a direct connection of one programming panel to the Modnet 2/NP is therefore possible and therefore also the functions of remote operation and downloading, remote archiving between the programmable controller, programming panel and central program organization.

A detailed description of the networking configuration is given in a separate document (see documentation catalogue).

1.8 Tesy

The Tesy software kit allows the input and output of text and data to peripherals. It is thus possible to set up an operator interface for the A500 via a video terminal (MMI⁵⁾). This operator interface only permits interventions into the process which the user has expressly foreseen. Process data can be requested or the processing sequence affected in the A500, e.g., by the default of new setpoint values or by the selection of a new processing stage with step chains. The current process status can also be logged on a printer.

There are the following hardware prerequisites for A500:

- KOS 152 with Modnet 1N / Tesy firmware
- or
- KOS 882 with DSW 135/99 firmware

The software required for the programming is part of the supplied basic software. A more comfortable possibility for entering the program is offered by the off-line "Tesy → A350/A500" program kit.

A detailed description of the Tesy configuration is given in a separate document (see documentation catalog).

5) MMI = **Man-Machine-Interface**

1.9 Survey of the Usable Software Packages

Table 5 gives a survey and a short description of the features of the available software kits. They are identical for A350 and A500. Further information can be found in the programming instructions enclosed with the software kits.

The software kits are supplied in a slip case. It includes the software on 3 1/2"- and 5 1/4" diskettes and the program documentation.

Table 5 Survey of the Software Available for the A500

Name	Performance Features	Comments
INSTAL → Programming unit	simplified installation of the MS-DOS operating system	only for programming panels with a hard disk included in the delivery scope of the AEG programming panels
Dolog AKF → A350/A500	Specialist programming language according to DIN 19 239 in instruction lists, ladder diagrams, function block diagrams, cf. 1.6.3 and 1.6.4	can only be run on programming panels with a hard disk
Dolog B → A350/A500	Specialist programming language for programming in the block method, cf. 1.6.3 and 1.6.5	can only be run on programming panels with a hard disk
ARCHIVE → A350/A500	for on-line programming with a PC to archive Dolog B programs generated on-lined on-line	can be run on P125, P300, P510, P610 included in the delivery scope of the EPS 2000
COM → A350/A500 → Dolog B	Configuration and start-up of distributed systems (networking structures) PADT ⁶⁾ ↔ programmable controller link possible via RS 485 interface (Modnet 1/SFB) with the full performance capability of the PADT	can only be run on programming panels with a hard disk can only be run together with the Dolog B → A350/A500 software kit
SET UP LOOP CTRL. → A350/A500 → Dolog B	to support the start-up, e.g., displaying markers and works, changing parameter sentences, block by block	can be run on P125, P300, P510, P610 can only be run together with the Dolog B → A350/A500 software kit
TESY → A350/A500 → Dolog B	to set up an operator interface, e.g. displaying events and errors, generating error lists, etc.	only for programming panels with a hard disk can only be run together with Dolog B → A350/A500 and Editor → A350/A500 → Dolog B
Editor → A350/A500 → Dolog B	Screen text editor to generate Dolog B programs and Tesy files	only for programming panels with a hard disk can only be run together with the Dolog B → A350/A500 software kit
EXPERT → VIP 101 → AKF35	configuration software for VIP 101	only for programming panels with a hard disk can only be run together with the Dolog AKF → A350/A500 software kit
PROM → EPS 2000	for burning and reading EPROMs on the EPS 2000 EPROM programming station	can be run on P125, P300, P510, P610 included in the delivery scope of the EPS 2000

6) PADT = programming and debugging tool

1.10 Module Survey

Table 6 Survey of the Modules Available for the Controller of the A500

Module	Function
Physical Characteristics	
DTA 024	Primary subrack with rear connection, 19" construction width
DTA 27.1	Primary subrack with rear connection, 19" construction width
DTA 028	Primary subrack with rear connection, 19" construction width
DTA 101	Primary subrack with front connection, 19" construction width
DTA 107	Primary rack with front connection, 19" construction width
FIX 001	Mounting flange for DTA 101, DTA 103/113, DTA 107
Central Processing Units	
ALU 011	Central processing unit
ALU 061	Central processing unit
ALU 150	Central processing unit
COP 82	Co-process for ALU 011, ALU 061, ALU 150
MAT 827	Connecting socket with 8087 arithmetic processor for ALU 150 (Floating point processing, controlling)
Memory Modules, Monitoring Modules	
SC 8128	Memory module, 128 kB RAM
SC 8256	Memory module, 256 kB RAM
SF 8512	Memory module, 512 kB EPROM, unequipped
UKA 024	Monitoring module
Power Supplies	
DNP 023	Power supply, 230 VAC primary, with isolation
DNP 023-1	Power supply, 24 VDC primary, with isolation
DNP 023-2	Power supply, 48 VDC primary, with isolation
DNP 023-3	Power supply, 24 VDC primary, with isolation
DNP 023-4	Power supply, 48 VDC primary, with isolation
DNO 028	Power supply, 24 VDC primary, without isolation
DNP 028	Power supply, 230 VAC primary, with isolation
Modnet 1/SFB Interface Modules and I/O Bus Communication	
BIK 151	Modnet 1/SFB networking (front connection) with 1 RS 485 interface
BIK 812	Modnet 1/SFB networking (rear connection) with 1 RS 485 interface
DKV 023	PEAB networking in the controller
Modnet 1/N Interface Modules	
GDUE 12	Remote I/O interface with a high transmission rate for the use with Slave-KOS
KOS 152	Communication processor (front connection) for Modnet 1/F and for Modnet 1/N networks, with 2 RS 232C/LS interfaces
KOS 882	Communication processor (rear connection) for Modnet 1/F and for Modnet 1/N networks, with 4 RS 232C/LS interfaces
LABKO 1	Remote I/O interface with DC data transfer
LABKO 12	Remote I/O interface with DC data transfer for the use with Slave-KOS
SEA 020	Asynchronous serial communication control unit
UVL 841	RS 232C / signal transformer in the memory bus area (PMB)
UVL 842	RS 232C / LS signal transformer in the I/O bus area (PEAB)
Modnet 2/NP Interface Modules	
BK1	Carrier band modem
KP1-B	Communication processor with firmware (ICOS basic version)
KP1-BC5	Communication processor with firmware (ICOS basic version) and modem
KP1-E	Communication processor with firmware (expanded ICOS version)
KP1-EC5	Communication processor with firmware (expanded ICOS version) and modem

Table 7 Modules for Setting up the I/O Peripherals with Front Connection

Module	Function
Physical Characteristics	
DTA 102	Secondary subrack for distributed I/O via DEA 106/DEA 156, 1/2 19"
DTA 103	Secondary subrack for distributed I/O via DEA 106/DEA 156, 19"
DTA 112	Secondary subrack for distributed I/O, construction width 1/2 19"
DTA 113	Secondary subrack for distributed I/O, construction width 19"
FIX 001	Mounting flange for DTA 101, DTA 103/113
Modnet 1/SFB Communications	
DEA 106	Modnet 1/SFB communication for DTA 102, DTA 103, 0.8 A
DEA 116	Modnet 1/SFB communication for DTA 112, DTA 113
DEA 156	Modnet 1/SFB communication for DTA 102, DTA 103
Analogue Value Processing	
ADU 115	16 analogue inputs, I/R/U
ADU 116	16 analogue inputs, U/I
DAU 104	8 analogue outputs, I/R/U,
DAU 108	8 analogue outputs, U/I
Binary Value Processing	
DAP 102	16 binary outputs, 24 VDC/2 A and 16 binary inputs, 24 VDC/7 mA
DAP 103	16 relay outputs, 24 VDC/VAC ... 230 VAC and 16 binary inputs, 24 ... 60 VDC
DAP 104	8 relay outputs, 24 VDC/VAC ... 230 VAC and 8 binary inputs, 110/230 VAC
DAP 106	16 relay outputs, 24 VDC/VAC ... 230 VAC
DAP 112	32 binary outputs, 24 VDC / 0.5 A
DEP 112	32 binary inputs, 24 VDC
DEZ 160	32 binary inputs, 24 ... 60 VDC, with real-time recording
Intelligent Function Modules	
NOK 116	Cam controller
VIP 101	Visual display module
ZAE 105	Fast counter

Table 8 Modules for Setting Up I/O Peripherals with Rear Connection

Module	Function
	Physical Characteristics
DTA 025	Secondary subrack for central I/O, construction width 19"
DUV 025	Connecting printed board for DTA 025 with bus port
	Power Supplies
DNP 025	Power supply for DTA 025, 230 VAC
DNP 026	Power supply for DTA 025, 24 VDC
	Function Modules for the PEAB
DKV 022	PEAB link in the DTA 025
DKU 022	PEAB monitoring in the DTA 025
	Analogue Inputs, Conversion Method According to the Step Encoder
ADU S9	16 inputs, unipolar
ADU S12	14 inputs, unipolar/bipolar switch-over / bipolar
AEM 2511.110B	16 inputs, bipolar
AEM 2511.110U	16 inputs, unipolar
EMU 2610	Semiconductor multiplexer for AEM 2511
MWE 32	Semiconductor multiplexer for ADU S9, 2x16 channels
	Analogue Inputs, Integrating Conversion Method
ADU I13.2	1 input, bipolar, 3 measuring ranges
ANV 1.2	Matching amplifier for ADU I13.2
MWE 16x2	Semiconductor multiplexer for ADU I13.2, 16 channels
MWE QR1	Relay multiplexer for ADU I13.2, 16 Kanäle
	Analogue Outputs
MWA 012	8 outputs, unipolar/bipolar switch-over /
MWA 16PN	16 outputs, bipolar
	Binary Outputs, Non-Isolated
DAO 012	32 outputs, 24 VDC, 100 mA, permanently memorizing, display
DAO 013	32 outputs, 24 VDC, 100 mA, permanently memorizing, display, simulation
DAV 001	2x8 outputs, 24 VDC, 2 A, short-term/permanently memorizing, display
DAV 002	16 outputs, 24 VDC, 500 mA, display
	Binary Outputs, Isolated
DAP 002	4x8 outputs, 24 VDC, 400 mA, display, simulation
DAP 004	2x8 outputs, 24/60 VDC, 210 mA, display, simulation
DAP 006	4x4 outputs, 24 VDC, 500 mA, display
DAP 015	16 outputs, 230 VAC, 2 A, contacts, display, simulation
DAP 016	16 outputs, 115 VAC, 2 A, contacts, display, simulation
DAP 017	DAP 016, with RC protective circuits
	Binary Inputs, Non-Isolated
DEO 011	32 inputs, 24 VDC, 4 mA
DEO 012	32 inputs, 24 VDC, 4 mA, display
DEO 013	32 inputs, 24 VDC, 4 mA, display, simulation
	Binary Inputs, Isolated
DEP 002	32 inputs, negating, 24 VDC, -5 mA
DEP 005	32 inputs, 60 VDC, 2.7 mA
DEP 007	16 inputs, 24/60/110 VDC, 5 mA, display, simulation
DEP 012	32 inputs, 24 VDC, 5 mA, display
DEP 013	32 inputs, 24 VDC, 5 mA, display, simulation
DEP 014	8x2 inputs, 230 VAC, 5 mA, display, simulation
DEP 016	8x2 inputs, 115 VAC, 5 mA, display, simulation
SES 2	16 spontaneous inputs, 24 VDC, 10 mA
	Intelligent Function Modules
BUR 001	Back-up control
DBS 001	digital back-up controller, 32 inputs, 8 outputs
DOZ 001	Batching counter
POS 001	Single-axis controller for controlled / switched drives
POS 002	Single-axis controller for switched drives
POS 011	Single-axis controller for absolutely controlled / switched drives

Table 9 Operating Devices

Device	Function
Operating Devices to be Installed on PEAB Slots	
DBK 021	DAP
DPL 011	HEX input/output
Operating and Control Devices to be Installed in the Process Peripherals	
BLG 301	Operating and control devices for back-up control
BLG 305	Operating and control devices for batching counter
DBK 111	Operating panel for POS 001, POS 002, POS 011

Table 10 Cables

Cable	Function
JE-LiYCY	System field bus cable, in meters
MDL 66.1	PEAB extension without DKV 023
MDL 67	PEAB extension with DKV 023
VKX 104	Coax cable for VTH 104 ↔ colour monitor, 6 m long
VKX 114	4.fold mini.coax cable for VIP 101 ↔ VTH 104, 2 m long
YDL 40	Bus cable for BIK ↔ DEA, 40 cm long
YDL 053	Cable for VIP 101 ↔ printer (RS 232C), 3 m long
YDL 054	Cable for VIP 101 ↔ printer (current loop), remote, 3 m
YDL 101	Cable for VIP 101 ↔ RGB monitor, 2.5 m long
YDL 102	Cable for VIP 101 ↔ PBT 102 standard keyboard, 1.5 m long
YDL 103	Cable for VIP 101 ↔ PBT 103 membrane keyboard, 3 m long
YDL 104	Cable for VIP 101 ↔ printer (RS 232C / LS), 5 m long
YDL 105	Cable for VIP 101 ↔ programming panel (P510/P610), 3 m long
YDL 106	Cable for connecting board on YDL 108 ↔ PBT 103 membrane keyboard, 6m
YDL 107	Cable for VIP 101 ↔ MTP 001 for printer (RS 232C, LS), 2 m
YDL 108	Cable for VIP 101 ↔ MTR for PBT 102, PBT 103, 2 m long

Table 11 Accessories

Accessories	Function
LLB	Air guide
MTP 001	Connecting board of 2HE/4T for MTR (25 pole Cannon connector)
MTR 101	Mounting carrier for process cable
MTR 102	Mounting carrier for process cable
SAE 2	Cabinet connection unit
VTH 104	Connecting board of 2HE/8T for MTR with a coax adapter
BBS 1	RS 485-connector
SIM 011	Simulator for 8 binary inputs (for modules with front connection)
DCF 77E	Time of day receiver
	Console for DCF 77E

Chapter 2

Operating

This chapter is only concerned with the topics which are relevant for the operator of an A500 running in the process, divided according to operating and indicating elements as well as simple maintenance works. It shows the possibility concerning the structure of an operator interface and supplies catch points which are significant for the compilation of system-/application-specific operating instructions and maintenance schedules for the Modicon A500.

2.1 Indicating Elements

Most of the modules of the controller has LED indicators at their disposal for the purpose of diagnosis. There are LEDs in **green** and **red**. Their meanings for each module are clearly given in the following:

ALU 011 Central Processing Unit

- | | | | |
|-------------|--------|---------------|---|
| □ green LED | "run" | lights up: | User program runs over END, cycle monitoring time is not exceeded |
| | | has gone out: | Faulty user program or processor sequence |
| □ red LED | "batt" | lights up: | Rechargeable battery has undervoltage at the time when the system is switched on or after the rechargeable battery test |
| | | has gone out: | Rechargeable battery voltage in the nominal area or not tested |

ALU 061 Central Processing Unit

- | | | | |
|-------------|-------------|---------------|---|
| □ green LED | "run" | lights up: | User program runs over END, ; cycle monitoring time is not exceeded; event relay is applied |
| | | has gone out: | The user program is not started or there is a faulty processor sequence; cycle monitoring time exceeded; marker 60 = 1; event relay has dropped out |
| □ red LED | "watchdog" | lights up: | User program is not running within the max. permitted cycle time |
| | | has gone out: | User program is running |
| □ red LED | "> 70 °C" | lights up: | Excess temperature reached |
| | | has gone out: | No excess temperature |
| □ red LED | "batt test" | lights up: | Rechargeable battery undervoltage at the time when the system was switched on |
| | | has gone out: | Rechargeable battery voltage in the nominal range or not tested at the time when the system was switched on |
| □ green LED | "batt test" | lights up: | Load test of the rechargeable battery was successful |
| | | flashes: | Undervoltage of the rechargeable battery during the load test |
| | | has gone out: | Undervoltage of the rechargeable battery between 2 load tests |

DNP 023, DNP 023-x, DNP 028 Power Supply

- | | | | |
|-------------|---------------|---------------|---|
| □ green LED | "Operation" | lights up: | Supply voltage of the entire system is in the nominal range |
| | | has gone out: | Supply voltage of the system is not in the nominal range |
| □ red LED | "Malfunction" | lights up: | Malfunction on the power supply |
| | | has gone out: | No malfunction on the power supply |
| □ green LED | "Mains" | lights up: | Primary voltage is present |
| | | has gone out: | Primary voltage is not present |

UKA 024 Monitoring Module

□ green LED	"watchdog"	lights up:	User program is running within the set cycle time: voltage to be monitored in the nominal range: event relay is applied
		has gone out:	User program has not started, faulty processor sequence; cycle monitoring time is exceeded or the voltage to be monitored is not in the nominal range: event relay has dropped out and marker 60 = 1
□ green LED	"vchk"	lights up:	The voltage fed to the E 48M connector of the UKA and to be monitored is outside the nominal range and "SUE" jumper is plugged in
		has gone out:	No undervoltage or "SUE" jumper not plugged in
□ red LED	"cycl"	lights up:	The cycle monitoring time set on the module is exceeded
		has gone out:	Program is running within the set cycle time
□ red LED	"PEAB"	lights up:	Marker 61 = 1 (PEAB group error, e.g., DKU
			has detected a PEAM transmission error)
□ red LED	"PMB"	lights up:	Marker 61 = 0
		has gone out:	Marker 62 = 1 (memory bus group error)
□ red LED	">70 °C"	lights up:	Marker 62 = 0
		has gone out:	Excess temperature is reached
□ red LED	"V _{bat} "	lights up:	No excess temperature
		lights up:	Rechargeable battery undervoltage at the time when the system was switched on
□ green LED	"V _{bat} "	lights up:	Rechargeable battery voltage in the nominal range at the time when the system was switched on
		flashes:	Rechargeable battery voltage in the nominal range after a rechargeable battery load test
□ green LED	"PD"	lights up:	Rechargeable battery voltage outside the nominal range after a rechargeable battery load test
		has gone out:	Rechargeable battery voltage outside the nominal range between 2 rechargeable battery load tests
□ red LED	"break"	lights up:	Programming panel is connected and M5 signal given
		has gone out:	There is no programming panel connected or the M5 signal is not given
□ red LED	"break"	lights up:	Connected programming panel sends "Break" and the "Breake → Reset" jumper is closed (as delivered)
		has gone out:	Programming panel does not send "Break" or the "Break → Reset" jumper is open

Other indicating elements are not present on the controller. The meaning of the LEDs on the I/O modules is described in section 2 of the user manuals for the relevant I/O peripherals (front or rear connections)

2.2 Switches, Contact Sockets, Push Buttons

2.2.1 Switches

DIP switches are located on the ALU 011 and behind the cover on the ALU 061. Since they are not operating elements, they are not treated in more detail at this point.

2.2.2 Contact Sockets

Contact sockets are located on the ALU 011, ALU 061, ALU 150, UKA 024, SC 8128, SC 8256 and the DKV 023. They have the following meaning:

UKA 024, ALU 011, ALU 061

- B2 B500 transparent mode, no operating element
- B4 Freely available bit defined by software

SC 8128

- SS1 Writing protection for 1st 64 kbyte block
- SS2 Writing protection for 2nd 64 kbyte-block

SC 8256

- SS1 Writing protection for 1st and 2nd 64 kbyte blocks
- SS2 Writing protection for 3rd. and 4th 64 kbyte block

ALU 150, ALU 011, ALU 061

- set automatic SYRES, (close B1 jumper on UKA as well with ALU 150)
- reset no operating element
- Q program enable despite rechargeable battery undervoltage (with ALU 011 only)
- batt acknowledging the rechargeable battery undervoltage, triggering a recharging battery load test, program enable despite rechargeable battery undervoltage (with ALU 061 only)

DKV 023

- FAX Interrupt evaluation for test and start-up purposes, no operating element



Caution The jumpers on the modules are not operating elements. They should not be changed by the operator.

2.2.3 Push Buttons

Error messages can be acknowledged with the “ACK” push button on the front panel of the UKA 024 if the errors are no longer valid at the time of acknowledgement.



Note Starting the A500 is blocked if the rechargeable battery has undervoltage when the A500 is switched on. This blockage can be removed by pressing the “ACK” push button on the UKA.

2.3 Changing the Rechargeable Battery (Maintenance)

A rechargeable battery integrated in the primary subrack serves to backup the RAM on the ALU (system RAM, also user program with ALU 011 and ALU 061) and the SC 8128 or SC 8256 (user program).

The rechargeable battery is accessible from the front (DTA 101 or DTA 107) or from the rear (DTA 024, DTA 27.1, DTA 028) depending on the subrack used. The exact position is given in the module description of the subracks.

The rechargeable battery⁷⁾ has to be changed if

- ☐ the green LED "V_{bat}" on the UKA 024 has gone out (only when using the ALU 150)
- ☐ the red LED "batt" on the ALU 011 lights up
- ☐ the green LED "batt" on the ALU 061 goes out
- ☐ the replacement date on the sticker has been reached. The sticker is located on the cover of the battery compartment for the DTA 101 and DTA 107; it is stuck on to the rechargeable battery for the other subracks.

If the LEDs on the ALU or UKA do not signalize undervoltage of the rechargeable battery, the battery can be changed without interruption even if the supply of the A500 is switched off. The rechargeable battery port on the subrack is therefore designed as double. Proceed as follows to change the rechargeable battery:

- 1 Open the rechargeable battery compartment (for DTA 101 and DTA 107 only) and loosen the rechargeable battery from the threaded joint **ohne** disconnecting the supply line from the rechargeable battery to the subrack.
- 2 Connect the new rechargeable battery and fix it to the subrack.
- 3 Now loosen the supply line of the previous rechargeable battery from the subrack and close the compartment of the rechargeable battery (for DTA 101 and DTA 107 only).
- 4 Enter the new replacement date on the sticker.

The following is valid for the life time of the rechargeable batteries:

- ☐ with an operating temperature of 20 °C > 5 years, typically 10 years
- ☐ with an operating temperature of 50 °C: > 2 years, typically 5 years



Caution Used rechargeable batteries are special refuse. Please dispose of them in the special disposal containers.

7) E-No. 424 142 148

2.4 Setting Up an Operator Interface

Setting up an operator interface via Tesy or Viewstar is recommended for the operation of the A500. Only process interventions which are expressly intended by the operator are possible via an operator interface. The following possibilities are available:

- ☐ TESY with KOS 152 or KOS 882 and Modnet 1N / Tesy firmware
- ☐ Viewstar 200 XA with VIP 101
- ☐ Viewstar 200 PC with an IBM AT compatible PC
- ☐ Viewstar B500

You will find more detailed information in the documentation assigned to these products.

Operating Devices

Operating devices are required to:

- ☐ Change the process parameters, e.g., time and counted measurands
- ☐ Track the process sequence, e.g., status indicators
- ☐ For the error diagnosis, e.g., error list output, explanatory text output, requesting the system markers, updating the setting parameters, etc.

The following is suitable as operating devices:

- ☐ passively switched programming panels, e.g., P125, P300, P510, P610 or other passively switched IBM AT compatible PCs (cf. page 12, section 1.6.2).
- ☐ DSG 110⁸⁾ video terminal



Warning Connecting an operating device to the serial interface of the UKA or the ALU 0x1 permits the operator to make serious interventions in the process. The user therefore has to ensure that dangerous process statuses are avoided. Setting up a separate operator interface via tesy or Viewstar is recommended to avoid such situations. This interface only permits process interventions expressly intended by the operator.

Printers

Printers are necessary to print out error lists, explanatory text messages, changed process parameters. Recommended printers are listed in section 1.5.2 (page 11).

Information about the connection, connection cables, start-up and operation of the devices can be found in the operating instructions of the relevant printers.

8) The DSG 110 is a "still in sales" model; a successor is not foreseen. The VR 320 device type of DEC can be used as a VT 100 compatible video terminal if necessary. This device is to be ordered directly from Digital Equipment GmbH.

2.5 Switching the Supply Voltage On and Off

The supply voltage is switched on and off by:

- The user switching the system on and off
- The system being switched on and off by a powerfail

It is to be ensured in both cases that dangerous process statuses do not occur during the voltage failure or when the voltage returns. This is to be stressed especially for a powerfail since the voltage returns at an undefined time as opposed to the system being switched on and off by the user.

2.5.1 The System is Switched On and Off by the User

The programmable controller is switched on and off via the central power supply (power supply in Fig. Figure 25 on page 19) Check that all the measures mentioned in point 2.5.3 are guaranteed before you switch off the system.

2.5.2 The System is Switched On and Off by a Powerfail

The risk of a powerfail is permanent. Therefore always ensure that the measures mentioned in point 2.5.3 are guaranteed.

2.5.3 Check Measures (Inspection)

- **Always Ensure an Intact Rechargeable Battery**
Ensure that the rechargeable battery in the primary subrack is functioning correctly so that the program and data are not lost if the voltage supply should fail. A used rechargeable battery is therefore to be replaced immediately.
- **Do not Adjust DIP Switches**
DIP switches can be found on the SC 8xxx and ALU 0x1 modules and serve to set the writing protection and some status bits (ALU 061 only). Their position is determined in the configuration stage and may not be adjusted afterwards (basic rule). Exceptions are to be mentioned explicitly.

Chapter 3

Configuration

This chapter contains detailed configuration guides, hardware settings and installation guidelines with notes for the system start-up for the A500.

3.1 Configuration of the Hardware

The A500 consists of a **controller** and the **I/O peripherals**, i.e., one of a number of I/O modules which depends on the task. It can be assembled specifically for the respective application due to its modular structure. Standard equipment is available for standard applications and it can be expanded with a memory and I/O peripheral.

3.1.1 Structure of the Controller

The controller consists of a central subrack (DTA 024, DTA 27.1, DTA 028, DTA 101 or DTA 107) which must be equipped with special modules. These modules are summarized in table 6. The most important ones are:

- ❑ **Power Supply**; DNP 023, DNP 023-1, DNP 023-2, DNP 023-3, DNP 023-4, DNO 028 or DNP 028 depending on the subrack and primary voltage
- ❑ **Central Processing Unit**; ALU 011, ALU 061 or ALU 150 depending on the performance capability
- ❑ **Monitoring Module**; UKA 024 (only required when using the ALU 150)
- ❑ **Memory Module**; SC 8128 or SC8256 with RAM elements (only required when using the ALU 150)
- ❑ **Memory Module**; SF 8512 for EPROM elements (only required when using the ALU 150)
- ❑ **PMB Nodes**, such as BIK 151, BIK 812, KOS 152, KOS 882, KP1-..., etc. (depending on the task)
- ❑ **PEAB Communication** DKV 023 (only required with PEAB expansions)

The power supply and central processing unit are always necessary. The UKA 024 monitoring module and at least one memory module are also to be inserted when using the ALU 150. In contrast to that all other modules are optional, i.e., foreseen for special applications. 2 examples:

The DKV 023 is required if I/O modules with rear connection are to be used and more than one secondary subrack is necessary (cf. section 3.1.2.2). It is inserted on a slot in the PEAB area.

The BIK is required if I/O modules with front connection are to be used (cf. section 3.1.2.1) or networking is to be set up via Modnet 1/SFB. It is inserted on a slot in the PMB area.


The controller modules are either PEAB nodes and therefore to be inserted on a slot in the PEAB area or PMB nodes and to be operated on a slot in the PMB area. The area (PEAB or PMB), to which the corresponding module is to be assigned, is indicated in the module description of each individual module in the specifications under the "structure" title.

The modules can generally be inserted anywhere within their structure. However, there are some limits. These include the fact that the PMB and PEAB areas are arranged differently depending on the subrack. Detailed information about the equipment of subracks is therefore to be found in the module descriptions of the subracks.



Note Pay attention to the configuration limits mentioned in section 3.1.3!

3.1.1.1 Structure of the Controller with the STA 501 / STA 551

 **Note** Expansions with front connection and rear connection are possible with the STA 501 and STA 551 standard equipment.

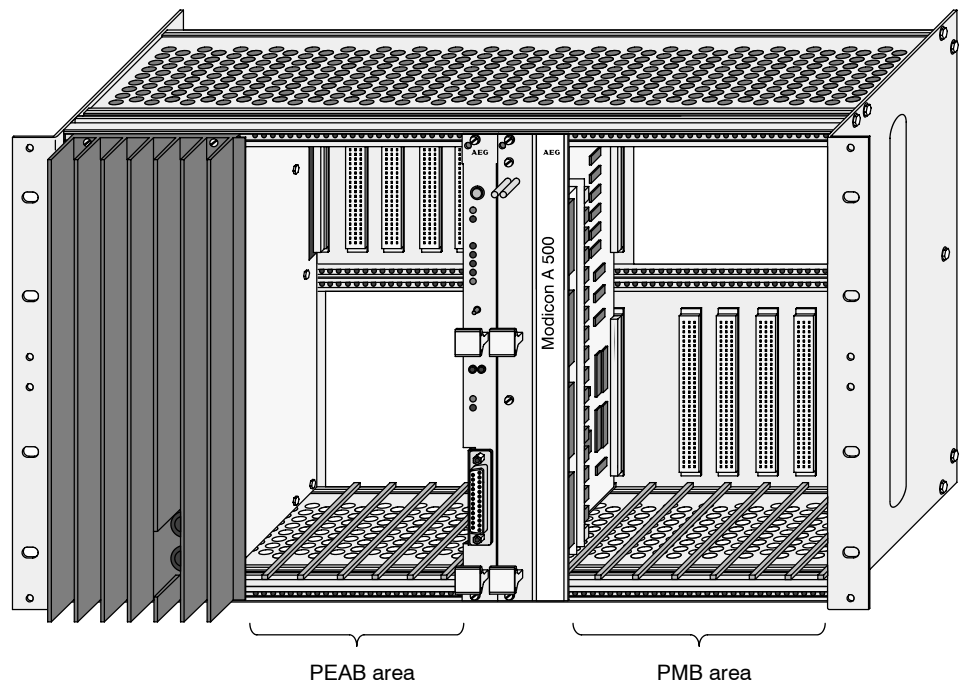



Figure 9 STA 551 Standard Equipment

The STA 501 and STA 551 standard equipment is designed for various primary voltages (24 VDC for STA 501 or 230 VAC for STA 551). They are designed with rear connection and consist of:


Table 12 Equipping the STA 501 and STA 551 Standard Equipment

	STA 501	STA 551
Subrack	DTA 024	DTA 024
Power supply	DNP 023-1 (24 VDC, primary)	DNP 023 (230 VAC, primary)
Monitoring module	UKA 024	UKA 024
Central processing unit	ALU 150	ALU 150

STA 501 and STA 551 have 6 free **PEAB slots** and 7 free **PMB slots**. The PEAB slots can be equipped with I/O modules with rear connection, the PMB slots with memory and interface modules, for example.

 **Note** DNP, UKA and ALU are fixed to their slots. The slots for the PMB and PEAB modules can be freely selected within their structure.

3.1.1.2 Structure of the Controller with the STA 503 / STA 553

 **Note** Expansions with front connection and rear connection are possible with the STA 503 and STA 553 standard equipment.

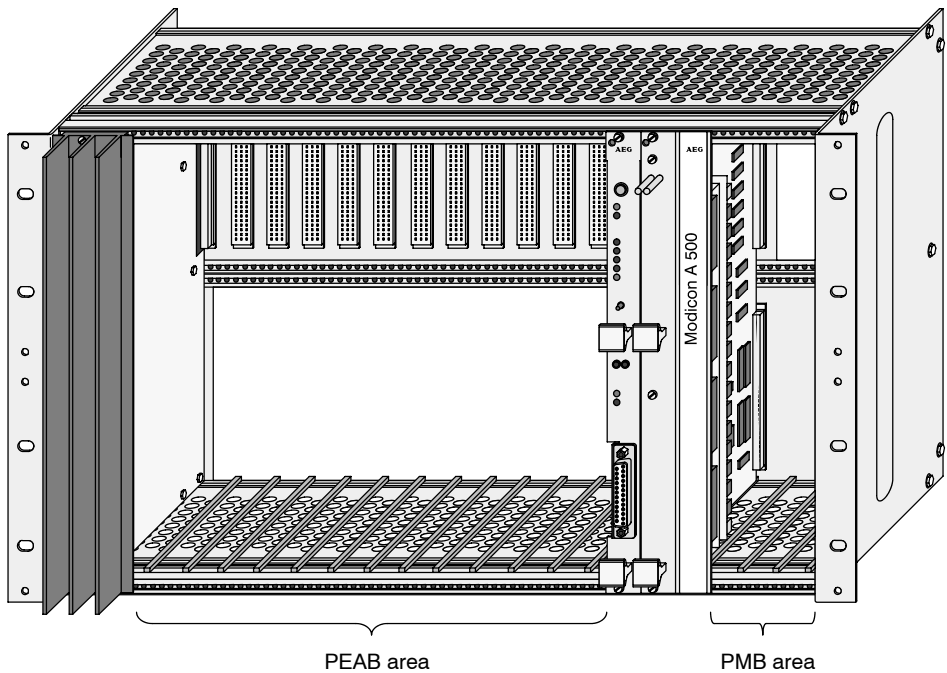



Figure 10 STA 503 Standard Equipment

The STA 503 and STA 553 standard equipment is designed for various primary voltages (24 VDC for STA 503 or 230 VAC for STA 553). It is designed with rear connection and consists of:


Table 13 Equipping the STA 501 and STA 551

	STA 503	STA 553
Subrack	DTA 028	DTA 028
Power supply	DNO 028 (24 VDC, primary)	DNP 028 (230 VAC primär)
Monitoring module	UKA 024	UKA 024
Central processing unit	ALU 150	ALU 150

The STA 503 has 13 free **PEAB slots** and 3 free **PMB slots**; the STA 553 has 10 free PEAB slots only due to the wider power supply. The PEAB slots can be equipped with I/O modules with rear connection, the PMB slots with memory and interface modules, for example.

 **Note** DNP, UKA and ALU are fixed to their slots. The slots for the PMB and PEAB modules can be freely selected within their structure.

3.1.1.3 Structure of the Controller with the STA 505 / STA 555

 **Note** Expansions with front connections **only** and **not** with rear connection are possible with the STA 505 and STA 555 standard equipment.

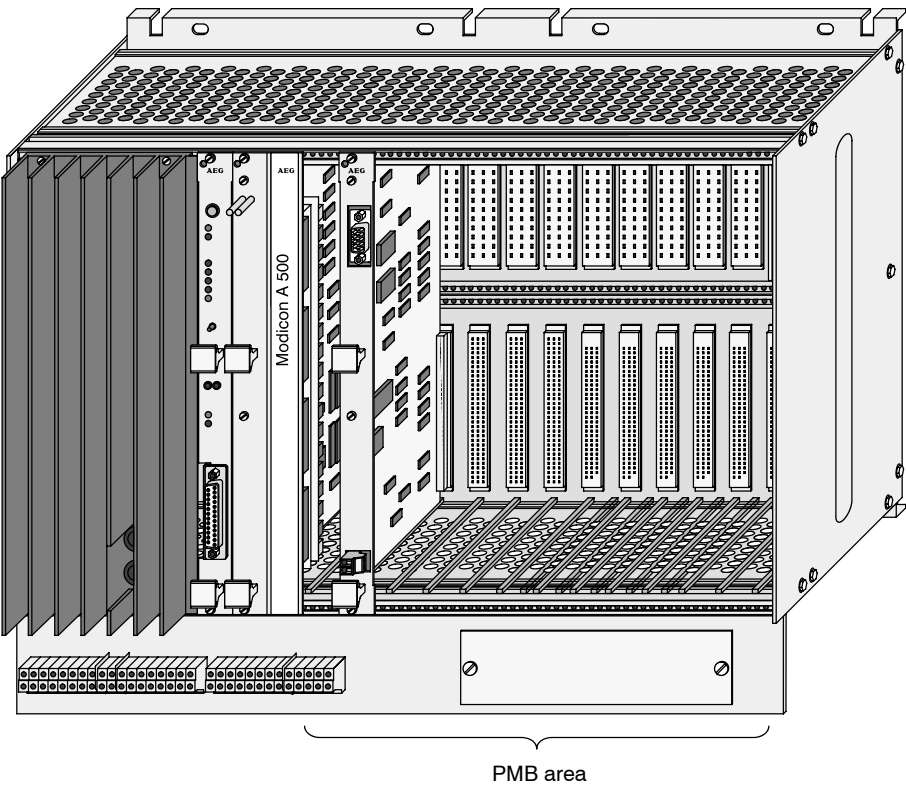



Figure 11 STA 505 Standard Equipment

The STA 505 and STA 555 standard equipment is designed for various primary voltages (24 VDC for STA 505 or 230 VAC for STA 555). It is designed with front connection and consists of:


Table 14 Equipping the STA 505 and STA 555 Standard Equipment

	STA 505	STA 555
Subrack	DTA 107	DTA 107
Power supply	DNP 023-1 (24 VDC, primary)	DNP 023 (230 VAC, primary)
Monitoring module	UKA 024	UKA 024
Central processing unit	ALU 150	ALU 150
Modnet 1/SFB network	BIK 151	BIK 151

STA 505 and STA 555 have 12 free **PMB slots**. A further PMB slot is equipped with a BIK 151. The free PMB slots can be equipped with memory and interface modules, for example. Free **PEAB slots** are not available.

 **Note** DNP, UKA and ALU are fixed to their slots. The slots for the PMB modules can be freely selected within their structure.

3.1.1.4 Structure of the Controller with the STA 557

 **Note** Expansions with front connection and with rear connection are possible with the STA 557 standard equipment.

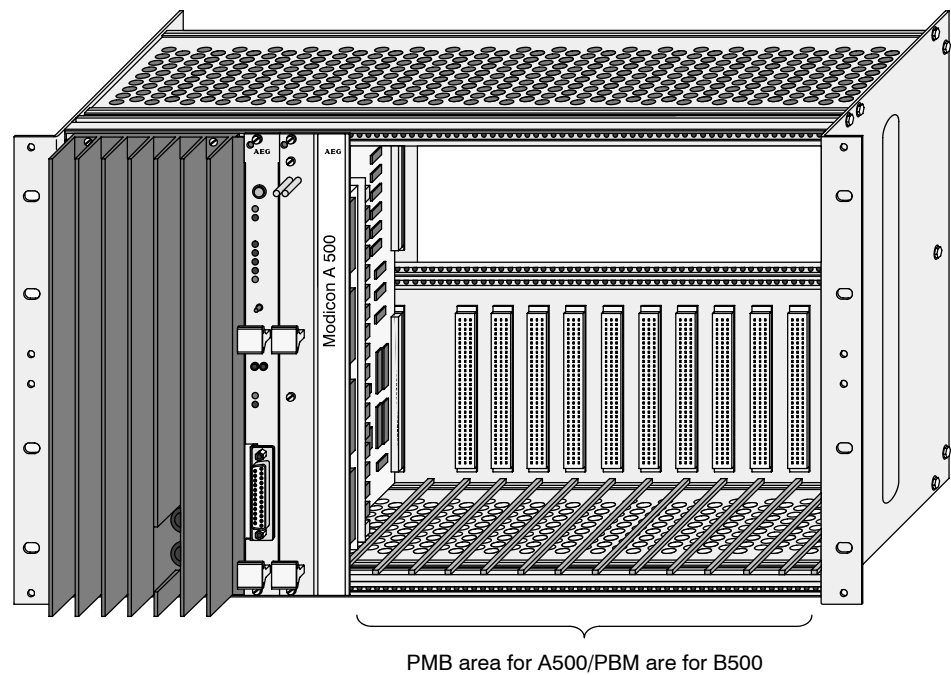



Figure 12 STA 557 Standard Equipment

The STA 557 standard equipment is designed for a primary voltage of 230 VAC. It is designed with rear connection and consists of:

Table 15 Equipping the STA 501 and STA 551 Standard Equipment

STA 557	
Subrack	DTA 27.1
Power supply	DNP 023 (230 VAC, primary)
Monitoring module	UKA 024
Central processing unit	ALU 150

The STA 557 has 13 free **PMB slots**. The slot on the righthand side next to the ALU should be equipped with a memory module. The remaining 12 slots can be divided into 5 ... 12 connecting B500 slots and 0 ... 7 connecting A500 slots accordingly. This division is carried out by the factory and is to be given with the order. The B500 slots can be equipped with B500 modules, the A500 slots with memory and interface modules, for example. Free **PEAB slots** are not available.

 **Note** DNP, UKA and ALU are fixed to their slots. The slots for the PMB modules can be freely selected within their structure.

3.1.2 Structure of the I/O Peripherals

The I/O peripherals consist of a number of I/O modules depending on the task. These modules are combined in subracks and are connected to the controller via **PEAB** or **Modnet 1/SFB**. These modules form the interface to the process, in which each of them processes up to 32 process signals.

The I/O modules designed with front connections are summarized on page 22, those with rear connection on page 23.

3.1.2.1 Structure of the I/O Peripheral with Front Connection

The I/O modules with front connection are connected via the Modnet 1/SFB. The bus interface is an RS interface and is located in the controller on the front of the BIK 151 or BIK 812. An expansion is possible with any primary subrack via the Modnet 1/SFB.

Expansions via **Modnet 1/SFB** (distributed expansions) can be:

- DTA 102 or DTA 112 secondary subrack with max. 4 I/O modules with **front connection** and one DEA as the Modnet 1/SFB network

or

- DTA 103 or DTA 113 secondary subrack with max. 9 I/O modules with **front connection** and one DEA as the Modnet 1/SFB network

or

- the righthand half of the DTA 101 primary subrack with max. 4 I/O modules with **front connection** and one DEA as the Modnet 1/SFB network

or

- DEA-H1 or DEA-K1 compact device with an integrated Modnet 1/SFB network, 24 inputs and 16 outputs as semiconductors (DEA-H1) or as relays (DEA-K1).

The DEA 106, DEA 116 and DEA 156 are seen as DEA modules. Table 16 shows which DEA are suitable for which subrack.

Table 16 Assignment of Subracks and Suitable Modnet 1/SFB Networks (DEA 1x6)

Equipment	Suitable DEA	Suitable Subrack	Configuration Notes
binary and analogue I/O only	DEA 106	DTA 102, DTA 103, DTA 112, DTA 113 DTA 101 (righthand half)	
max. one intelligent function module (e.g., VIP, ...)	DEA 156	DTA 102, DTA 103, DTA 112, DTA 113 DTA 101 (righthand half)	VIP 101 has to be inserted on the right next to the DEA
several intelligent function modules	DEA 116	DTA 112, DTA 113	max. 3 VIP 101 possible, if the slot between two VIP 101 or between a VIP and the DEA is not used or used for a standard I/O module.



Warning Never insert a DEA 116 in a DTA 101, DTA 102 or DTA 103!

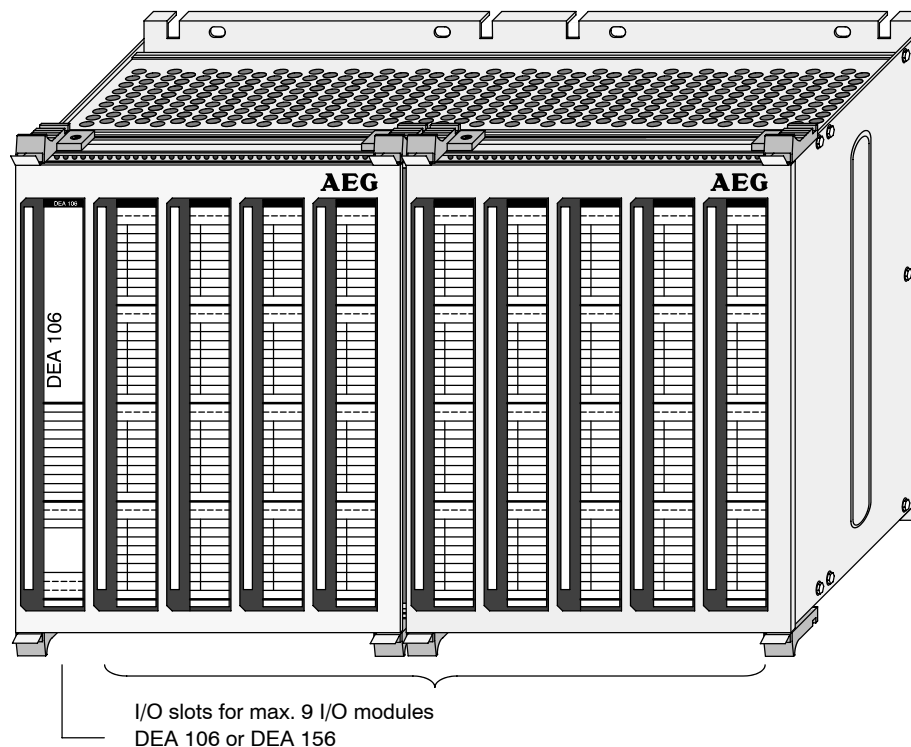


Figure 13 DTA 103 Secondary Subrack

The DEA 1xx is fixed to its slot (extreme left). The I/O modules can be inserted in any combination on the I/O slots.

The communication between the controller and the individual expansions is carried out via a twisted JE-LiYCY cable, which is to be laid from the BIK 151 or BIK 812 bus interface (slot in the PMB area of the controller) to the DEA 106, DEA 116 or DEA 156 remote I/O interfaces (slot in the secondary subrack) or to the DEA-H1 / DEA-K1 compact devices.

Each BIK can drive several DEAs. If one DEA is connected only and if the distance to be bridged is too short, the YDL 40 cable (cable length: 40 cm) can be used for the connection from BIK and DEA. The cable is to be assembled by the user himself for larger distances or for the case when one BIK should drive several DEA modules. The RS 485 connector and the twisted JE-LiYCY cable (in meters) can be received here as accessories. A detailed set of installation instructions is enclosed with the RS 485 connector (BBS 1).

Figure 14 shows the connection of the secondary subracks to the controller. The DEA-H1 and DEA-K1 compact devices are treated here as secondary subracks equipped with a DEA 1xx.

A maximum of three Modnet 1/SFB networks (BIK 151 or BIK 812) are permitted, each of which can drive up to 16 DEA modules. The Modnet 1/SFB can be expanded up to 159 I/O slots. Since the upper limit of the total number of permitted I/O slots is also reached in this case, no PEAB nodes can be operated here.



Note The limits for the I/O expansion are given in section 3.1.3.

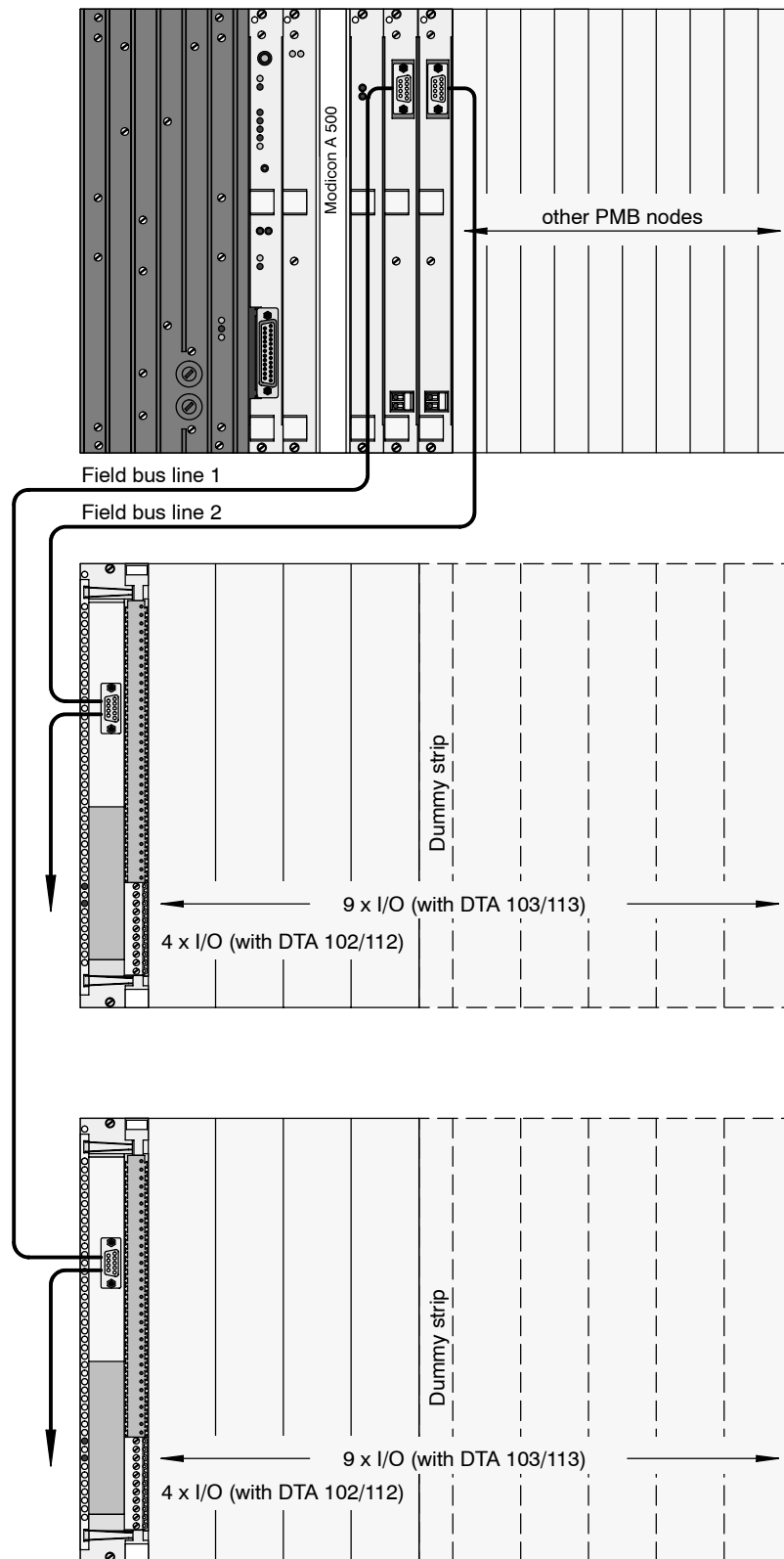


Figure 14 Expansion of an A500 with a DTA 107 Primary Subrack via Modnet 1/SFB

The unequipped PMB slots in the controller can be equipped with other PMB nodes bearing in mind the configuration limits.

3.1.2.2 Structure of the I/O Peripherals with Rear Connection

The I/O modules with rear connection must be connected with the PEAB, the interfaces of which are guided out on the rear of the primary subrack. This is possible if the primary subrack is a DTA 024, DTA 27.1 or DTA 028. An expansion via **PEAB** (central expansion) consists of:

- ❑ DTA 025 secondary subrack with DNP 025 or DNP 026 power supply, DUV 025 connecting printed board, PEAB network DKV 022, PEAB monitoring DKU 022 (optional, cf. 3.5) and max. 16 I/O modules with **rear connection** (see Figure 15). DNP, DUV and DKV are generally not required with the second subrack of a pair.

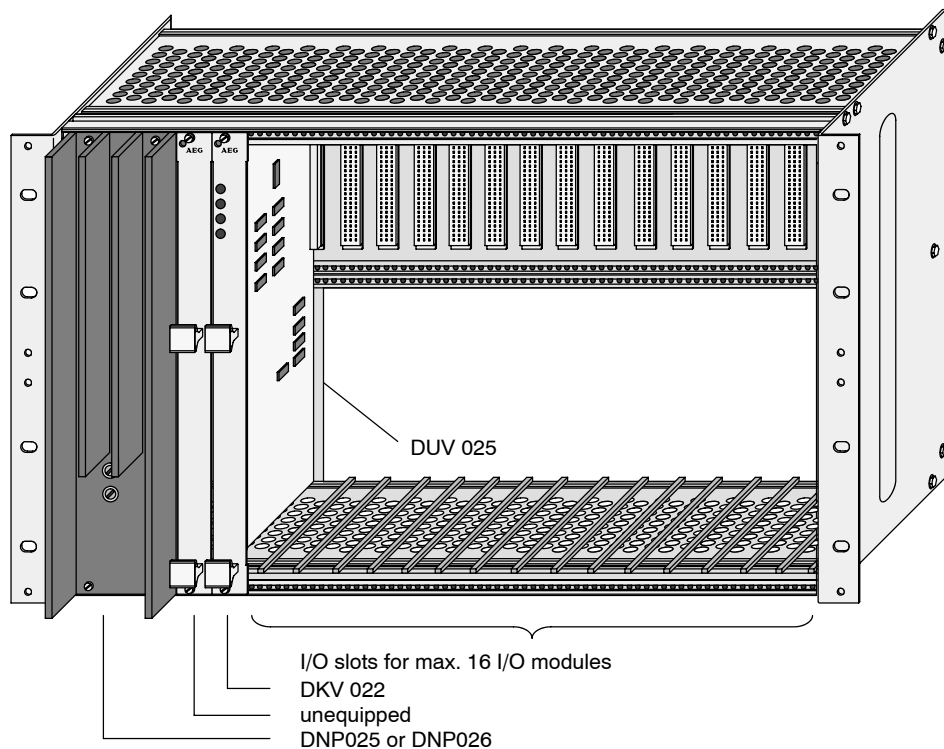


Figure 15 Equipping the DTA 025 Secondary Subrack

The PEAB expansion and the connection of the subracks are carried out in pairs and shown in Figure 16 and Figure 17. The following is to be noted here:

- ❑ DNP, DKU and DKV are fixed to their slots. The I/O modules can be inserted on the I/O slots in any combination.
- ❑ The controller must be equipped with a DKV 023 with more than one DTA025.
- ❑ Power supplies are necessary in the secondary subracks if the summated current of the used modules is larger than the power made available by the preceding power supply. Each of the 1st subracks of a pair is equipped with a power supply in the following two figures.
- ❑ Each first DTA 025 of a secondary **pair** must be equipped with a DUV 025 connected printed board and a DKV 022. A maximum of 4 secondary pairs are permitted.
- ❑ Each subrack which has a DKV 022 and/or a power supply must be equipped with a DUV 025.

PEAB Expansion of an A500 with a DTA 024 / DTA 028 Primary Subrack

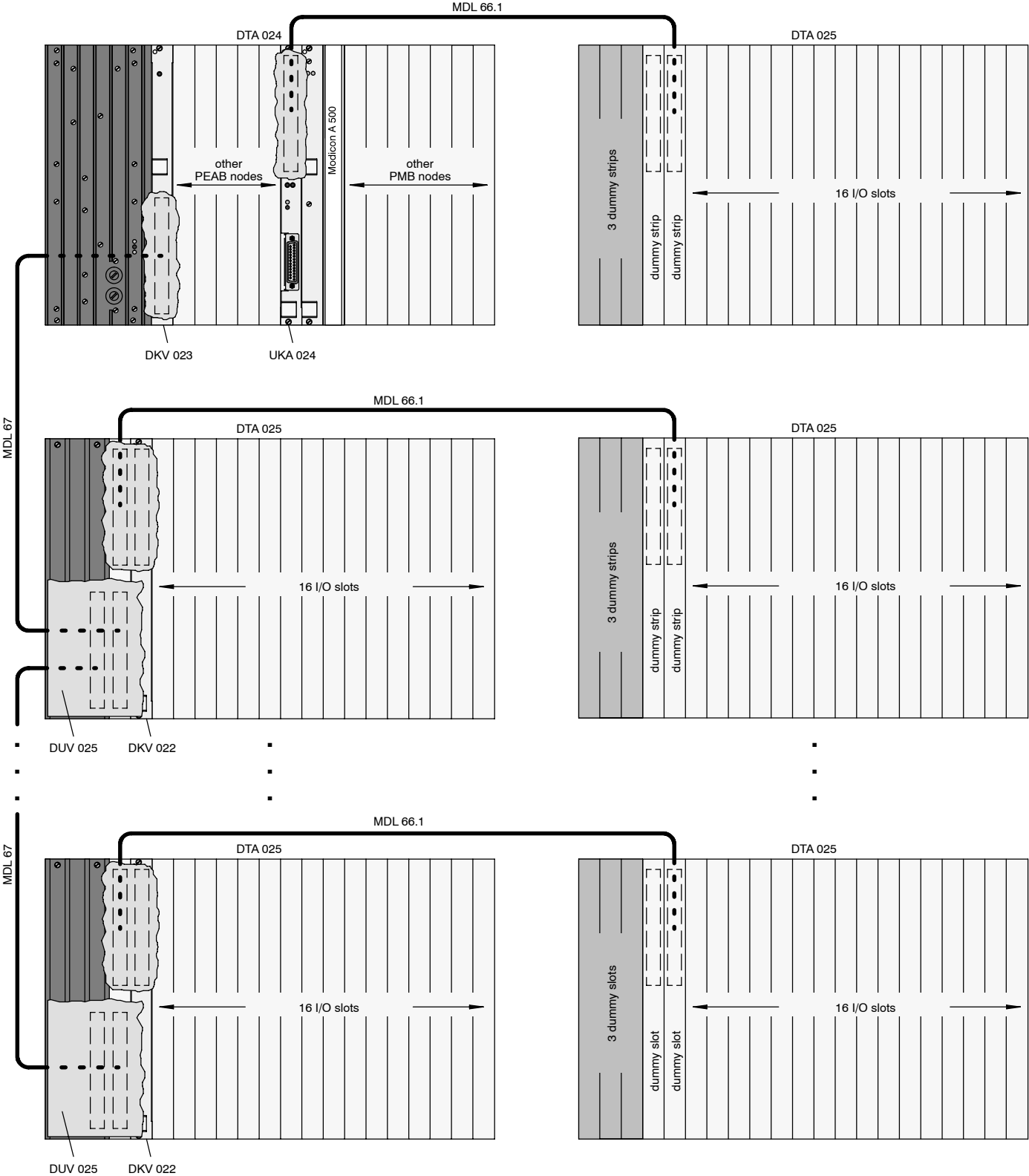


Figure 16 Expansion of an A500 with a DTA 024 Primary Subrack via PEAB

The connectors of the cables are located on the rear of the subracks.

PEAB Extension of an A500 with a DTA 27.1 as a Primary Subrack

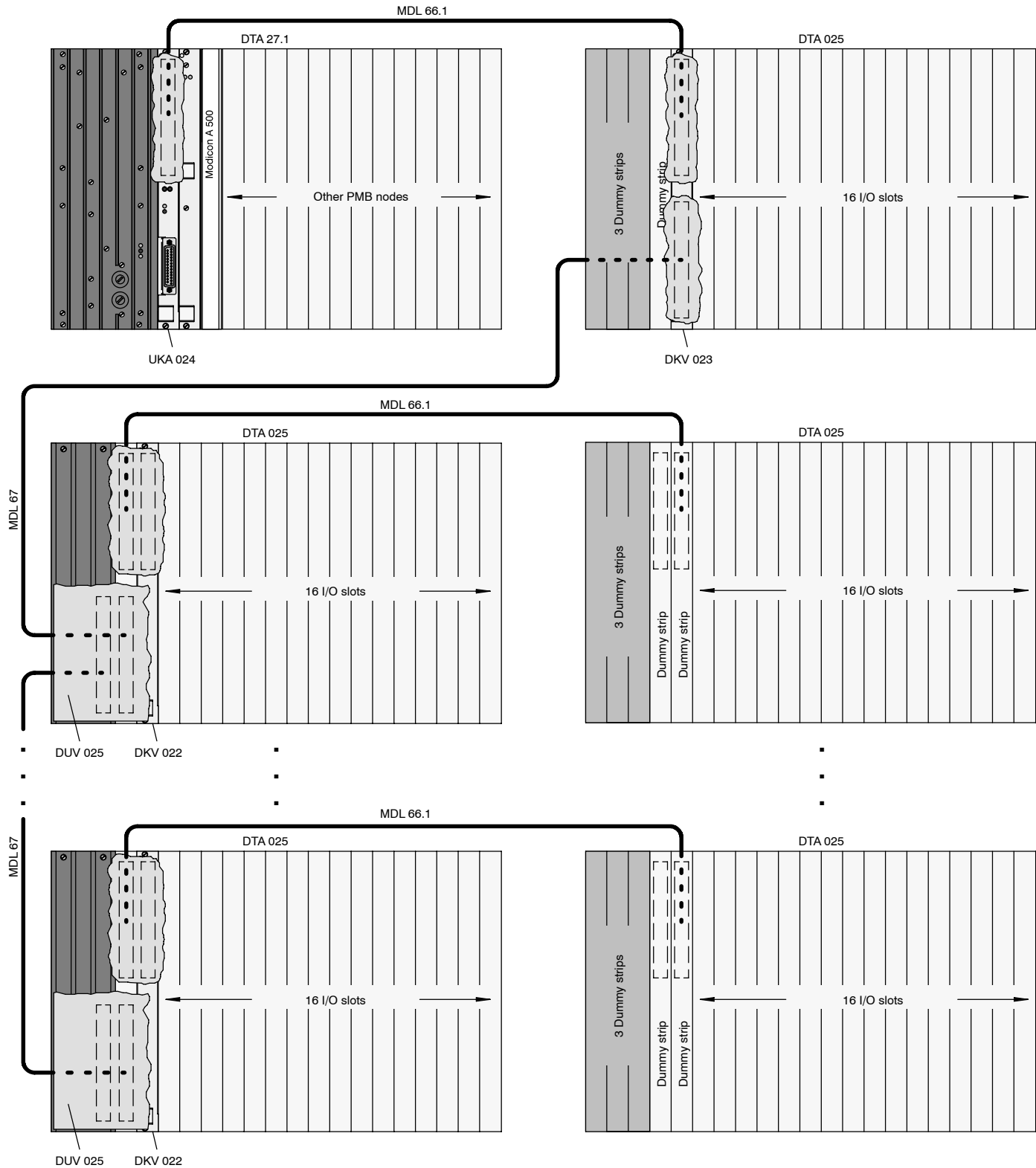


Figure 17 Expansion of an A500 with a DTA 27.1 Primary Subrack via PEAB

The connectors of the cables are located on the rear of the subracks.

3.1.2.3 Mixed Structure

The secondary subracks can be accommodated together with the primary subracks in a switch cabinet (central structure). This is the only possibility due to the cable length of the MDL 66.1 (70 cm) when using I/O modules via PEAB. Extending this cable would endanger a perfect data transfer and may therefore not be done in any circumstances.

The spatial structure of the system can be more variable when using the Modnet 1/SFB I/O. It is possible here to position individual secondary subracks away from the controllers near the process (decentral structure) so that long cables between the process and I/O modules can be shortened considerably. However, the Modnet 1/SFB cable may not be longer than 1200 m here. The baudrate varies depending on the cable length from 2 mbaud with max. 30 m to 62.5 kbaud with 1200 m.

The following configuration example represents a mixed structure of a system consisting of PEAB and Modnet 1/SFB I/O.

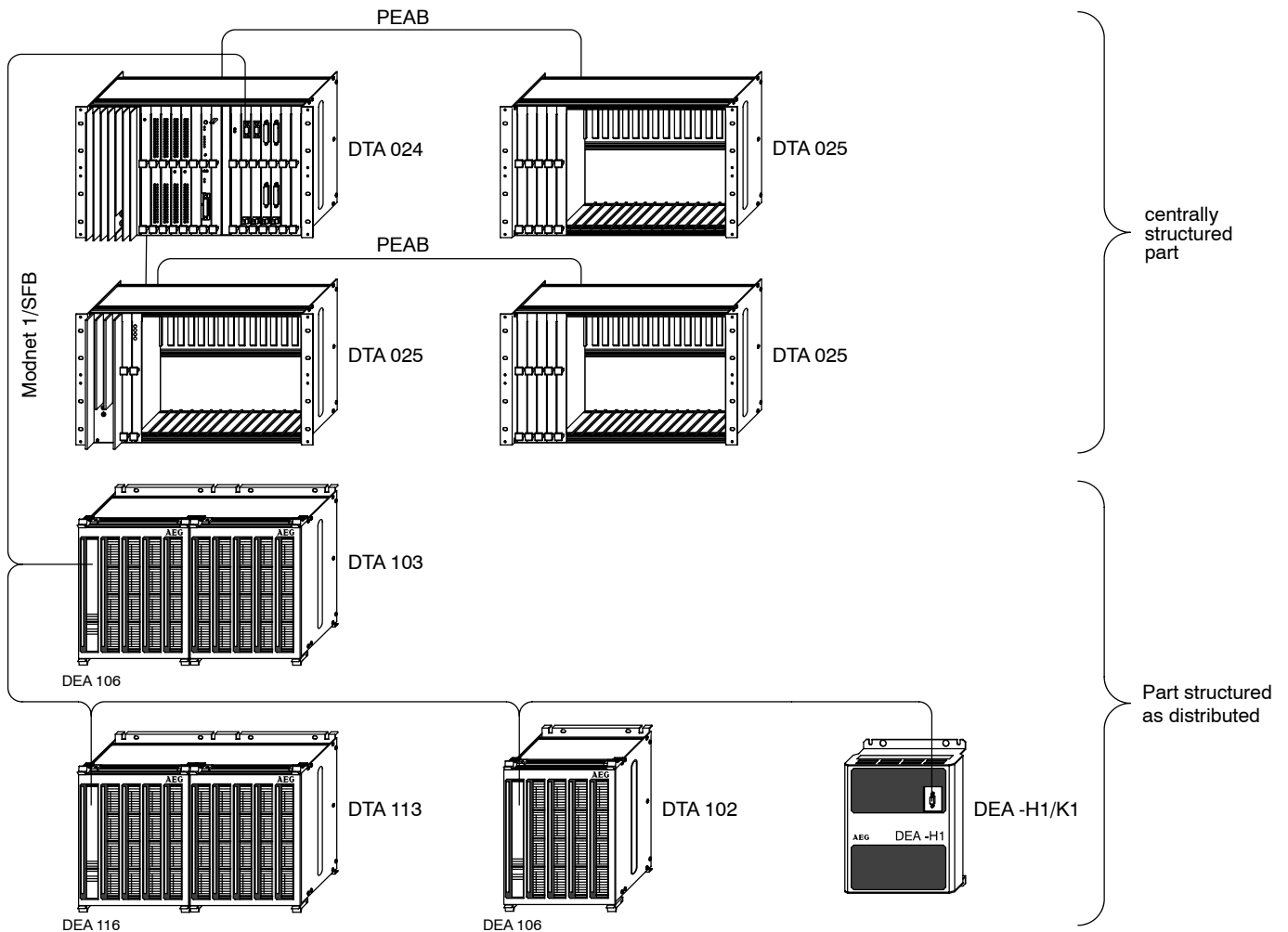


Figure 18 Expansion of an A500 with Modules with Front and Rear Connection

3.1.3 Configuration Limits (Maximum Expansion)

The following configuration limits are valid for the A500:

- distributed expansions (Modnet 1/SFB) for each programmable controller
 - BIK 151 / BIK 812 for I/O for each programmable controller 3
 - distributed expansions (DEA ...) for each BIK 151 / BIK 812 16
 - distributed expansions (Modnet 1/SFB) for each A500 $48 = 3 \times 16$
- central expansions (PEAB) for each A500 and each programmable controller
 - controller set up with DTA 024 or DTA 028 9
 - controller set up with DTA 27.1 9
- expansions (Modnet 1/SFB **and** PEAB) for each programmable controller
 - controller set up with DTA 024 or DTA 028 $48 + 9$
 - controller set up with DTA 27.1 $48 + 9$
 - controller set up with DTA 101 or DTA 107 $48 + 0$

The maximum numbers for the I/O slots and for the I/O points cannot be derived. The following limits are valid for these:

Table 17 Configuration Limits of the A500

Configuration	I/O Slots	Binary I/O Points (max.) ⁹⁾
DTA 024 primary subrack	6 ¹⁰⁾	192
DTA 027.1 primary subrack	-	-
DTA 028 primary subrack with DNP 028	10 ¹⁰⁾	320
DTA 028 primary subrack with DNO 028	13 ¹⁰⁾	416
DTA 101 primary subrack	4	128
DTA 025 secondary subrack	16	512
DTA 102/DTA 112 secondary subrack	4	128
DTA 103/DTA 113 secondary subrack	9	288
DTA 024 with max. I/O configuration via PEAB	$149 = 9 \times 16 + (6 - 1)$	4768
DTA 27.1 with max. I/O configuration via PEAB	$142 = 8 \times 16 + 14$	4544
DTA 028 with DNP 028 and max. I/O configuration via PEAB	$153 = 9 \times 16 + (10 - 1)$	4896
DTA 028 with DNO 028 and max. I/O configuration via PEAB	$156 = 9 \times 16 + (13 - 1)$	4992
max. I/O configuration via Modnet 1/SFB	159 ¹¹⁾	5088
max. I/O configuration via PEAB and Modnet 1/SFB	159	5088



Note The configuration for the maximum values resulting purely theoretically are not obtained in practice by using intelligent function modules and analogue I/O modules.

9) A basis of I/O modules with 32 I/O points is used. The given maximum value is reduced accordingly if modules with fewer I/O points are used (analogue I/O, relay outputs, ...).

10) If PEAB expansions are configured, an I/O slot must be reserved in the primary subrack for the DKV 023.

11) Each DEA-H1 and each DEA-K1 "uses" 2 I/O slots!

We Recommend you to Execute the Necessary Activities in the Following Order:

- ❑ Establishing the I/O Equipment (cf. 3.1.4)
- ❑ Establishing the Slot References (cf. 3.1.5)
- ❑ Assigning the Signal Addresses to the Signals (addressing, cf. 3.1.6)
- ❑ Planning and Structure of the Circuits (cfl. 3.2, chapter 5)
- ❑ Executing the Peripheral Ports (cf. 3.2, chapter 5)
- ❑ Switching Off Mode of the Binary Output, e.g., if there is Undervoltage or Excess Temperature of the Supplying Power Supply (see section 3.3)
- ❑ Synchronization of the Power Supplies (for Rear Connection only, cf. section 3.4)
- ❑ PEAB Monitoring Yes/No (cf. 3.5)
- ❑ Determining and Setting the Start-Up Characteristics (cf. 3.6)
- ❑ Settings for the Modules (cf. 3.7.1)
- ❑ Installing and Equipping the Subracks (cf. 3.7.2)
- ❑ Earth Grounding and Earthing Measures (cf. section 3.7.3)
- ❑ Entering the Equipment in the Equipment List (cf. 3.10.1)
- ❑ Initial Start-Up (cf. 3.9)
- ❑ Documentation and Archiving (cf. 3.11)

3.1.4 Specifying the I/O Equipment

It must be specified during the configuration which I/O modules are inserted where. Generally any I/O module can be inserted on any I/O slot so that the equipments can be carried out almost exclusively for the specific task. If there are any limits as far as this is concerned, they are mentioned in the module descriptions of the affected modules. Omitting individual I/O slots is permitted.

3.1.5 Specifying the Slot References

A slot reference between 2 and 160 is assigned to each I/O slot.



Caution If 1N logs (networking) and I/O logs are to be run via a BIK, the slave addresses and the slot references must be different.

3.1.5.1 Specifying the Slot References with Front Connection

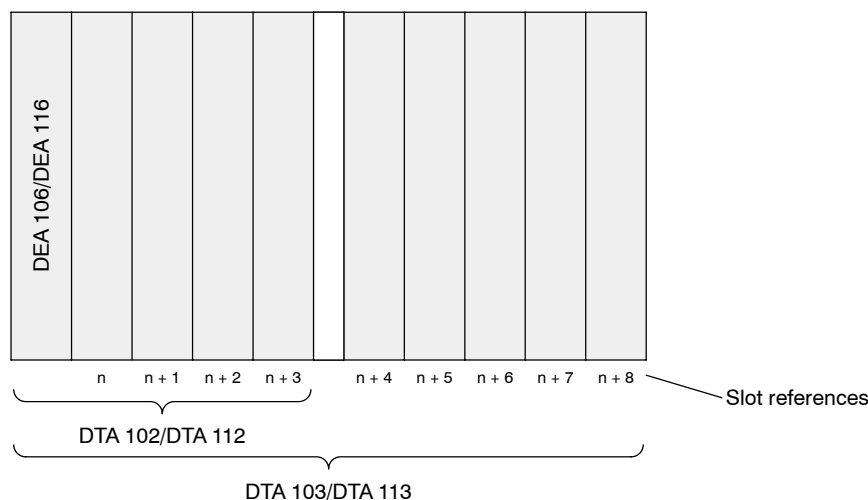


Figure 19 Specifying the Slot References in Subracks with Front Connections

Proceed subrack by subrack. The address n is assigned to the first I/O slot of a subrack. The addresses of the following 3 (DTA 102/DTA112) or 8 (DTA 103/DTA113) I/O slots are thus specified (cf. Figure 19). The first I/O slot in the following subrack then receives a number starting from $n+4$ or $n+9$, etc., until all the subracks are taken into consideration.

The slot reference n of the first **I/O slot** of a subrack is to be set to the DEA 1x6 by means of plug-in jumpers (see module description). The slot, on which the DEA is inserted, does **not** receive a slot reference.

3.1.5.2 Specifying the Slot References with Rear Connection

The subracks are to be seen as pairs for the addressing. The first subrack pair consists of the primary subrack and the 1st secondary subrack; the second pair consists of the 2nd and 3rd secondary subrack, etc.

The slot references are now specified by counting the PEAB slots within the subrack from **right to left**. 16 addresses are reserved for each subrack independently of whether they can be used or not.

Start with the primary subrack. The 1st PEAB slot on the left-hand side next to the UKA receives the slot reference 2, the next one 3, etc., until all the I/O slots of the subrack are addressed (cf. Figure 20). Continue counting with 17, 18 ... 32 in the 1st secondary subrack independently of the highest slot reference given in the primary subrack. The subaddresses of this DTA 025 must be set to 0 and 1 using jumpers (see DTA 025 module description).

If the controller is set up in the DTA 27.1, the counting starts in the 1st secondary subrack. The subaddresses of 0 and 1 are to be set there accordingly so that the slot references of 1 ... 16 are assigned to the PEAB slots (from right to left).

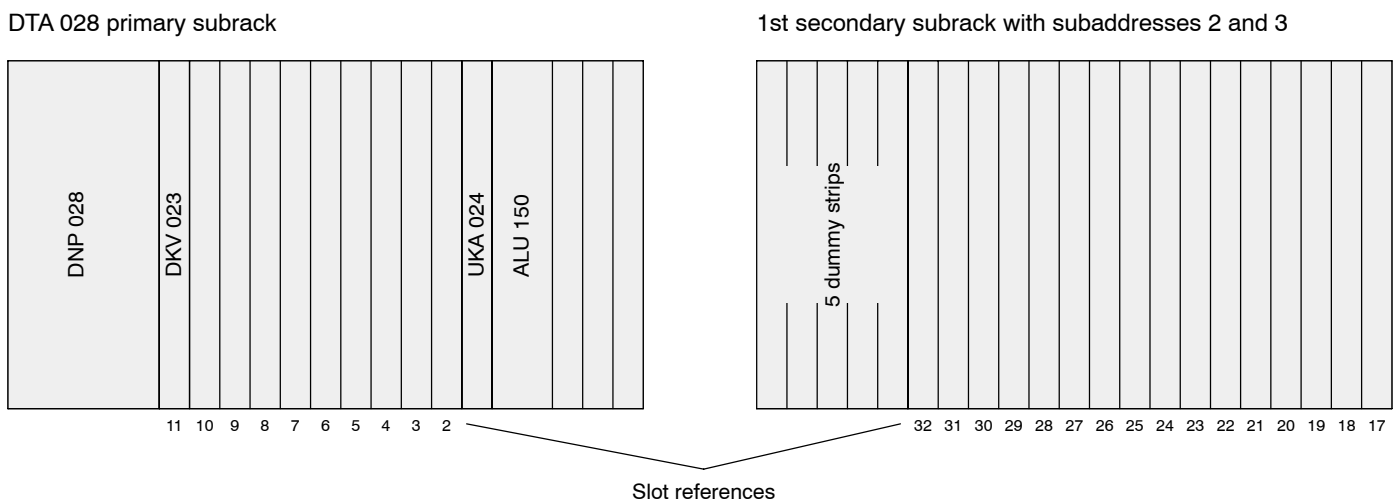


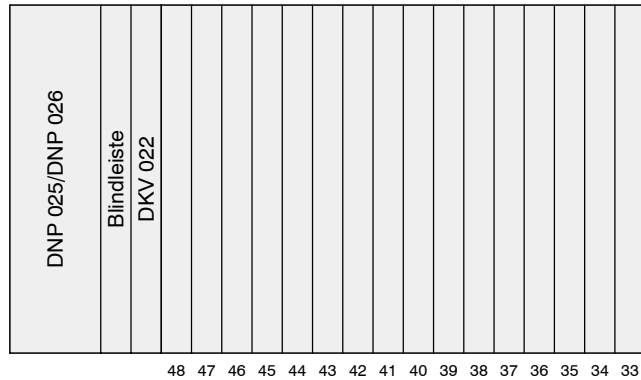
Figure 20 Specifying the Slot References in the 1st Subrack Pair (DTA 024 or 028 Primary Subrack)

Continue counting with 33, 34 ... 48 and with 49 ... 64 in the following subrack pair (cf. Figure 21). The address jumpers of A and B must be jumpered to 1 on the DKV 022 ($\hat{=}$ offset of 32, see the DKV 022 module description). The subaddresses of 0 and 1 are to also to be set on the 1st subrack of the pair, the subaddresses of 2 and 3 on the 2nd subrack of the pair.



Caution The slot references of 1 and 16 may not be used with rear connection since they are reserved for the UKA.

2nd secondary subrack with the subaddresses of 0 and 1



3rd secondary subrack with the subaddresses of 2 and 3

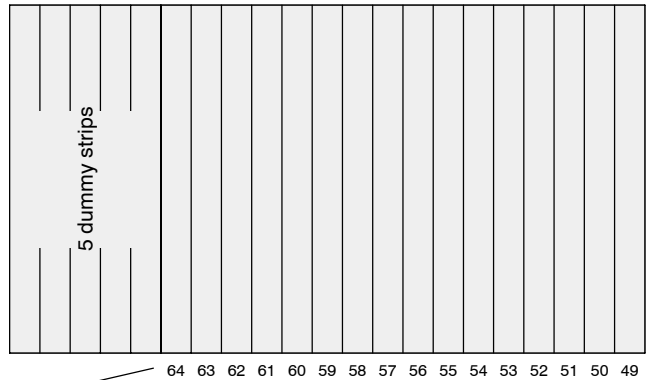


Figure 21 Specifying the Slot References in the 2nd Subrack Pair

The corresponding is true for the following pairs. The address jumpers of A and B of the affected DKV 022 are to be set to the address of 2, 3 or 4 (see Table 18). The following is therefore also generally valid:

- ❑ 32 addresses are reserved for each subrack pair. A corresponding offset in stages of 32 is caused by the DKV 022 which is inserted in each 1st subrack of a pair so that the address bus does not begin to count from 1 all over again (offset 32 for 1st DKV, offset 64 for 2nd DKV, ...).
- ❑ 16 addresses are reserved for each subrack. An offset of 16 is caused by the subaddresses of 2 and 3 which are to be set in each 2nd subrack of a pair so that the address bus does not always assign the same addresses to both subracks of a pair. The subaddresses of 0 and 1 do not cause an offset and are to be set in each 1st subrack of a pair. Exception: Primary subrack; the setting is carried out here by the factory.

Table 18 Specifying the Slot References with Rear Connection

Addresses	Address Jumpers on DKV 022	Subaddress on DTA 025
1 ... 16	not required	not required
17 ... 32	not required	Set to 2 and 3
33 ... 48	Setting as 1st DKV	Set to 0 and 1
59 ... 64	not required	Set to 2 and 3
65 ... 80	Setting as 2nd DKV	Set to 0 and 1
81 ... 96	not required	Set to 2 and 3
97 ... 112	Setting as 3rd DKV	Set to 0 and 1
113 ... 128	not required	Set to 2 and 3
129 ... 144	Setting as 4th DKV	Set to 0 and 1
145 ... 160	not required	Set to 2 and 3

3.1.5.3 Example for a Mixed Structure (Front and Rear Connection)

The following are to be connected:

- ❑ with rear connection: 4 SES 002 (breadth: 4T), 2 POS 011 (breadth: 8T)
- ❑ with front connection: 2 DAP 102, 1 DEP 112

Figure 22 shows an equipment possibility of the A500 with the DTA 028 and DTA 102 subracks, Table 19 a possible referencing.

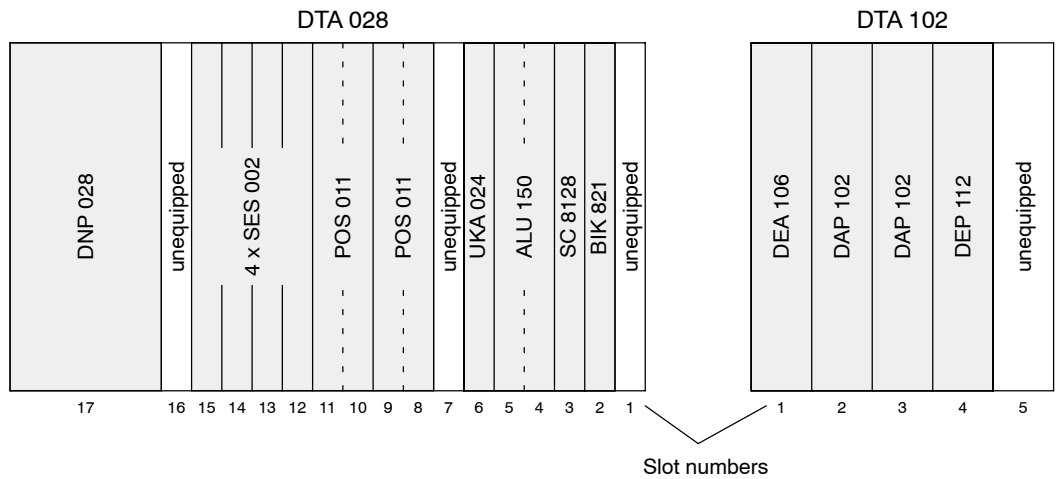


Figure 22 Equipment Example of an A500

Table 19 Equipment Example of an A500 with Modules with Front and Rear Connection

Module	Subrack	Slot	Slot Reference
1st POS 011	DTA 028	8 and 9	4
2nd POS 011	DTA 028	10 and 11	6
1st SES 002	DTA 028	12	7
2nd SES 002	DTA 028	13	8
3rd SES 002	DTA 028	14	9
4th SES 002	DTA 028	15	10
1st DAP 102	DTA 102	2	13
2nd DAP 102	DTA 102	3	14
1st DEP 112	DTA 102	4	15

The address of 13 is to be set on the DEA 106.



Caution Slot references may not be equipped twice at all with a mixed structure (front and rear connection).

3.1.6 Assignment of the Signal Addresses to the Signals (Addressing)

An address (signal address) must be assigned to each terminal so that the processor can assign the I/O signals of the signal memory to the terminals of the I/O modules. For **analogue I/O modules** this is carried out via the software blocks, with which the relevant modules are linked into the user program and is documented in these blocks. The following explanations are therefore only valid for **binary I/O modules**.

The addressing according to DIN, the symbolic addressing and an addressing specific to AEG are available as types of addressing independently of the selected method of programming (cf. Table 20).

Table 20 Types of Addressing

Programming in	AEG Addressing	DIN-Addressing	Symbolic Addressing
Dolog AKF	possible	possible	possible
Dolog B offline	possible	possible	possible
Dolog B online	possible	not possible	not possible

3.1.6.1 Addressing According to DIN

A DIN address consists of the following:

Slot reference + port number. The slot reference and port number are separated from each other by a point.

Example: 4.6 → slot reference 4, port no. 06
5.28 → slot reference 5, port no. 28

The following is generally valid:

- A **slot reference** is assigned to each slot. The assignment must be carried out during the configuration of the hardware and is described in section 3.1.5.
- The **port number** results by counting the terminals for the I/O signals from the top to bottom for the modules with front connection (cf. Figure 23, left-hand half).

Figure 24 shows the assignment of the port numbers to the ports for the I/O modules with rear connection.

Example of a Logic Operation with DIN Addressing

An AND block (Dolog block) should link the entries of input 1 and input 2 of a DEP 112 (slot reference 5) to each other and output the result to output 16 of a DAP 106 (slot reference 6).

```
AND
I    5.1
I    5.2
O    6.16
END
```

The letters of “I” for input and “O” for output are parameters of the “AND” block and are automatically offered when the block is called.

The following example shows the addressing of a DEP 112 and a DAP 106 in the DIN (left-hand half) and the AEG addressing (right-hand half). The slot reference of 6 is assumed for the DAP 106, the slot reference of 5 for the DEP 112.



Note The DAP 102 and DAP 103 modules are to be addressed like a DEP 112.

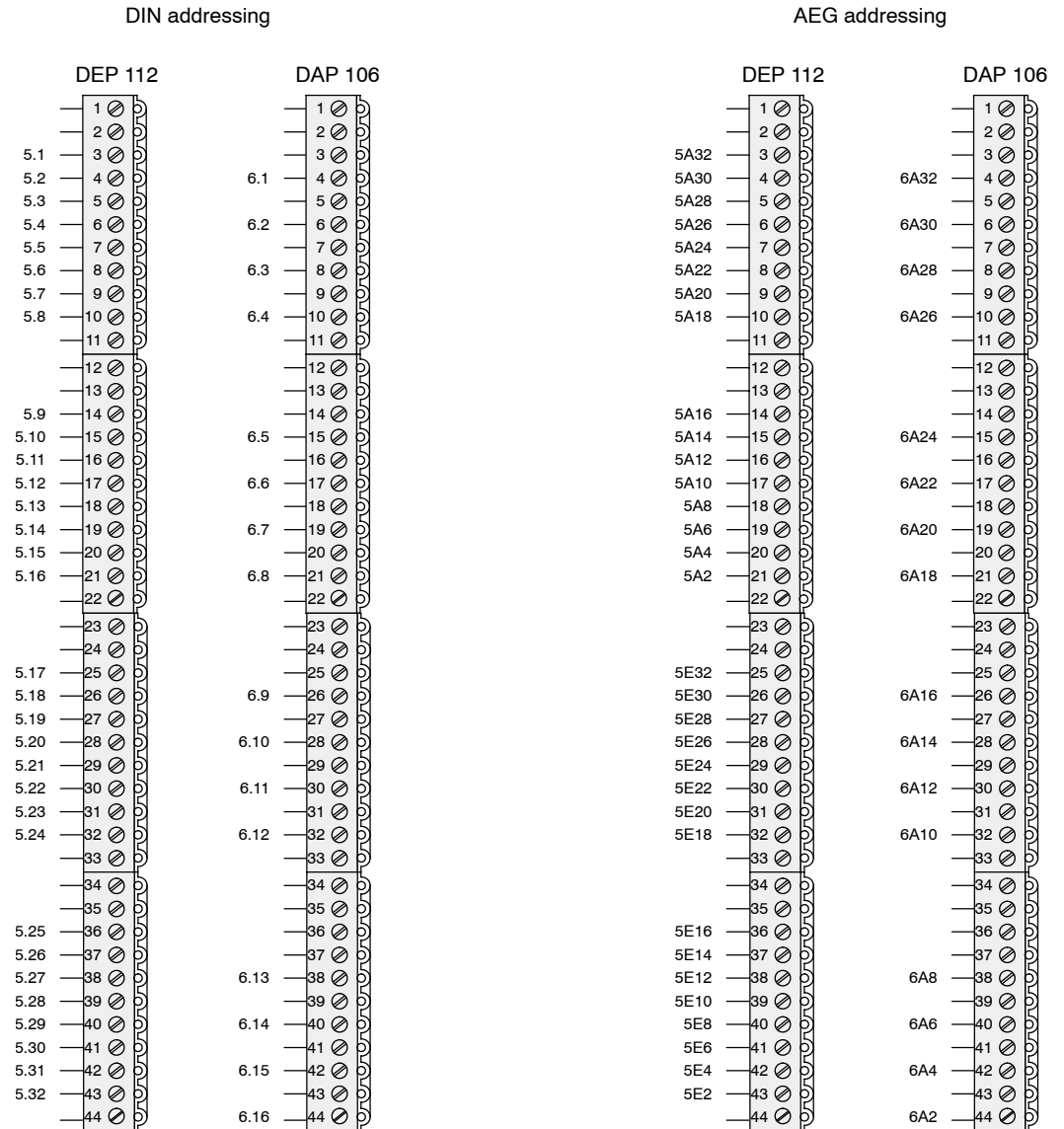


Figure 23 Addressing Example for a DEP 112 and a DAP 106 (DIN and AEG Addressing)

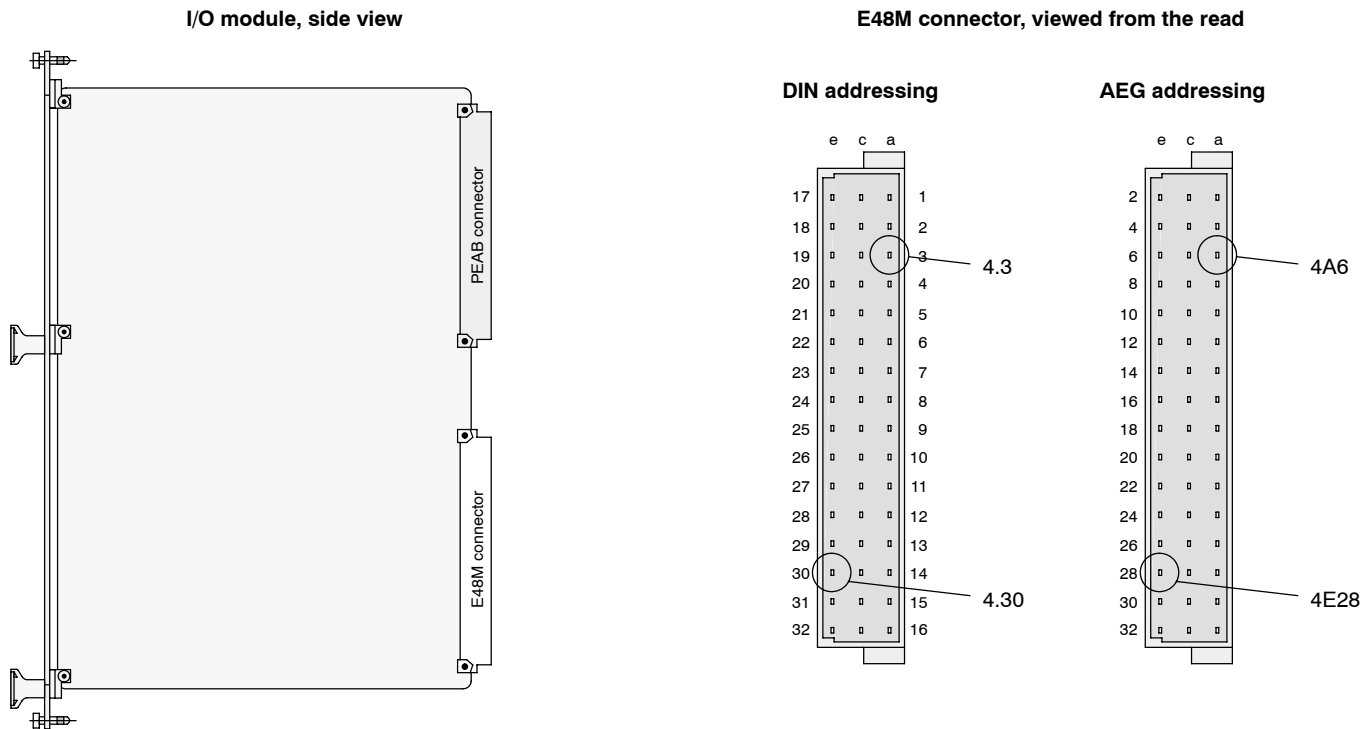


Figure 24 Left: Position of the E48M Connector; Center: DIN Addressing of the Ports; Right: AEG Addressing of the Ports

3.1.6.2 AEG Addressing

The signal address consists of:
Slot reference + port column + port no.

Example: 4A6 → slot reference 4, port column a, port no. 06
 5E28 → slot reference 5, port column e, port no. 28

The following is generally valid:

- ❑ A **slot reference** is assigned to each slot. The assignment must be carried out during the configuration of the hardware and is described in section 3.1.5.
- ❑ The assignment of the **port column** and the **port number** to the terminals depends in the I/O modules with front connection and is documented in the module descriptions. Figure 23 shows a DEP 112 on slot reference 5 and a DAP 106 on slot reference 6 as an addressing example for the I/O modules with front connection.

Figure 24 shows an example for modules with rear connection (right-hand example). The right-hand port column (seen from the rear) is the port column a, the left-hand one the port column e. Both columns can be inputs and outputs depending on the I/O module used. The ports are numbered in stages of 2 from 2 to 32. The ports designated in Figure 24 are to be addressed with 4A6 pr 4E28, for example, if the module is inserted on the slot with slot reference 4.

Example of a Logic Operation with AEG Addressing

An AND block (Dolog block) is to link the two upper inputs of the DEP 112 from Figure 23 to each other and output the result to the lowest output of the DAP 106 .

```
AND
I    5A32
I    5A30
O    6A2
END
```

The letters of “I” for input and “O” for output are parameters of the “AND” block and are offered automatically when the block is called.

3.1.6.3 Symbolic Addressing

It is possible to assign a symbolic name (motor 1, switch 2, ...) to process signals (or markers, words, ...) with the offline programming (Dolog B or Dolog AKF). A table is generated internally which assigns the hardware addresses to the symbolic names when the user program is compiled. More details are made in the documentation enclosed with the software package.

Example of a Logic Operation with Symbolic Addresses

```
AND
I    enable1
I    switch2
O    motor1
END
```

3.2 Structure of the Power Supplies

Non-stabilized, rectified voltages or three-phase bridges without filtering are sufficient as power supplies for the 24 VDC supply of the A500 modules, sensors and contact elements.

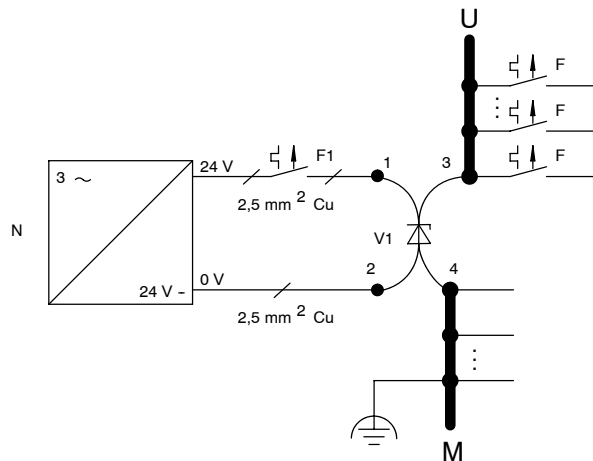
Suppressor diodes are to be used for each supplied or separately fused supply voltage in order to suppress inadmissible voltage peaks which can reach the DC supply via the power supply through

- capacitive external voltage connection or
- switching off inductivities, e.g., transformers, automatic circuit breakers, etc.

The suppressor diodes, e.g. OVP 001 (for top hat rail mounting) or OVP 2480 (for screwing down) overvoltage protection, are to be wired as four pole and arranged near to the power supply with a reference conductor with low impedance.

Each branch must be fused and is to be wired with a suppressor diode if the lines are long, e.g., 1N5646A, AEG E no. 424 152 500 (cf., e.g., V4 in Figure 29). The advantage of this arrangement lies in the fact that a branch can be switched off selectively via the relevant fuse even if the diode shorts. Additional lightning protection precautions are to be taken in environments prone to lightning strikes.

Also note section 5.1.3, "Functional earthing", and section 5.1.4, "Reference conductor system".



- F Automatic circuit breaker or fuse
- F1 10 A or 25 A power protection switch (25 A with OVP 2480 only)
from Messrs. E-T-A Elektronische Apparate GmbH
W-8503 Altdorf bei Nürnberg, Germany,
ordering code: 410-K-2-01-17001, 10 A for top hat rail mounting or
ordering code: 410-K-2-05-17004, 25 A for top hat rail mounting
- N 24 VDC power supply, max. 25 A
- V1 Overvoltage protection: OVP 001 (max. 10 A), AEG E no. 424 244 894
or OVP 2480 (max. 25 A), AEG E no. 424 247 033

Figure 25 Principle Power Supply Structure

Installing the Overvoltage Protection (V1 in Figure 25)

The following is offered from the factory:

- ❑ OVP 001 (Figure 26) for 10 A and top hat rail mounting
- ❑ OVP 2480 (Figure 27) in a cast plastic chassis for 25 A, to be screwed to a level surface

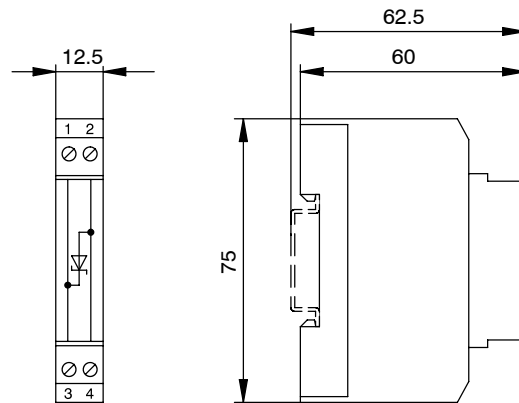


Figure 26 Ports and Dimension Drawing of the OVP 001

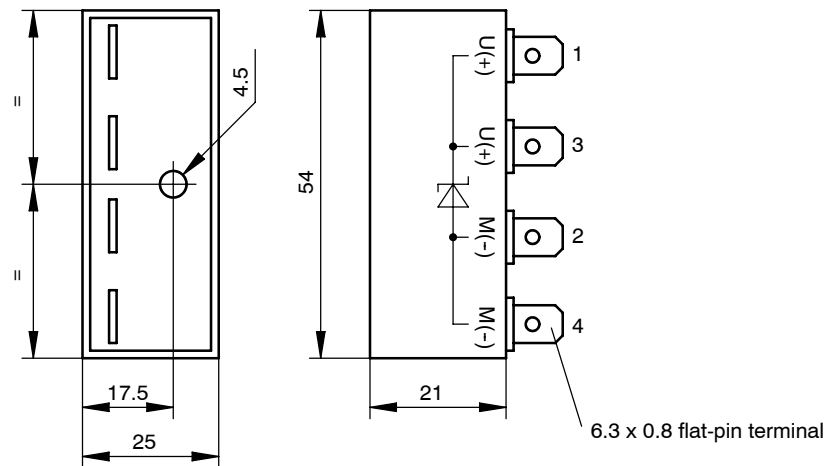


Figure 27 Ports and Dimension Drawing of the OVP 2480

Planning and Division of the Circuits

A distinction is to be made between

- the U_B supply voltage to supply the modules, relay coils and sensors (port figures, page 20ff) and
- the U_S working voltage to control the actuators (port figures, page 27ff).

It is generally recommended to obtain the U_B supply voltage and the U_S working voltage from two different 10 A or 25 A power supplies (known in the following as N1 and N2) so that the supply of the electronics is not affected by interference caused by switching operations. Further power supplies (N3 ...) are to be configured for the working voltage with load currents >25 A.

3.2.1 Supplying the Supply and Working Voltages for I/O Modules with Rear Connection

The internal operating voltage of +12 VDC is guided to the modules via the PEAB (upper printed board in the subracks). The process 24 VDC supply (U_{B24} , M1) is required to process the inputs with some input modules (e.g., DEP 005, DEP 006) and is to be laid to port C28, C30 (E48M connector).

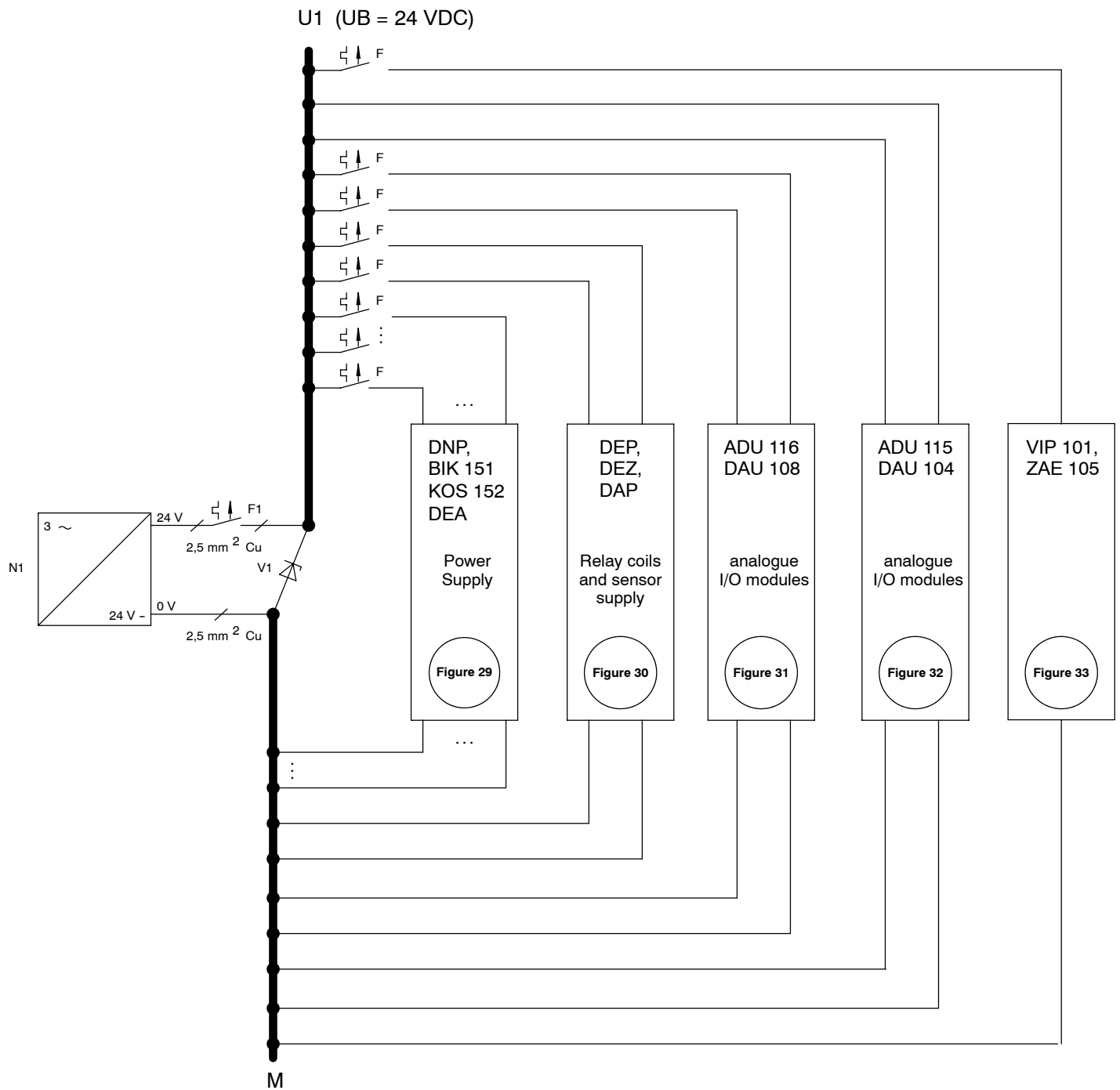
3.2.2 Port Diagram of the U_B Supply (24 VDC for Modules and Sensors) with I/O Modules with Front Connection

A mutual supply circuit with its own power supply is to be configured for the supply of the modules and sensors (inputs).



Note The arrangement shown is valid for lengths of the supply voltage line between the power supply and A500 of approx. 5 m.

Sections 5.2 "EMC measures" and 3.2 "Structure of the power supplies" are to be noted.



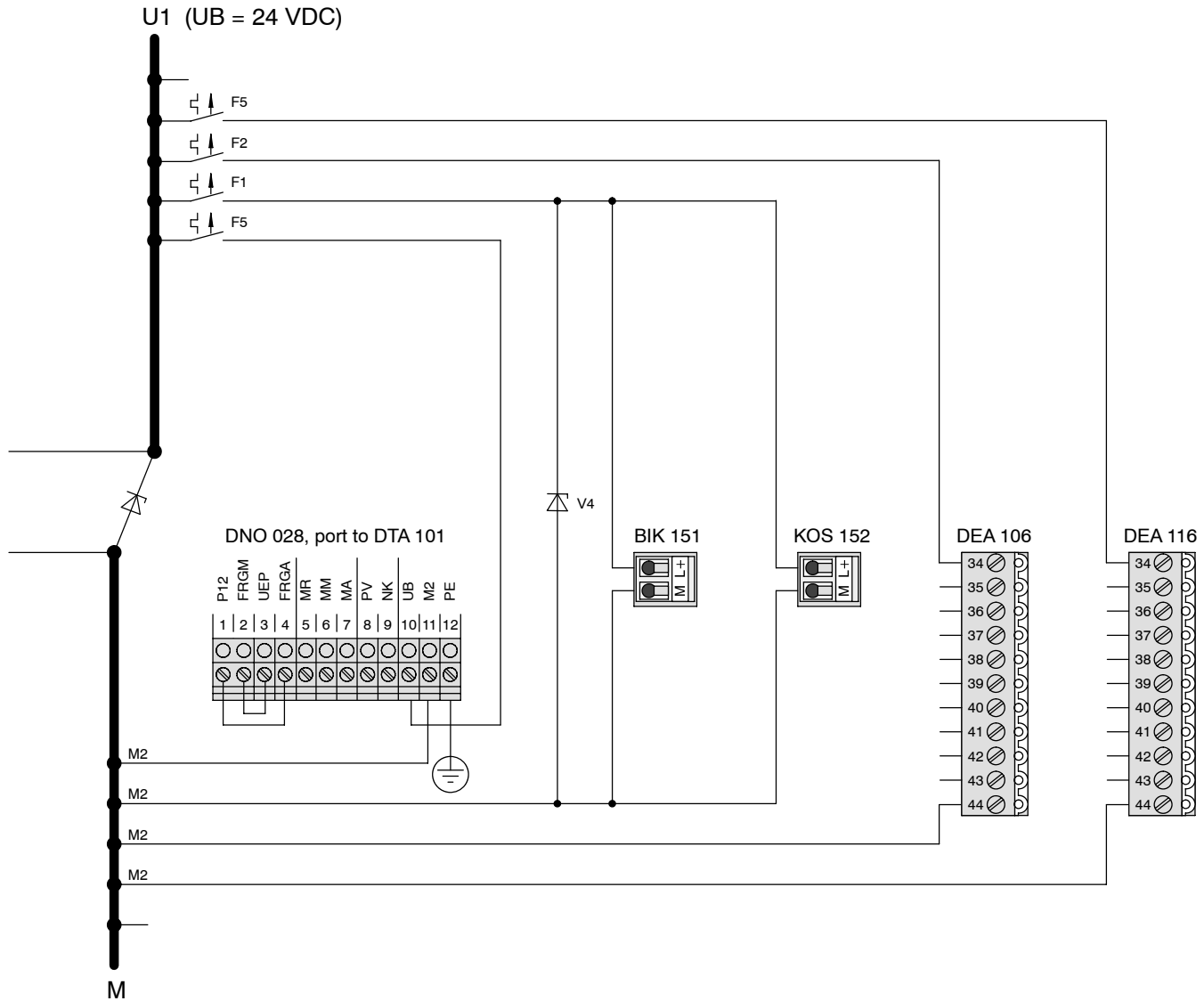
- F Automatic circuit breaker or fuse
 F1 10 A or 25 A power protection switch (see Figure 25)
 N1 Power supply for 24 VDE, max. 25 A
 V1 Overvoltage protection: OVP 001, AUE E no. 424 244 894 or OVP 2480, AEG no. 424 247 033

Figure 28 Port Survey of the UB Supply (24 VDC)



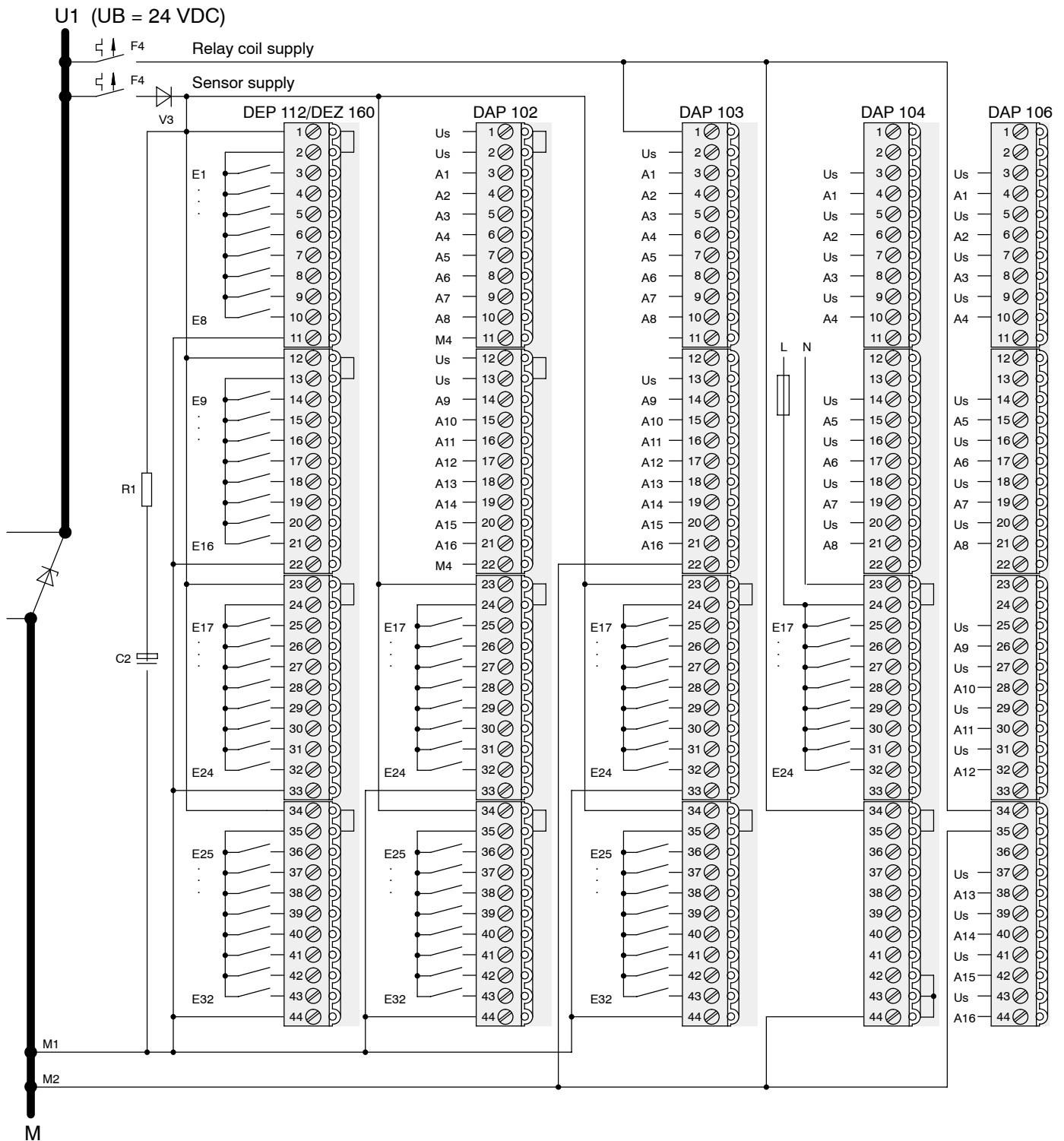
Note Suppressor diodes are integrated in the DEA 106, DEA 116 and DEA 156 as EMC protection.

We recommend you to divide the circuits according to the following detailed port figures:



- F1 Medium time-like 1A fuse
- F2 Max. 2 A automatic circuit breaker or medium time-like 2A fuse
- F5 Medium time-like 5 A fuse
- V4 1N5646A overvoltage protection (suppressor diode), AEG E no. 424 152 500A

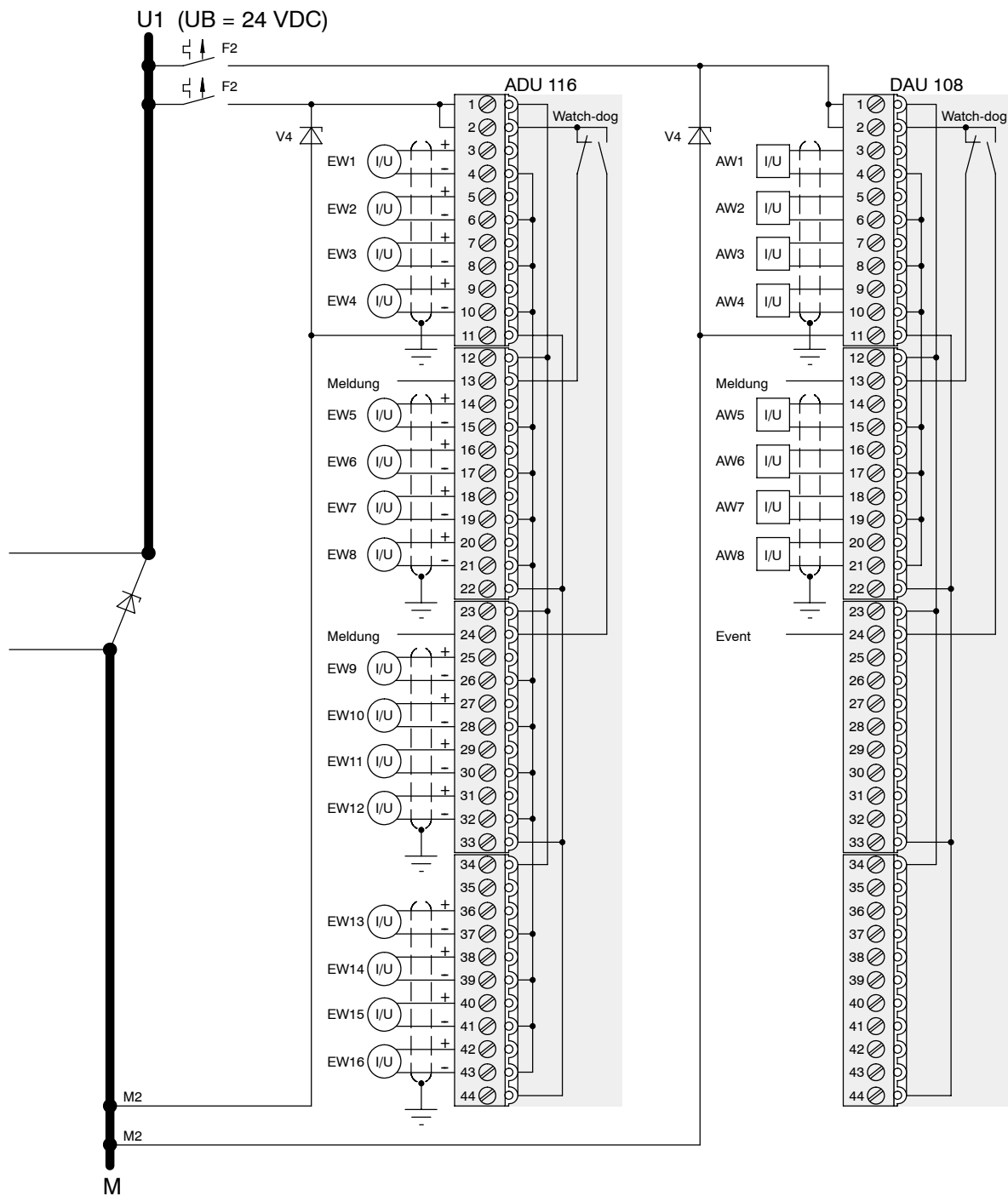
Figure 29 Detailed Port of the Power Supplies



- F4 Max. 4 A automatic circuit breaker for max. 500 inputs or 100 relays
The following is also required for the restart operating mode (off-delaying effect):
C2 Smoothing capacity; the size is dependent on the load
R1 Current limiting resistor: 0.86 ohms/3 W, AEG E no. 424 104 884
V3 BYW 80/200 isolating diode, AEG E no. 424 201 560

Figure 30 Detailed Port for the Supply of the Binary I/O Modules (Relay Coils, Sensors)

The noise immunity can be increased if this charge capacitors are connected to the U and M ports of the relevant module. See page 46 for more details.



F2 Max. 2 A automatic circuit breaker or medium time-like 2 A fuse
V4 Overvoltage protection (suppressor diode), 1N5646A type; AEG E no. 424 152 500

Figure 31 Detailed Port for the Supply of ADU 116 and DAU 108

The V4 overvoltage protection is required if the supply lines of the ADU 116 or the DAU 108 are longer than approx. 5 m.

The noise immunity can be increased if discharge capacitors are connected to the U and M ports of the relevant module. See page 46 for more details. The shields are to be earthed before entering the cabinet according to Figure 60 and guided up to the module.

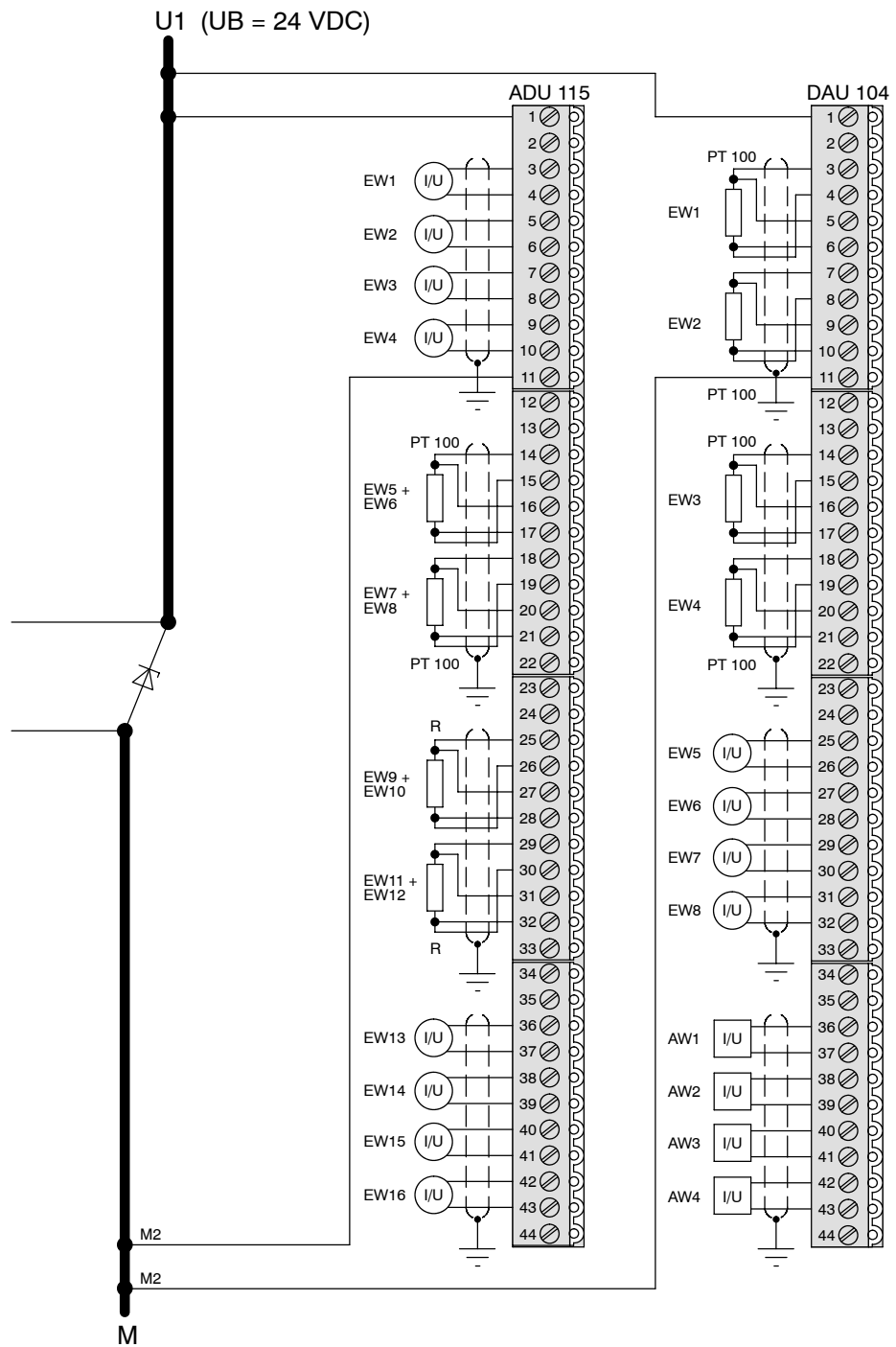
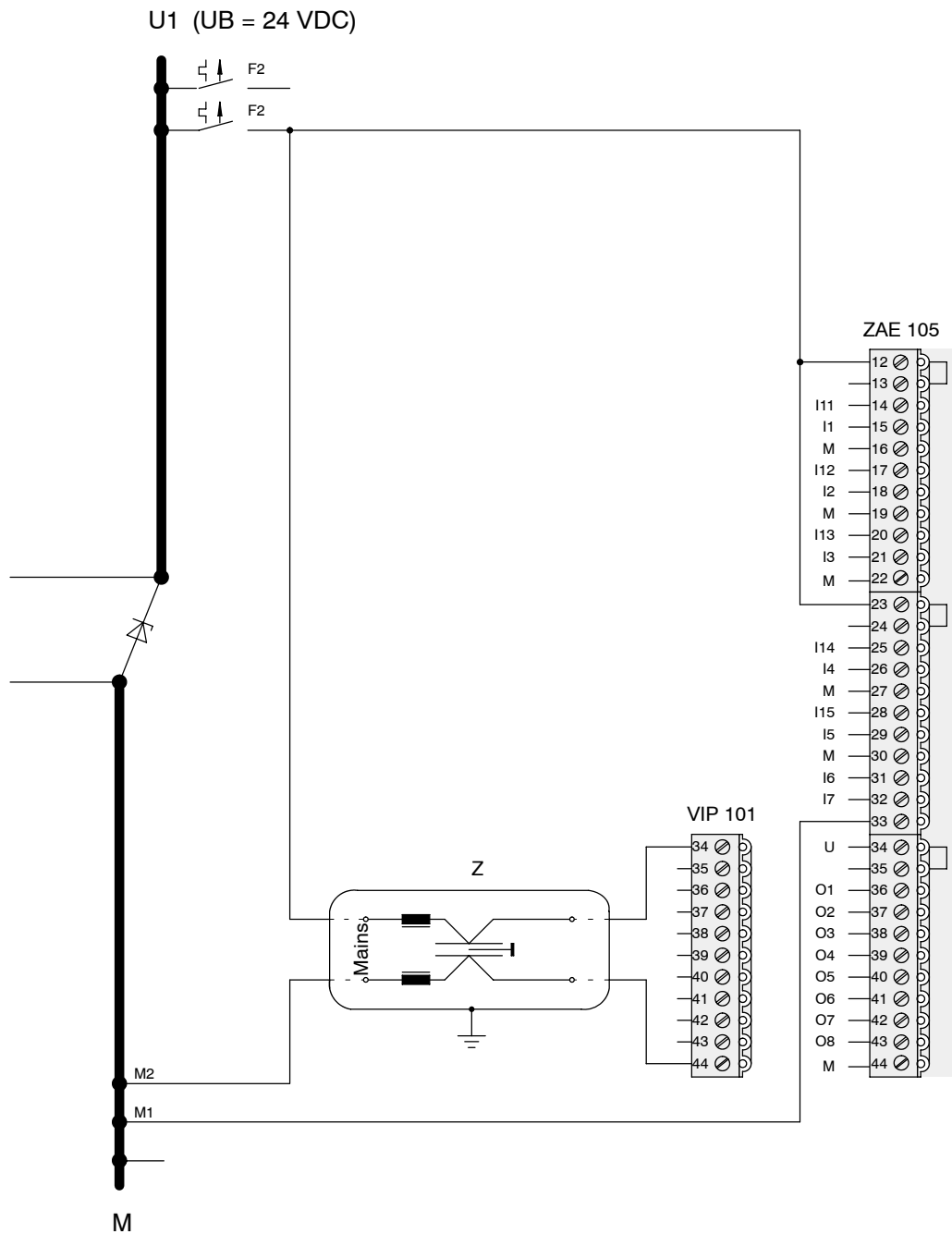


Figure 32 Detailed Port for the Supply of ADU 115 and DAU 104

The noise immunity can be increased if discharge capacitors are connected to the U and M ports of the relevant module. See page 46 for more details.

The shields are to be earthed before entering the cabinet in accordance with Figure 60 and guided up to the module.



F2 Max. 2 A automatic circuit breaker or medium time-like 2 A fuse
 Z 2 A suppression filter, 250 VAC, AEG E no. 424 084 047

Figure 33 Detailed Port for the Supply of VIP 101 and ZAE 105

An external 24 VDC supply (100 mA) must be supplied to the VIP 101 for keyboard with a current loop interface (PBT 103, DSG 101). A filter can be wired beforehand if the voltage is unfiltered and to avoid interference from electromagnetic influences.



Caution It is to be ensured that the filter is installed properly as regards the EMC and electrical requirements as shown in Figure 33.

3.2.3 Port Figure of the Working Voltage Supply ($U_S = 24 \text{ VDC}$ / $L = 230 \text{ VAC}$) for I/O Modules with Front Connection

The working voltages are combined for two or more outputs (corresponds to a group). Each group is to be fused separately.

Please ensure that no inadmissible overvoltages occur due to switching operations of inductive consumers as these can lead to the semiconductors being endangered or destroyed in the programmable controller.

$U_S = 24 \text{ VDC}$

The 24 VDC working voltage should be supplied by a separate power supply. Further power supplies are to be configured with load currents $>25 \text{ A}$.

Auxiliary circuits may be operated as earthed or unearthed according to VDE 0100 and VDE 0113. Use an isolation monitoring device with unearthed operation so that a message can be output if an isolation fault occurs.

Up to 60 VDC supplied actuators can be wired with the contacts of the DAP 103, DAP 104 and DAP 106 modules.

$L = 230 \text{ VAC}$

24 ... 230 VAC supplied actuators can be wired with the contacts of the DAP 103, DAP 104 and DAP 106 modules.



Note The use of only one power supply is permitted with a 24 VDC supply requirement of $<25 \text{ A}$ for the entire system.

The sections 5.2 "EMC measures", and 3.2 "Structure of the power supplies", are to be noted.

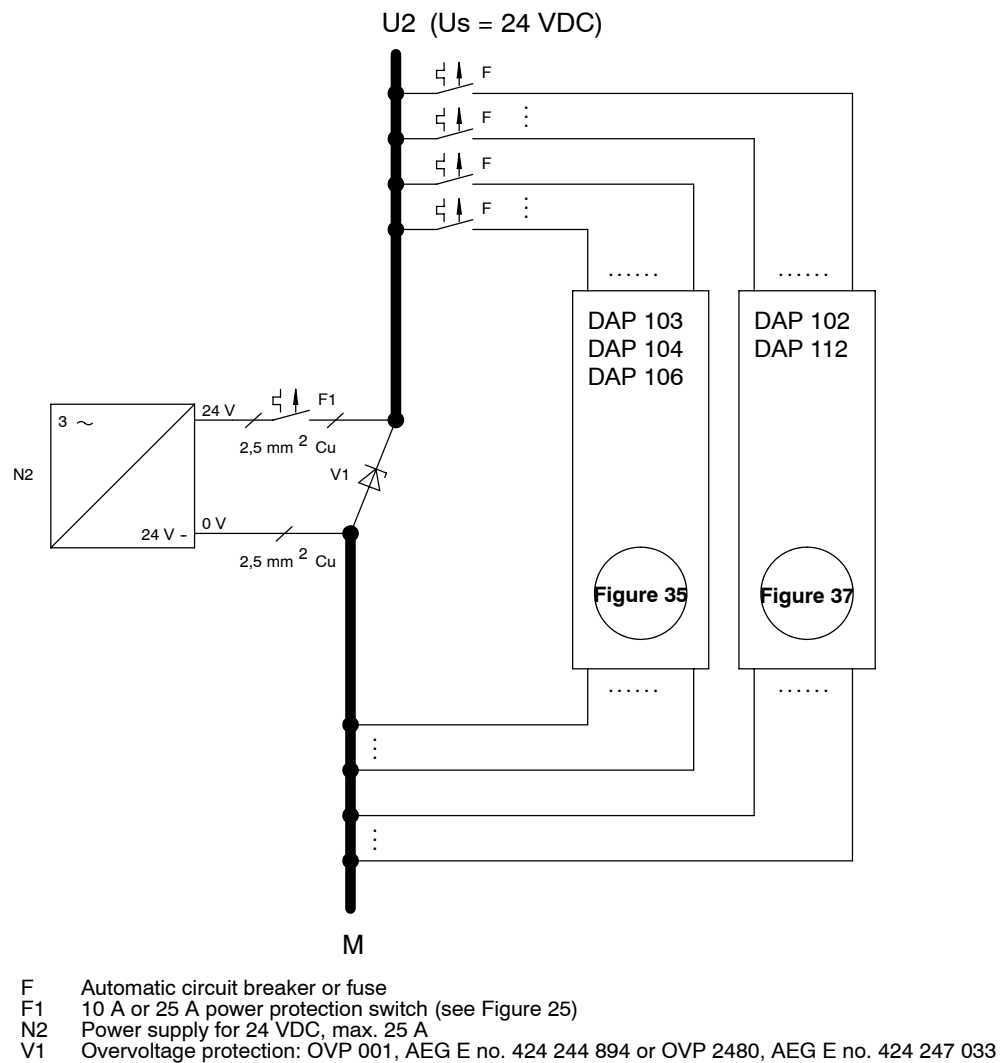


Figure 34 Port Survey of the U_s Supply (24 VDC)

We recommend you to divide the circuits according to the detailed port figures shown on the following pages.

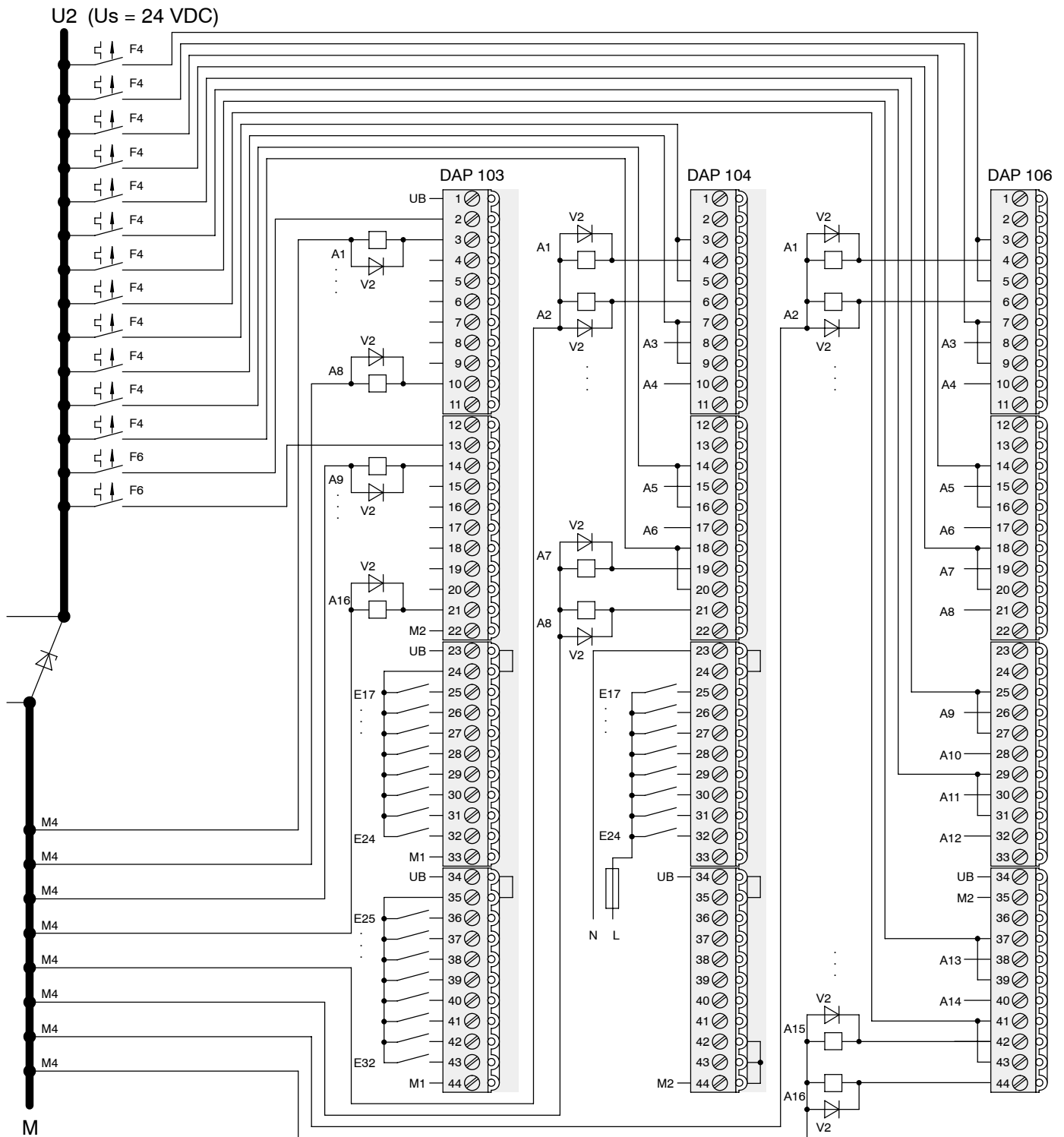
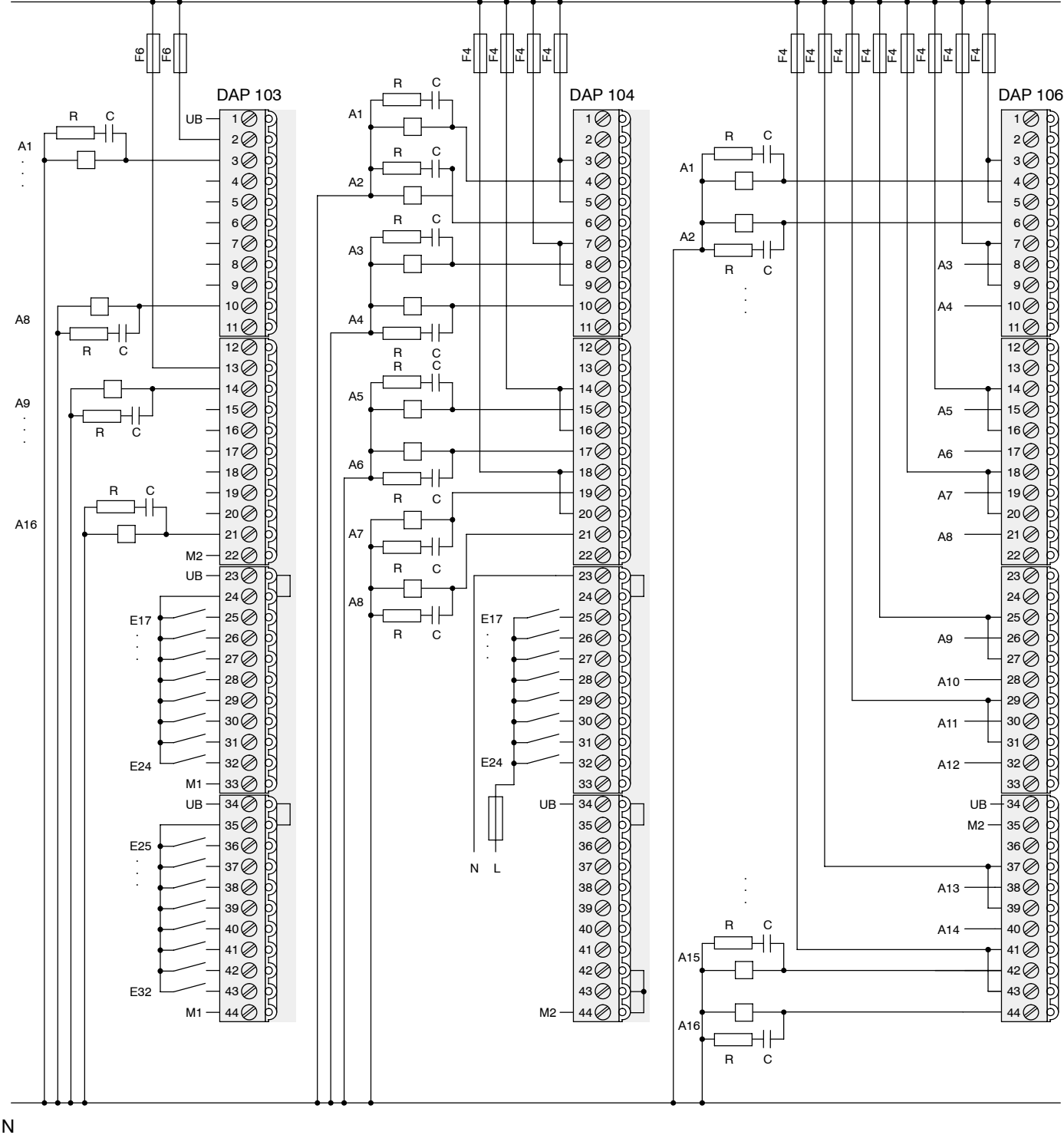


Figure 35 Detailed Port of the Relay Outputs for $U_S = 24$ VDC

The noise immunity can be increased if this charge capacitors are connected to the U and M ports of the relevant modules. See page 46 for more details.

L (230 VAC)



- F4 Max. 4 A fuse
F6 Max. 6 A fuse
L L1/L2/L3 phases
N Reference conductor
RC sufficiently dimensioned (according to the manufacturer) RC protective circuit, required at all costs with inductive actuators (loads)

Figure 36 Detailed Port of the Relay Outputs for L = 230 VAC

3.3 Switching Off Mode of the Binary Outputs with Malfunctions on the Power Supply

3.3.1 Switching Off Mode for Modules with Rear Connection

All the power supplies deliver a 12 V signal (WWSRN signal) when ready for service. This signal is supplied to the PEAB via the C04 contact pin and enables the signal outputs of the binary output modules. If malfunctions occur on the power supply (access temperature, undervoltage in the secondary area), the WWSRN signal of the affected power supply becomes 0 V and causes these outputs to be switched off for the length of the malfunction.

It must be configured so that

- each output module receives a WWSRN signal
- the output module receives the WWSRN signal from the power supply from which it is supplied

so that only the outputs are switched off, the power supply of which has a malfunction.

Carry out the necessary settings by means of plug-in jumpers. These are located on the DUV 025 (in each I/O subrack, in which a power supply and/or a DKV 022 is inserted) and on the DKV 023 (controller). Their effect is explained in Table 21.

Table 21 Meaning of the Jumpers when Configuring the WWSRN Signal






Jumper	Position	Effect
 A	DKV 023 (Controller)	interrupts the WWSRN signals from the power supply of the controller to the I/O module supplied via a separate power supply
	above the 813 contact comb on DUV 025 in the 1st I/O subrack	disconnects the in-coming WWSRN signal
	above the 810 contact comb on DUV 025 in the 1st I/O subrack	hands the current WWSRN signal over to the 3rd I/O subrack
	above the 813 contact comb on DUV 025 in the 3rd I/O subrack	supplies the in-coming WWSRN signal to the 3rd I/O subrack
	above the 810 contact comb on DUV 025 in the 3rd I/O subrack	prevents the current WWSRN signal from being handed over to other I/O modules which are not supplied by this power supply.

Figure 38 represents the course of the signal with the example of three DTA 025 which are all supplied via one power supply. This is inserted in the upper righthand subrack and supplies the current WWSRN signal to the PEAB via the 202 contact comb. The DKV 022 undertakes the connection between the ports 217 and 817 in the 1st and 3rd I/O subrack.

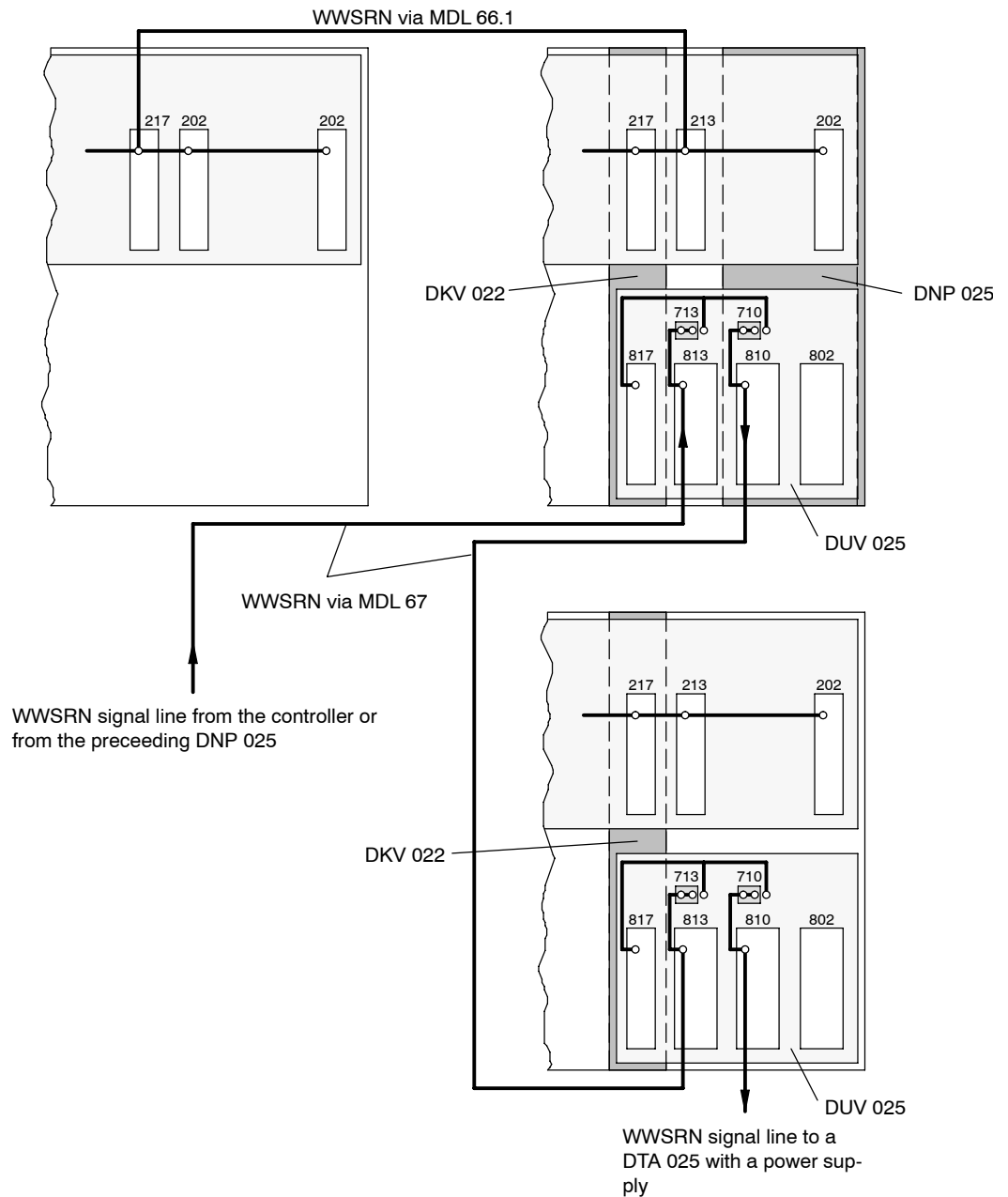


Figure 38 WWSRN Signal Path (with a View onto the Rear of the Subracks)

3.3.2 Switching Off Mode for Modules with Front Connection

The switching off mode of the output modules is controlled by the DEA in the case of a malfunction (interrupting the telegram traffic). A distinction is made between:

- ❑ Maintaining the signal status (permanently memorizing; this is valid for all system field bus nodes of a subrack, the DEA of which is set this way).
- ❑ The device is switched off after the monitoring time set in word 66 is over (this is valid for all system field bus nodes which do not have permanent memorizing)

Detailed information is included in the module description of the DEA ("Process peripherals with front connection" user manual).

3.4 Synchronization of the Power Supplies

It must be specified for systems with rear connection and several power supplies whether and/or in which way a voltage failure or a tolerance access of an output voltage of a power supply affects the other power supplies of the system as regards the wiring of the synchronization lines.

There are the following possibilities for the synchronization:

- ❑ All power supplies of a system operate independently.
- ❑ If an error occurs on the power supply of the controller, the peripheral power supplies are also switched off. If a peripheral power supply fails, this is registered via a time error of the I/O modules assigned to it (marker 21/31). The other intact power supplies are not switched off in this case (see Figure 39).
- ❑ Each power supply switches off all the other power supplies as well in the case of an error (standard case).

The SYNCN signal required for the synchronization and the relay contact are led to the subracks. The wiring measures to be carried out are described accordingly in the module descriptions of the relevant subracks. Figure 39 shows case 2 as an example.



Note The power supply does not switch on its secondary voltages without a corresponding wiring method.

3.5 PEAB Monitoring

The DKU 022 is provided to monitor the PEAB transmission paths, e.g., for line, connector or PEAB driver faults. Ascertained faults are documented in the marker area and can be evaluated (user program, process intervention). Details can be read in section 3.8.6 "Special marker area", and in the module description of the DKU 022.

Each pair of each I/O subracks to be monitored must be equipped with a DKU 022 for this purpose. It is to be inserted at the costs of an I/O module to the right next to the DKV 022 on slot 16.

The DKU 022 is to be entered in the EQL list (see information in section 3.10.1 and DKU 022 module description).

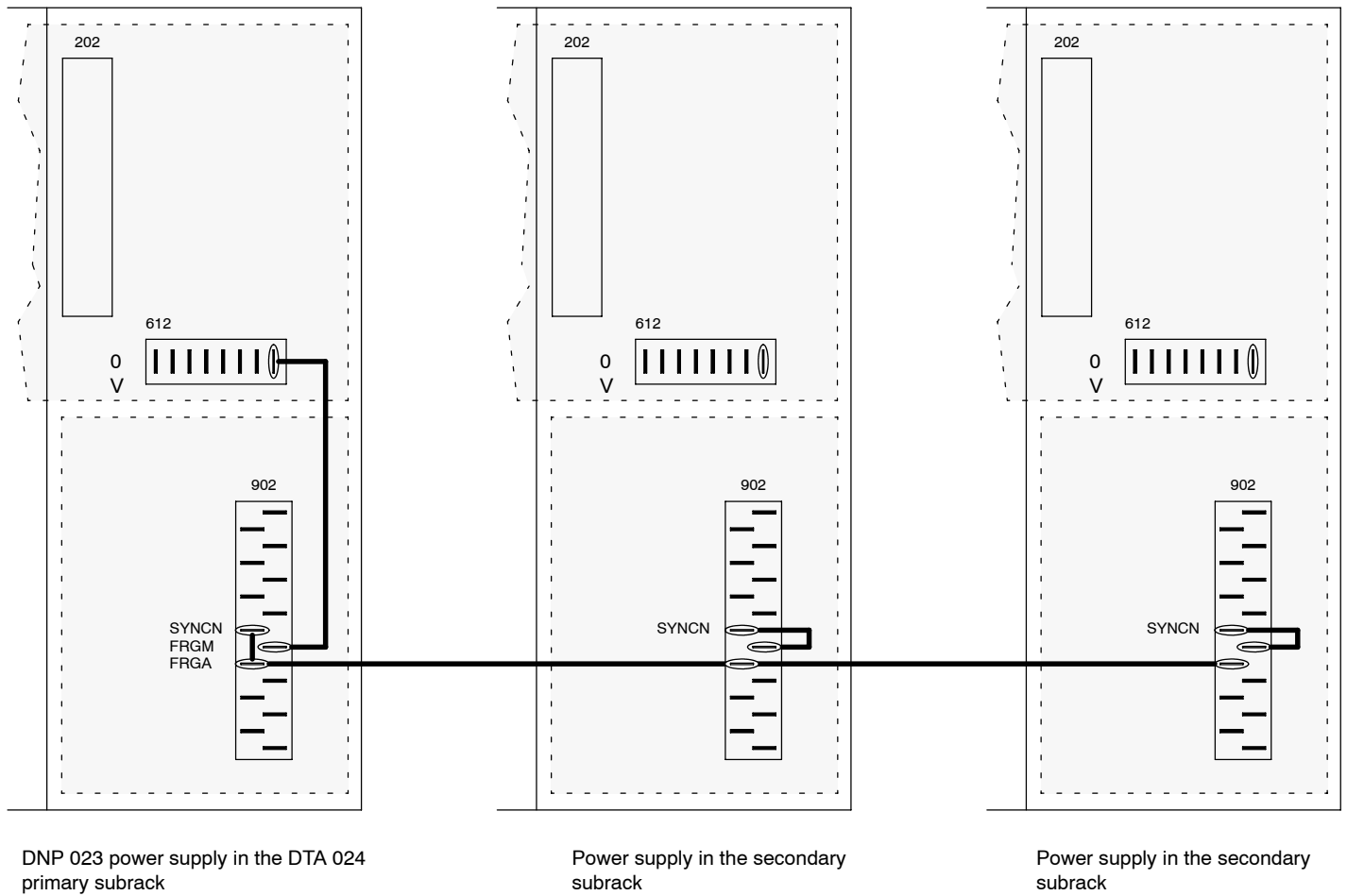


Figure 39 Example for Synchronizing 3 Power Supplies

3.6 Start-Up Characteristics



- ❑ Configure centrally a switch to switch the supply on and off. The supplies of the sensors and actuators as well as the supply of the A500 are to be included here.

Also configure an emergency stop device according to section 5.5 if there are possible risks to man and machine (page 130).



- ❑ Specify which start-up characteristics the A500 should have. The settings are to be carried out on the ALU itself or on ALU and UKA depending on the ALU type. The following variants are possible:
 - ❑ Manual start: The PSC only starts after a manual start command via a video terminal or programming panel.
 - ❑ Automatic start: The PLC automatically starts immediately after the voltage return. It starts at the start of the program (original start) or at the point of interruption (restart) depending on the position of the ALU pin.

It is to be ensured that no dangerous process statuses can occur during the voltage failure or voltage return. This is to be taken into consideration especially with a power-fail, since the voltage can return at an undefined time as opposed to the system being switched on and off by the user.

3.6.1 Start-Up Characteristics when Using the ALU 011

Manual start:	W13 jumper jumpered to unlabelled side	
Automatic start:	W13 jumper jumpered to labelled side	
		
Original start:	“Set” ALU pin plugged in	
Restart:	“Set” ALU pin not plugged in	

3.6.2 Start-Up Characteristics when Using the ALU 061

Manual start:	S8 jumper jumpered	
Automatic start:	S8 jumper not jumpered	
Original start:	“Set” ALU pin plugged in	
Restart:	“Set” ALU pin not plugged in	



Note The “automatic start” setting is only effective if a programming panel is not connected. If a programming panel is connected and switched on, the “manual start” is always valid.

3.6.3 Start-Up Characteristics when Using the ALU 150

The start-up characteristics are defined via settings which are to be made on the UKA and ALU (see Figure 40). Alterations to the settings are effective only after switching the controller on and off again.

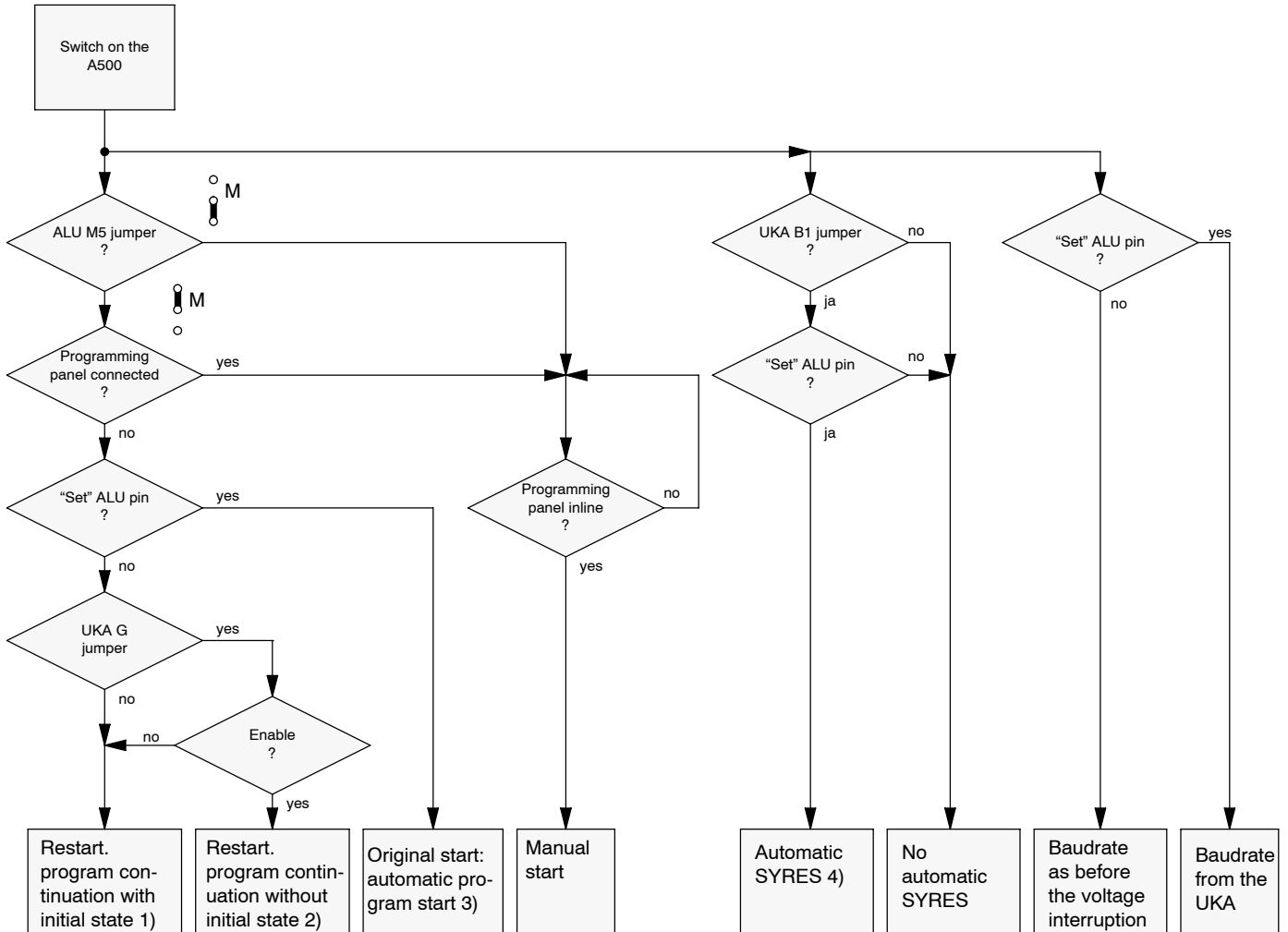


Figure 40 Specifying the Start-Up Characteristics when Using the ALU 150

Explanations to the flow chart:

- 1) The program is continued at the point of interruption. There are no outputs made when the END block is reached. Blocks with initial state characteristics are standardized in the following standardizing cycles. Blocks which are not processed in the cycles are not standardized (e.g., blocks in interrupt Vlists).
- 2) The program is continued at the point of interruption. Blocks with initial state characteristics are not standardized. These now behave like blocks with non-volatile characteristics.
- 3) Some standardizing cycles are executed with the original start. Blocks with initial state characteristics are standardized here. Blocks which are not processed in the cycles are not standardized (e.g., blocks in interrupt Vlists).
- 4) If an automatic program start is to be carried out according to SYRES (restoring the system variables), SYKON (recording the system variables) must be carried out with the program running, since otherwise the address of the memory area to be started is not stored at the same time with SYKON.

3.7 Installation

3.7.1 Settings for Modules

An overview of the settings and activities which are to be carried out for the relevant modules is given in the following. More details are to be taken from the relevant module descriptions.

DTA 024 / DTA 27.1 / DTA 028

- ☐ Earthing system (Z screws)
- ☐ Converting a PEABN slot for DKV 023, if necessary (with DTA 028 only)
- ☐ Connecting the battery block
- ☐ Wiring the monitoring signals
- ☐ Removing RAK jumpers from SES2 slots (with DTA 024 and DTA 028 only)
- ☐ Synchronizing the power supplies

DTA 101 / DTA 107

- ☐ Earthing system (Z screws, Z jumpers)
- ☐ Connecting the battery block
- ☐ Synchronizing the power supplies
- ☐ Modification for the B500-2 use (with DTA 107)

DTA 102/112, DTA 103/113

- ☐ Earthing system (Z jumpers)

DTA 025

- ☐ Earthing system (Z screws)
- ☐ Mounting the DUV 025
- ☐ Setting the subaddresses
- ☐ Removing RAK jumpers from SES2 slots
- ☐ Synchronizing the power supplies
- ☐ Supplying the PEAB

DUV 025

- ☐ WWSRN signal

DNP xxx

- ☐ Connecting the supply, power supply synchronization (wiring in the subrack)
- ☐ Wiring to extend the backup time

DKU 022

- ☐ No hardware settings

DKV 022

- ☐ Address group assignment (1st DKV, 2nd DKV, ..., plug-in jumpers of A and B)
- ☐ Interrupt evaluation (FAX contact socket)

DKV 023

- ☐ Interrupt evaluation (FAX contact socket)
- ☐ WWSRN signal guide (A jumper)

ALU 150

- ☐ Starting characteristics of the A500 (together with the UKA 024)
- ☐ Transmission rate of the V.24 interface
- ☐ Voltage for charging the rechargeable battery (BL jumper)
- ☐ Reset permitted or not permitted (R jumper)

SC 8128 / SC 8256

- ☐ Writing disable for RAM areas (SS1, SS2 contact sockets)
- ☐ Address setting of the memory blocks

SF 8512

- ☐ Equipping with EPROMs
- ☐ Address setting of the memory blocks

UKA 024

- ☐ Starting characteristics of the A500 (M5 jumper, together with the ALU 150)
- ☐ Status bits (B1 ... B4, E, G jumpers)
- ☐ PEAB plug-in check (SUE jumper)
- ☐ Watchdog time
- ☐ Evaluating the pilot relay
- ☐ Transmission rate of the V.24 interface
- ☐ Current loop operation of the interface (signal conversion, reference potential, supply and monitoring)

KOS 152, KOS 882

- ☐ KOS no. (addressing)
- ☐ Firmware equipment
- ☐ Link or Tesy
- ☐ Bus or star link (with KOS 882 only)
- ☐ Transmission rate of the V.24 interface
- ☐ Current loop operation of the interface

Modnet 1/SFB

- ☐ Specifying the Modnet 1/SFB node numbers
- ☐ Entire length of the bus, transmission type (transmission rate, cable type)
- ☐ Modnet 1/SFB termination (terminating resistor for BBS 1 plug)

BIK 151, BIK 812

- ☐ BIK no. (addressing)
- ☐ Entire length of the bus, transmission type (transmission rate, cable type)

DEA 106 / DEA 116 / DEA 156

- ☐ Slot reference (jumpers / DIP switches of A0 ... A7)
- ☐ Transmission rate for Modnet 1/SFB (jumpers / DIP switches of S0, S1 and R)
- ☐ Controlling the switching off mode of the output modules (S2, S3 jumpers)
- ☐ Non-isolating, electrical isolation of the Modnet 1/SFB (Z jumper)

DEA-H1 / DEA-K1

- ☐ Port of the supply
- ☐ Slot reference (A0 ... A7 jumpers)
- ☐ Transmission rate for Modnet 1/SFB (S0, S1 and R jumpers)
- ☐ Type of utilization of the inputs (with/without preceding logic operations, S2 and S3 jumpers)

ADU 115

- ☐ Type of measurand (current, voltage or resistance input, S1 ... S16 jumpers)
- ☐ Setting the measuring range (S20 ... S37 jumpers)
- ☐ Fritting ports (switched on or off, S41 jumper)
- ☐ Noise suppression (50 or 60 Hz, S42 jumper)
- ☐ Setting the identity code (3 or 33, S50, S51 jumpers)

ADU 116

- ☐ Type of measurand (current or voltage input per channel, K1 ... K16 jumpers)

DAP 102

- ☐ Type of utilization of the inputs (with/without preceding logic operations, F jumper)

DAP 103

- ☐ Type of utilization of the inputs (with/without preceding logic operations, S1 jumper)
- ☐ Setting the identity code (5 or 7, S2 jumper)

DAP 104

- ☐ Type of utilization of the inputs (with/without preceding logic operations, F1 jumper)
- ☐ Setting the sensor power supply (115/230 VAC, F2, F3 jumpers)
- ☐ Setting the identity code (5 or 7, S2 jumper)

DAP 106

- ☐ Setting the identity code (5 or 7, S2 jumper)

DAP 112, DEP 112, DEZ 160

- ☐ Do not carry out any settings on the module

DAU 104

- ☐ Type of measurand (Current, voltage or resistance input, S1 ... S8 jumpers)
- ☐ Current or voltage output (S10 ... S13 jumpers)
- ☐ Setting the measuring range (S20 ... S33 jumpers)
- ☐ Fritting ports (switched on or off, S34 jumper)
- ☐ Noise suppression (50 or 60 Hz, S35 jumper)

DAU 108

- ☐ Current or voltage input (K1 ... K8 jumpers)

3.7.2 Mounting and Equipping the Subracks

- Fix the subracks according to the module description ¹²⁾. Dimension drawings can be found in the module descriptions.
- The following subracks are suitable for **wall mounting**:
DTA 101, DTA 102, DTA 103, DTA 107, DTA 112, DTA 113
- All the subracks except for DTA 102 and DTA 112 are suitable for mounting in **19" holders**. Mounting flanges are required for DTA 101, DTA 103, DTA 107 and DTA 113 (ordering code: 424 234 113).
- Equip the subracks according to the pre-given configuration. Non-equipped slots in the controller and in the DTA 025 subracks are to be closed with dummy strips.
- Connect the modules according to the module descriptions ¹²⁾ (for the design of the peripheral ports, see also section 3.2)



Caution All the modules of the controller and with rear connection (PMB and PEAB nodes) may only be disconnected or plugged in with the supply switched off.



Note Modules with front connections may only be disconnected or plugged in with the supply switched on. The screw/plug-in terminals are to be removed before disconnecting the modules and to be re-installed after they have been plugged in only. However, the supply and working voltages of the affected modules should be switched off to avoid short-circuits; the bus supply (via DEA 1x6) can remain switched on.

¹²⁾ The module descriptions are included with the relevant modules. They are also combined for the modules of the controller in appendix B of this module, for the modules of the I/O periphery in the user manuals of "Process peripheries with front connection" and "Process peripheries with rear connection".

3.7.3 Discharge Measures

3.7.3.1 Discharge Measures for Analogue Shielded Cables

The following cable gives an overview of the recommended shielded cables depending on the intended purpose.

Table 22 Shielded Cable Designs

Type	E No. 424	Features	Purpose
JE-LiYCY	424 234 035	shielded, twisted as pairs, 2 x 2 x 0.5 mm ²	Inputs, outputs for ADU, DAU, ZAE System field bus for BIK and DEA
LiYrdF(Cgv)Y	424 002 691	shielded, 3 x 0.14 mm ²	DCF 77E for the DEZ 160

Earth the shielded lines as follows:

- Lay the shielded cables via the CER 001 cable earthing bar
- Remove the shield insulation at the level of the respective cable cleat
- Press the cable with the freed shield into the cable cleat (contacting to the top hat rails)
- Grip the individual cables with cable clips according to Figure 41

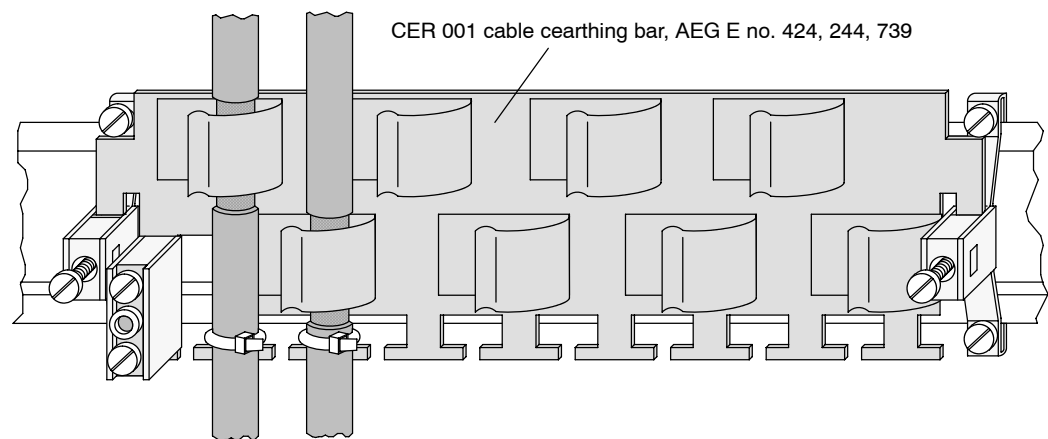
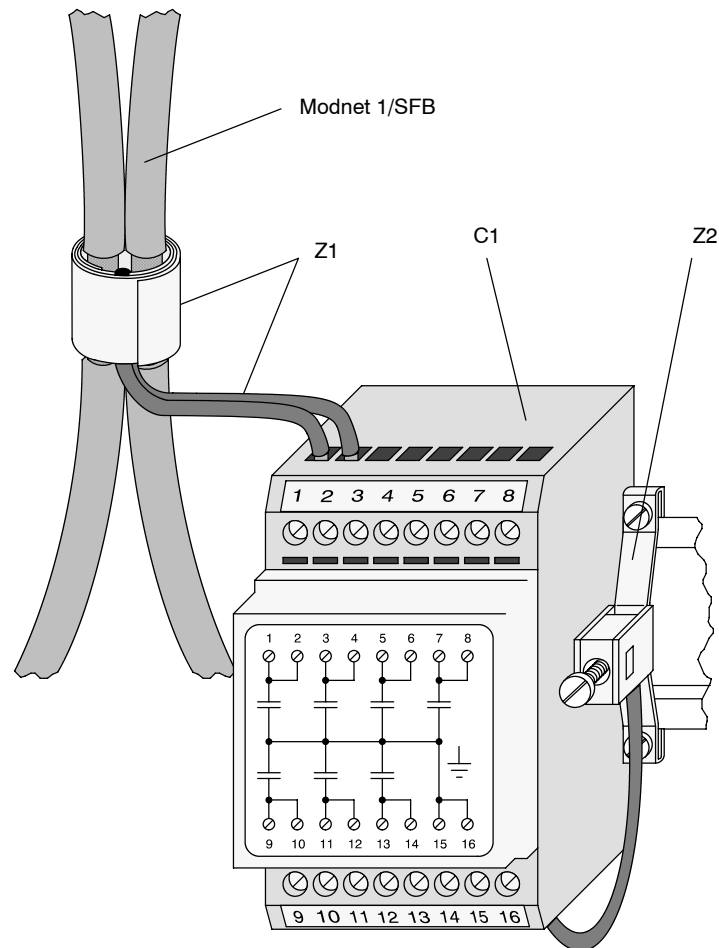


Figure 41 Earthing the Shields of the I/O Lines to the ADU, DAU, ZAE, ...

3.7.3.2 Discharge Measure for the Modnet 1/SFB

The system field bus may not be earthed directly to the respective nodes (slaves) but via discharge capacitors only.



- C1 GND 001 capacitive discharge terminal, AEG E no. 424 244 899
- Z1 Shield connection included in the delivery scope of the CER 001 cable earthing bar
- Z2 Earthing clamp, AEG E no. 424 249 007

Figure 42 Discharge Measure of the Shield for BIK as Modnet 1/SFB Node (Slave)



Note A longer system field bus cable which has already been laid but not yet connected must be discharged statically. Procedure:

- Plug BBS1 into the master (BIK) first
- Discharge the chassis of the other BBS1 (nodes) via PE

Proceed in the following way to install the shield connection:

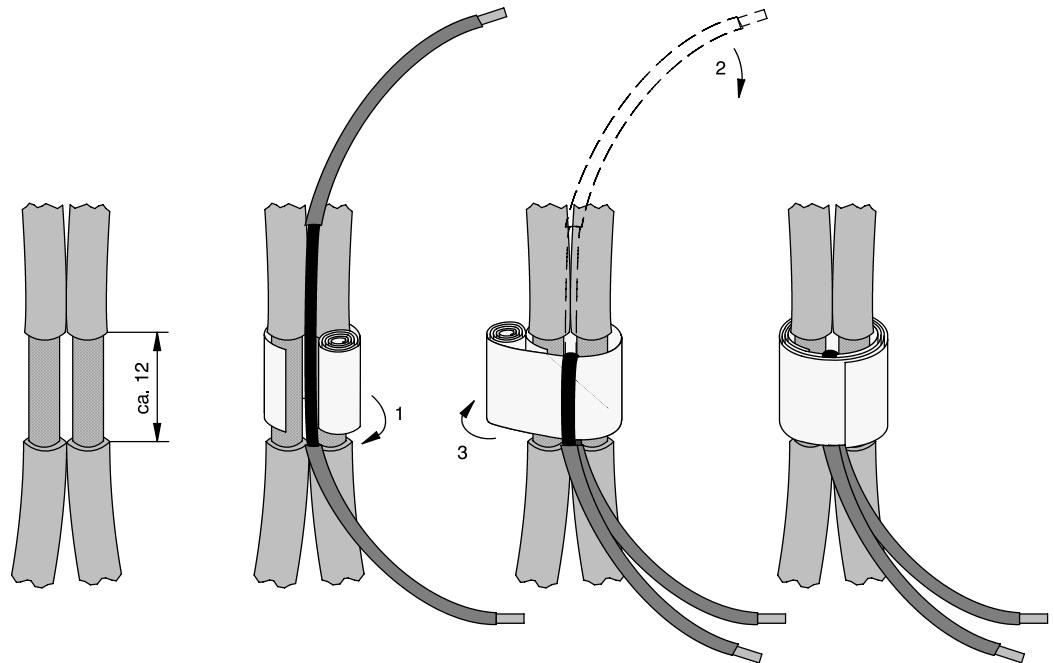
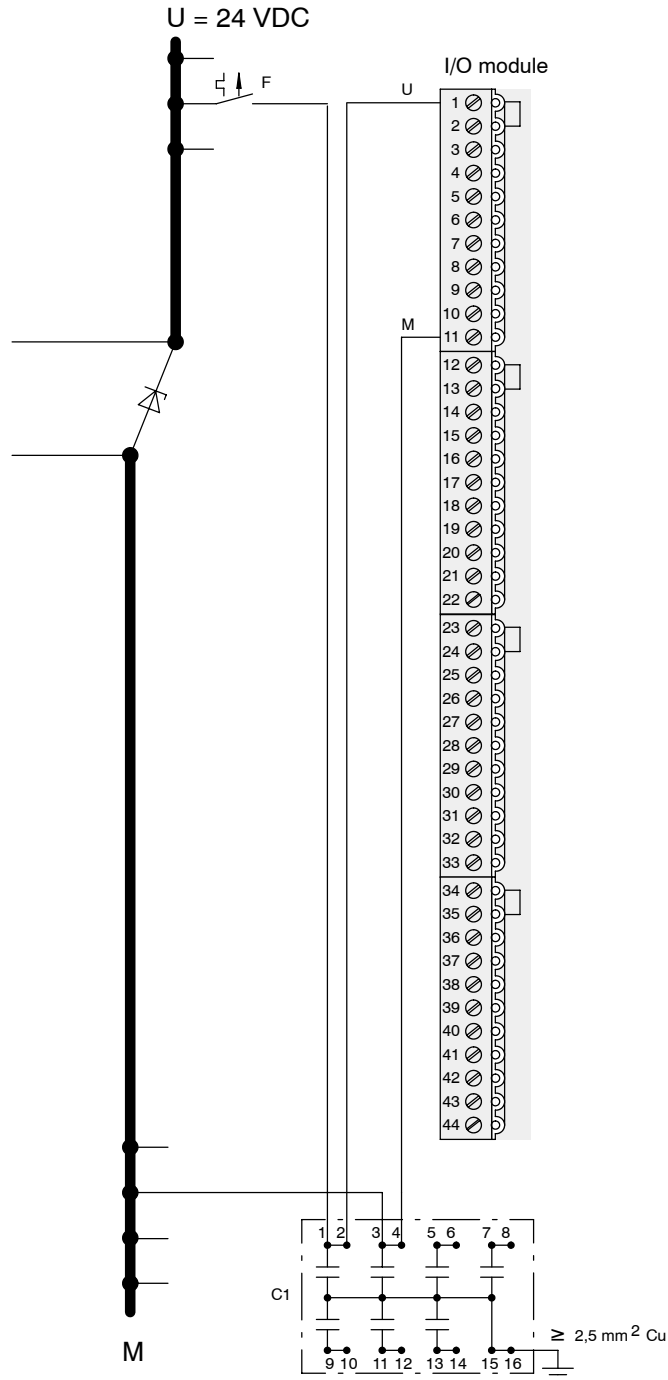


Figure 43 Installing the Shield Connection

3.7.3.3 Improving the EMC Immunity for the Modules

To improve the EMC immunity for the modules it is recommended to discharge the U and M ports used here from the terminal in a shorter way as possible to the functional earth. The GND 001 capacitive discharge terminal serves this purpose, see Figure 44.



F Automatic circuit breaker
C1 GND 001 capacitive discharge terminal, AEG E no. 424 244 899

Figure 44 Improving the EMC Immunity for the Modules

3.7.3.4 Overvoltage Protection for SFB Lines: Outside Buildings

To protect the transmission equipment, e.g., Modnet 1/SFB, against interfering overvoltages (lightning) it is recommended to use an overvoltage protection (lightning ductor). The nominal leakage current should be at least 5 kA here, e.g., ARE type, ordering code: 919 232 from

Fa. Dehn und Söhne
Postfach 1640
W-8430 Neumarkt 1
Germany

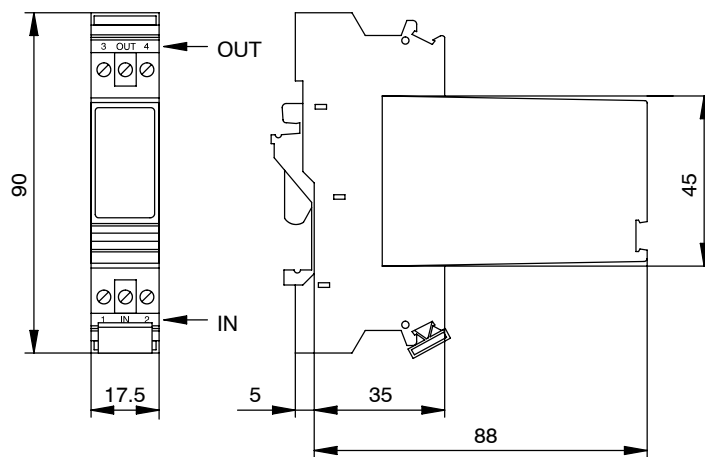
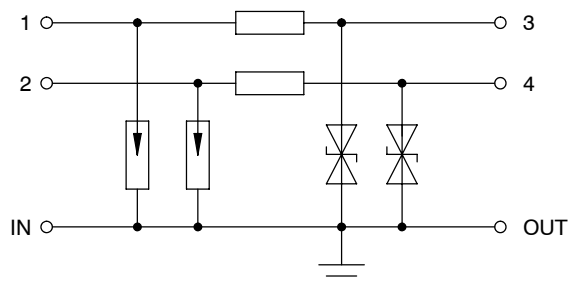
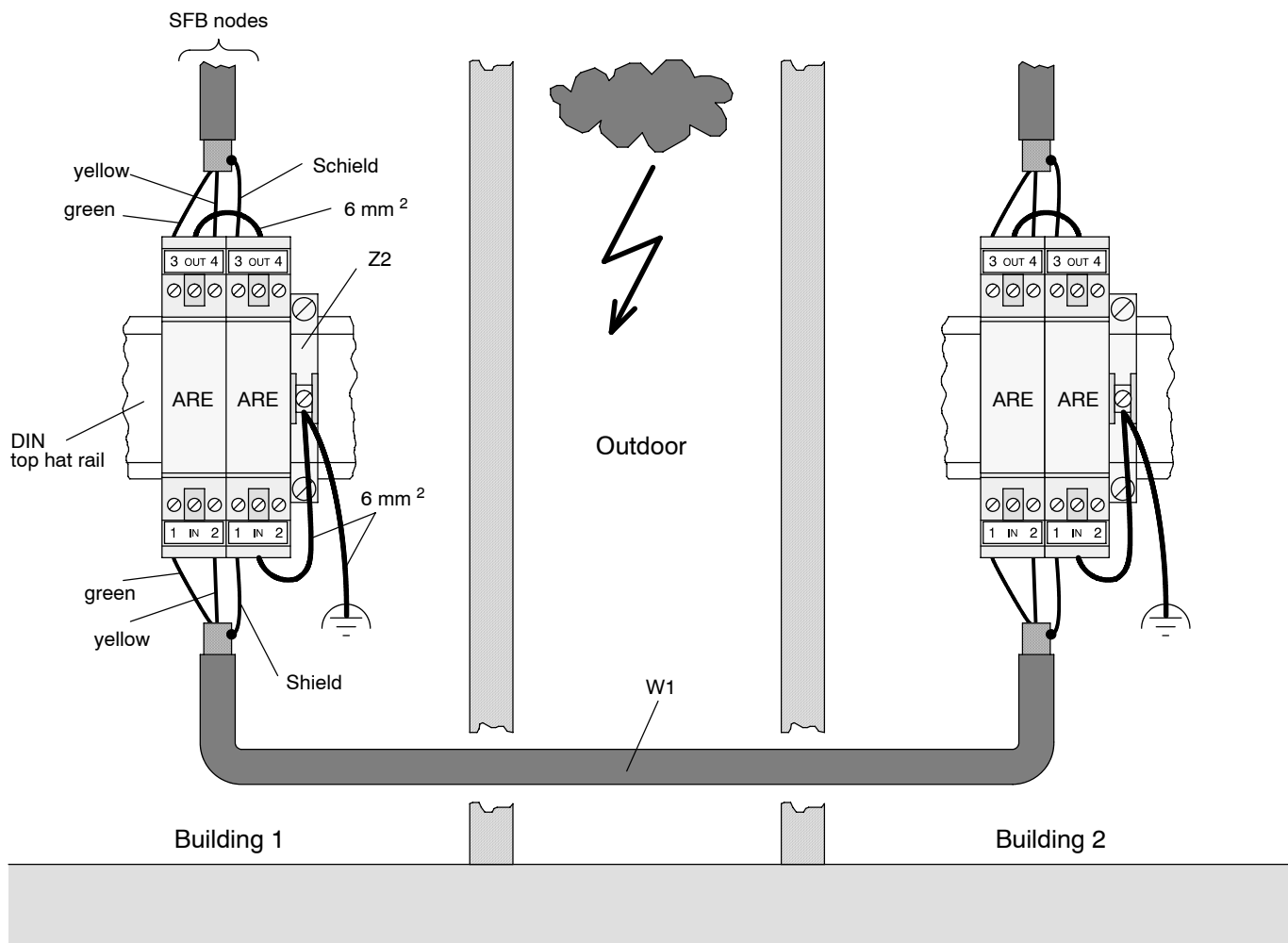


Figure 45 Circuit Diagram and Dimension Drawing of the ARE Lightning Ductor



W1 Modnet 1/SFB line of JE-LiYCY, AEG E no. 424 234 035
 Z2 Earthing clamp, AEG E no. 424 249 007

Figure 46 Port Diagram of the ARE Lightning Ductor

Observe the following criteria here:

- ❑ The yellow and green wires may not be confused for the continuity
- ❑ A functional earth (potential equilizer rail) is to be installed
- ❑ The lightning ducturs are to be installed near to the functional earth so that the search current is discharged along a short path to the building earth. The line to the functional earth is to be kept as short as possible with a cross-section of at least 6 mm²
- ❑ A maximum of 6 overhead lines can be protected with on system field bus

3.7.4 Connecting Peripherals

The peripherals mentioned in section 1.5 are to be used. Figure 47 shows their connection. Connection cables and interfaces for the printer port depend on the type of printer which you have selected and are documented in the operating instructions of the printers.

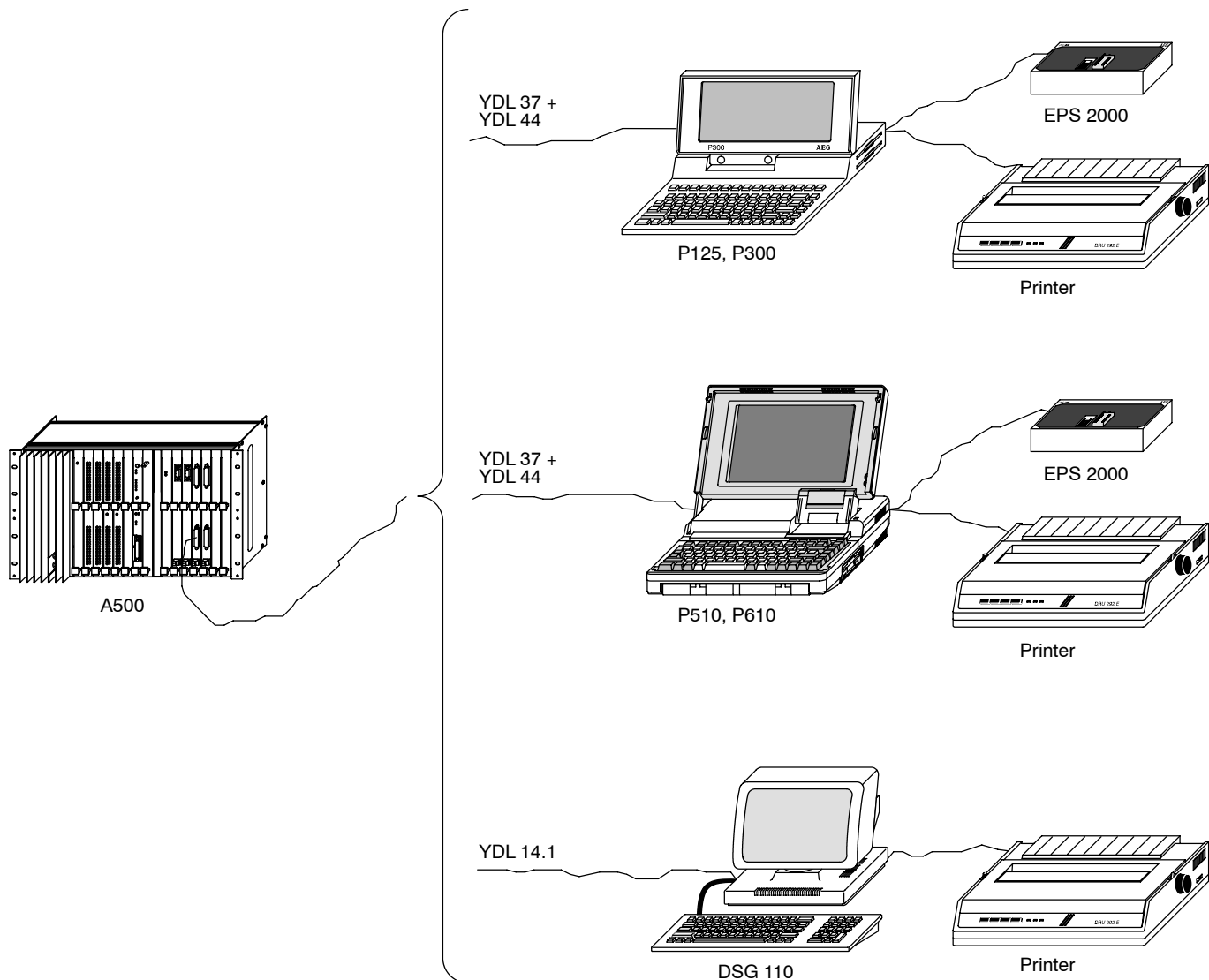


Figure 47 Connecting a Printer, Programming Panel and EPROM Programming Station



Warning Serious process interventions are possible with the operating and programming panels. It is therefore to be ensured that dangerous process statuses are avoided.

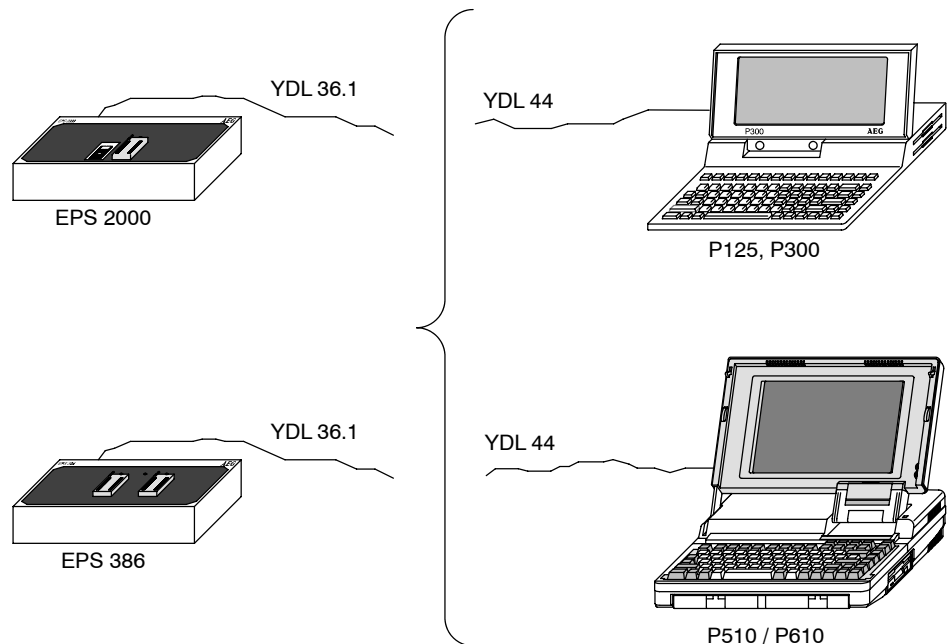


Figure 48 Connecting the EPS 2000 to the Programming Panel



Note If the user program is on EPROM and if you are working without a battery back-up, the system variables must be restored automatically after each time the A500 is switched on and off, if the system variables are also saved on EPROM. However, the current process image in the signal memory is then lost.

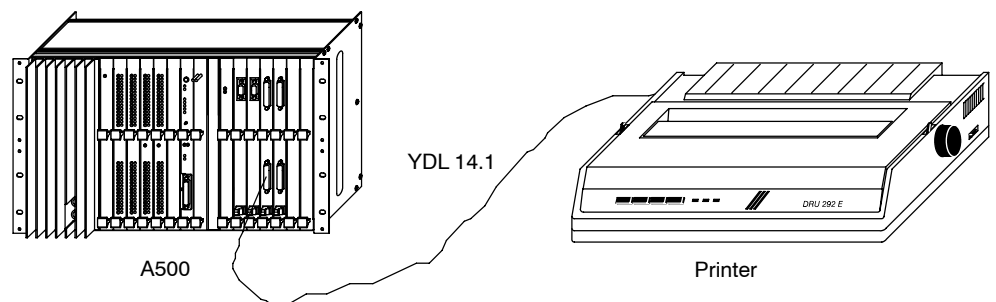


Figure 49 Connecting a Printer for Tesy

3.8 Addressing the Memory

3.8.1 Address Capacity

The ALU of the A500 has a microprocessor at its disposal which makes a 20 bit wide address bus available. 1,048,576 addresses ($= 2^{20} = 1 \text{ M}$) can thus be addressed, whereby one byte can be addressed each time.

This address capacity of 1 Mbyte is divided into a fixed grid of 32 segments. Each segment covers an address capacity of 32 kbytes. All the memory cells are addressed byte by byte from 1 ... 32 768 (decimal) within each segment.

(absolut) physical address		(Relative) address inside the segment	
Decimal	Hexadecimal	Segment	Dezimal
Byte 0000000	Byte 00000	1	Byte 00001
Byte 0032767	Byte 07FFF		Byte 32768
Byte 0032768	Byte 08000	2	Byte 00001
Byte 0065535	Byte 0FFFF	3	Byte 32768
Byte 0065536	Byte 10000		Byte 00001
		4	Byte 32768
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
		30	
Byte 0983040	Byte F0000		Byte 00001
		31	
Byte 1015807	Byte F7FFF		Byte 32768
Byte 1015808	Byte F8000		Byte 00001
		32	
Byte 1048575	Byte FFFFF		Byte 32768

Figure 50 Addressing the Memory in the A500

3.8.2 Dividing the Memory into Segments, Memory Areas

In order to be able to work with the A500, so-called memory areas (SB) still have to be set (via the first-time parameter assignment for Dolog AKF or with the Bsdol function of ASB for Dolog B). Programs, texts and data are saved in these memory areas.

A total of 32 memory areas can be defined over the entire available address capacity. Each memory area is always limited to one segment. The size of the memory area is freely selectable within the segment. Either one memory area which covers a maximum of 32 kbytes can therefore be opened in one segment or several memory areas which must then be correspondingly smaller. The memory area numbers can be given from 1 ... 32 as desired.

The starting address of a memory area within the segment is to be specified by the user. The address counting starts with the address of 1 within the memory areas. The assignment to the absolute addresses is carried out by the system. Address gaps between the memory areas are permitted.



Caution We recommend you to select addresses which result in the remainder of 1 when they are divided by 4 (e.g., 101, 121, 125, ...) when creating the memory areas. Problems which can occur when burning EPROMs can therefore be avoided.

Example:

- ☐ Memory area 3
- ☐ 2000 bytes large
- ☐ starting from the relative address of 101 in segment 9

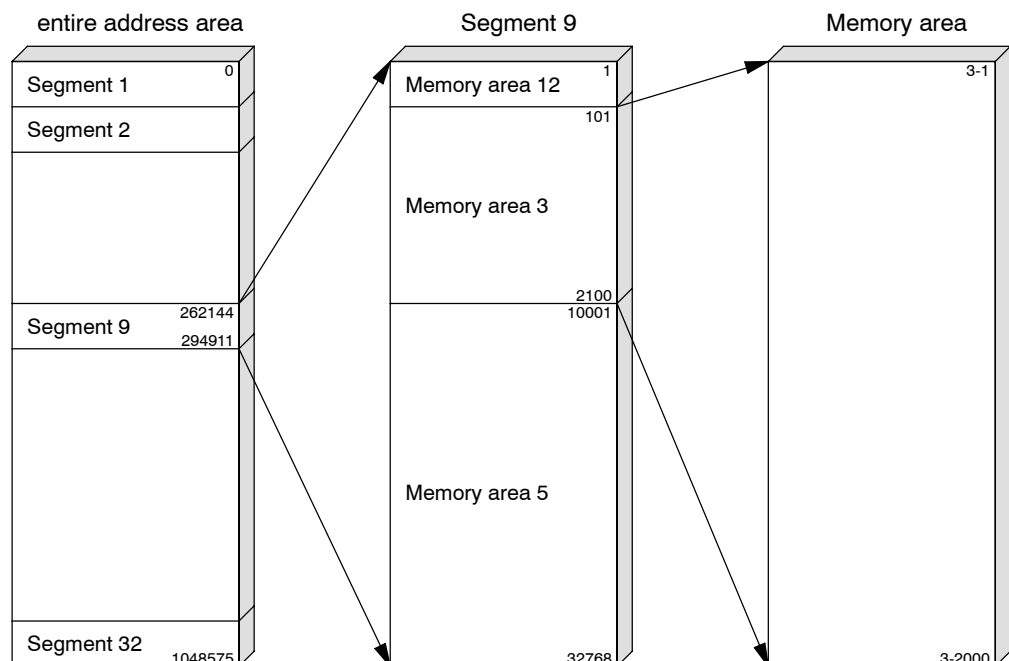


Figure 51 Addressing Memory Areas

3.8.5 Segments 1 and 2, Signal Memory

Segments 1 and 2 are located on the ALU. It is a question of a RAM area, which is mainly occupied by the system. Only a part of segment 1 is available to the user.

Segment 1 also includes the signal memory. The signal memory stretches over all the I/O bits, marker bits and words, double words and floating point words. The occupation of segment 1 is shown in Figure 52.

Byte 00001	System RAM	
Byte 01816		
Byte 01817	EQL list	
Byte 02136		
Byte 02137	System RAM	
Byte 06302		
Byte 06303	Marker 10000	
	Marker bits	⋮
Byte 07552	Marker	1
Byte 07553	I/O bits for address 160 E2 . . . 160 E32 I/O bits for address 160 A2 . . . 160 A32	
	I/O bits	⋮
	I/O bits for address 2 E2 . . . 32 E2 I/O bits for address 2 A2 . . . 32 A2 I/O bits for address 1 are occupied by UKA	
Byte 08192	System RAM	
Byte 12769	Word 10000	
	Word area or empty memory space*	⋮
Byte 31768	Word	501
Byte 31769	Word	500
	Word area (basic setting)	⋮
Byte 32768	Word	1

Figure 52 Memory Occupation of Segment 1 (on a Grey Background; Signal Memory)

* The number of the words (single words, double words and floating point words) can be defined on-line with the Bsdol function of AAW and off-line via special menu points in the corresponding software kits. The basic setting amounts to 500 words and is also the lower limit. Double words and floating point words count as 2 words. A maximum of 10,000 words can be set. If more than 500 words are defined, the empty memory area for each other single word is reduced by 2 bytes, for each other double and floating point word by 4 bytes. If 10 000 words are set, there is no more empty memory space in segment 1.

3.8.6 Special Marker Area

The markers of 1 ... 65 are occupied by the system; the markers of 66 ... 99 are reserved by the system for a subsequent use. Their meaning is given in the following for the valency of 1. The opposite meaning is then valid for the valency of 0. The remaining markers of 100 ... 10 000 are freely available for the user.

Table 24 Special Marker Area

Marker	Meaning	
1	Starting signal (after original start / restart for a loop = 1)	
2	0.3125 Hz flash	
3	0.625 Hz flash	
4	1.25 Hz flash	
5	2.5 Hz flash	
6	5.0 Hz flash	
7	Initial state of the sensor bit monitoring	
8	Starting characteristics of the program (0 = restart, 1 = original start); is set by the software at the end of the program	
9	(free)	
10	Constant 0 (zero)	
11	Constant 1 (one)	
12	Sensor bit, G jumper (UKA 024, ALU 0xx)	
13	Console space, E jumper (UKA 024, ALU 0xx)	
14	User program is running	
15	(free)	
16	(free)	
17	(free)	
18	Loading system variables (= 1: no valid data in segment 16)	
19	Loading system variables (= 1: automatic SYRES has taken place)	
20	Error in the signal check loop (PEAB plug-in check; this is not carried out by the ALU 061; error message can be suppressed by jumpering C10 and C12 pins on the UKA 024 or LI and LO ports on the ALU 011)	since the original start
21	PEAB time error (e.g., through the failure of a peripheral power supply)	since the original start
22	Access temperature on UKA 024 or ALU 061	since the original start
23	Battery undervoltage when the device is switched on (HE or RESET)	since the original start
24	(free)	
25	SEA parity	since the original start
26	with ALU 150: UKA 024 is faulty or missing	since the original start
27	Group error of Dolog blocks	since the original start
28	Undervoltage of the rechargeable battery	since the original start
29		
30	Error in signal check loop (PEAB plug-in check is not carried out by the ALU 061; error message can be suppressed by jumpering C10 and C12 pins on the UKA 024 or LI and LO ports on the ALU 011)	since restart
31	PEAB time error (e.g., through the failure of a peripheral power supply)	since restart
32	Access temperature on UKA 024 or ALU 061	since restart
33	Battery undervoltage when the device is switched on (HE or RESET)	since restart
34	(free)	
35	(free)	
36	with ALU 150: UKA 024 is faulty or missing	since restart
37	Group signal of the Dolog blocks	since restart
38	Undervoltage of the rechargeable battery	since restart
39		
40	Communication: transmit buffer is full	
41	Communication: telegram format error	
42	Communication: transmit initialization. Transmits all the configured logical message numbers, if, however, not to be set	
43	Communication: transmit disable	
44	Communication: receive disable	
45	Communication: receive buffer is full	
46	Communication: KOS error	
47	Communication: B500 transparent mode is active	

Marker	Meaning
48	Communication: receive bit is ignored with a stationary user program
49	Communication: transfer is faulty (a transfer telegram was rejected)
50	occupied for B200
51	(free)
52	(free)
53	(free)
54	(free)
55	(free)
56	(free)
57	(free)
58	PEAB supply has failed (cause: UKA 024, ALU 0xx or ALU 150)
59	Reaction to marker 58: 1 → program stops; 0 → program is continued despite PEAB failure; distributed I/O are still processed (to be defined by the user)
60	To be pregiven by the user; if 1 → drop-out of the signal relai, watchdog goes out
61	PEAB group error
62	Group error of the memory bus
63	Memory test is running
64	Memory test is faulty
65	Group error of Modnet 1/SFB
66-99	Reserved for later use

3.8.7 Special Word, Double Word and Floating Point Word Area

Words 1 ... 89 are occupied by the system, 90 ... 99 reserved by the system for later use.

Table 25 Special Word Area

Words	Meaning
1	(free, reserve)
2	Number of the maximum 10 ms interrupts/cycles since original start
3	Number of the minimum cycles/seconds since original start
4	Number of the maximum 10 ms interrupts/cycles since restart
5	Number of the minimum cycles/seconds since restart
6	Number of 10 ms interrupts/cycles with last value
7	Number of the cycles/seconds with last value
8	System (not available for the user)
9	PEAB address with an occurred time error (PEAB-ZF) with an error in pin row O: value = slot reference with an error within pin row I: value = slot address + 1000
10	Address of the encode bit (to be pregiven by the user). The addresses are composed of: Slot reference x 1000 + pin no. x 100 + code number for the pin row: 0 for O row, 100 for I row
11	(free, reserve)
12, 13 to 24, 25	12 - 25: Memory area and address for a maximum of seven user special drivers for inputs (EQL list 12). One of the seven word pairs contains the memory area in the first word, the address of the driver in the second word.
26, 27 to 38, 39	26 - 39: Same as for 12 - 25 for outputs (EQL list 26)
40, 41 to 58, 59	40 - 59: Memory area and address of the first ten Dolog blocks operating incorrectly. One of the seven word pairs contains the memory area in the first word, the address of the block starting from the second one. The error messages are deleted if the lefthand ALU pin (set socket) is plugged in at the start of the program.

Words	Meaning
60	Year
61	Month
62	Day
63	Hour
64	Minute
65	Tenth of a second of a minute. Value range: 0 - 599
66	Monitoring time for Modnet 1/SFB (must be larger than the program cycle time!). This also serves as a short-term / long-term memory for all DAP modules which are connected via Modnet 1/SFB: 0: Permanent memory (5 ... 255) x 10 ms: Short-time memory
67	Location of the malfunction on Modnet 1/SFB
68	Error number (type of error on the Modnet 1/SFB)
69	(free)
70	(free)
71	Code number for the transmission rate set with the software: 0 → 110 bd 1 → 300 bd 2 → 1 200 bd 3 → 2 400 bd 4 → 9 600 bd 5 → 19 200 bd the hardware setting is valid on the UKA 024, ALU 0xx or ALU 150 with ON/RESET/"HE"
72-76	(free)
77,78	Floating point word; cut-out address for control blocks
79	(free)
80,81	Floating point constant; contents = 0
82,83	Floating point constant: contents = 1
84,85	Floating point constant: contents = 10
86,87	Floating point constant: contents = 50
88,89	Floating point constant: contents = 90
90-99	Reserved for later use



Note The words of 80 ... 89 must be set with the basic software version 5 by the user himself.

3.9 Check List for the Initial Start-Up and Test

The measures which are necessary or recommended for the initial start-up are described in the following section. The modules which are included in the standard versions are also listed. The given jumper connections are to be carried out if necessary. The meaning of the individual setting measures is not explained in detail. It is to be taken from the relevant module descriptions.



Note The settings on the system can deviate from those described here in the subsequent operation of the system. The settings are to be adapted to the necessities of the relevant application (see relevant module description).

Alterations to the settings of DIP switches and plug-in jumpers are only effective after the supply voltage of the controller has been switched off and switched on again.

3.9.1 Settings, Ports, Equipment

UKA 024 (setting for V.24 operation)

- ☐ SUE jumper jumpered to the right
- ☐ M5 jumper jumpered to the left (open)
- ☐ LS → V.24 jumper plugged in to the right
- ☐ BR1 - BR3 jumpers closed
- ☐ B1 jumper closed, B2 - B4 jumpers open
- ☐ Jumper for transmission rate jumpered to 9 600 bd
- ☐ E jumper open
- ☐ G jumper open

ALU 150

- ☐ Set pin plugged in
- ☐ Reset pin not plugged in
- ☐ R jumper plugged in
- ☐ DIP switches:
 - 1 → 0
 - 2 → 0
 - 3 → 1
 - 4 → 1
- ☐ M jumper jumpered to the labelled side (top)
- ☐ BL jumper closed

SC 8128 / SC 8256 / SF 8512

- ☐ Plug-in jumpers for segments are correct (no double uses!)

KOS 152 (Settings are Only Valid for the 1st KOS with TESH)

- ☐ Modnet 1N / TESH firmware inserted
- ☐ T jumper jumpered to TESH (lefthand side)
- ☐ MN jumper plugged in to the labelled side (bottom)
- ☐ P jumper plugged in to the unlabelled side (top)
- ☐ A15 jumper closed, A12 - A14, A16 - A18 jumpers open
(segment 3, 1. 8 k block, $\hat{=}$ 1st KOS)

BIK 151 (Settings are Only Valid for 1st BIK)

- ❑ M jumper closed
- ❑ R jumper plugged in to the labelled side
- ❑ S0, S2 jumpers closed, S1, S3 - S5 jumpers open
- ❑ A13, A15 jumpers closed, A14, A16 - A18 jumpers open
(segment 3, 2nd 16 k block, $\hat{=}$ 1st BIK for I/O)

DEA 106 / DEA 156 (Setting for Slot References 2)

- ❑ R jumper plugged in to the labelled side (2 wire operation)
- ❑ A1 jumper closed, A0, A2 - A7 jumpers open (slot reference 2)
- ❑ Z jumper open (system field bus is potential-free)
- ❑ S0 jumper closed, S1 - S3 jumper open (transmission rate: 375 kbits/s, outputs are switched off 2.55 s after a malfunction)

General

- ❑ MOS rubber plugs are removed from all plugs
- ❑ Interface plugs and modules are screwed down
- ❑ Subracks are earthed
- ❑ The modules are connected according to section 3.2
- ❑ Data which are specific to the system are written on the fill-in labels of the individual modules; fill-in labels are pushed into the subracks (only with I/O modules with front connection)



Caution Switch off the external supply or working voltage of the affected module before removing an I/O module from the subrack.

3.9.2 Information About the Initial State Disable (G Plug-In Jumper on the UKA)

The standardization of Dolog blocks with initial state characteristics can be prevented via a peripheral input signal. This signal can only be recognized via the PEAB, i.e., it can only be generated by modules with rear connections. The initial state disable is only valid in the case of the program continuation (Restart, see Figure 40). Which peripheral input signal (enable) causes the suppression of the initial state characteristics is laid down in word 10.

The enable signal must be 1 when the device is switched on so that the initial state characteristics are suppressed.

Selection of the address of the peripheral input signal for the enable:

$$\begin{aligned} \langle 10 \rangle &= 1000 \times \text{slot reference} + \text{pin number for a signal of the O row} \\ \langle 10 \rangle &= 1000 \times \text{slot reference} + 100 + \text{pin number for a signal of the I row.} \end{aligned}$$

The controlling peripheral signal must have a slot reference which ≤ 32 .

Example: Slot reference 3

Pin number 16

I row

$$\begin{aligned} \rightarrow \quad \langle 10 \rangle &= 1000 \times 3 + 100 + 16 \\ \langle 10 \rangle &= 3116 \end{aligned}$$

3.9.3 Initial Start-Up

The contents of the RAM memory are not defined when the A500 is switched on for the first time. However, the A500 attempts to start a program when it switched on depending on the hardware setting. If this attempt is not prevented (see Figure 40), it is not possible to make contact with the A500. It is therefore necessary to make the settings mentioned in 3.9 during the initial start-up. If this is guaranteed, contact can be made with the A500 in the following way:

Step1 Create the connection between the A500 and the operating device or programming panel (plug in the corresponding cable on the RS 232C interface of the UKA or ALU 0xx, cf. section 3.7.4)

Step2 Switch on the operating device or programming panel

with a video terminal (DSG 110):

- ☐ Setting the data format (see the relevant operating instructions)
- ☐ Press CAPS LOCK (the A500 recognizes capital letters only)
- ☐ Enter <CTRL> +

with a programming panel:

- ☐ Call up the relevant program (see the relevant operating instructions for the installation)
- ☐ Call up the P150 operation (video terminal emulation); the transmission rate must be set if necessary.

Step3 Switch on the A500.

The A500 now registers with "DOLOG B:" and also indicates the type of ALU and the version number of the basic software.

Step4 Now enter the I/O equipment and the user program. You will find details:

- ☐ for the programming **Dolog AKF** in the documentation enclosed with the software kit
- ☐ for the offline programming in **Dolog B** in the documentation enclosed with the software kit
- ☐ for the online programming in **Dolog B** in appendix A, e.g., in point A.2 of this manual.

You will also find information about entering the I/o equipment in section 3.10.1.

3.10 Further Information

3.10.1 Information to Enter the Equipment in the Equipment List

There is an area in which 32 bits are assigned to each slot reference in the signal memory. The process image with which the processor operates is saved here. The signals are first handed on from the signal memory to the output modules at the end of the program; the entries into the signal memory are then carried out from the entry modules.

The A500 must therefore get to know the I/O equipment via an equipment list. You have to indicate which BIK is responsible for which subrack with subracks with front connection. Subracks, the presence of which is not made known to the A500, generally cannot be processed by the program. The equipment list is to be created in the following way:

- ❑ via the **EQL Bsdol function** with online programming on Dolog B. This is described in detail in the user manual for the Bsdol functions. Figure 53 also shows an example for the use of the EQL function.
- ❑ via the **A list** with offline programming in Dolog B. The equipment list is generated from the A list during the compilation. The editing of the A list is described in the documentation enclosed with the software kit.
- ❑ via the **"Editing" and "Equipment list" menu points** with offline programming in Dolog AKF. The editing of the list is described in the documentation enclosed with the software kit.



Note Certain I/O modules may not be entered in the EQL list. The following points are valid depending on the type of programming (more information can be found in the documentation of the EQL list or the software kits):

The following is valid for the **online programming**:

I/O modules with rear connection are only entered in the EQL list if it is a question of binary I/O modules or the DKU 022.

The following is valid for the **offline programming** with Dolog AKF or Dolog B:

The entry of the affected I/O modules is prevented by the AKF software or by the EQL function. The I/O modules can be entered in the A list with offline Dolog B (since the A list is also required to document the I/O equipment), but the transfer of these modules from the A list is suppressed when the equipment list is generated.

Example for the Equipment:

❑ **SES 002**

(Spontaneous input module with 16 inputs), first secondary subrack, PEAB slot reference 17

❑ **SES 002**

(Spontaneous input module with 16 inputs), first secondary subrack, PEAB slot reference 18

❑ **DAP 102**

(I/O module with 16 outputs and 16 inputs) is located in the DTA 101 primary subrack, first slot next to the DEA 106. The DEA is set here to address 33 and is supplied by the first BIK.

Entering the EQL List (Dialogue):

```
DOLOG B:BES
*** I/O-Occupancy list, V3.1 ***
BITBUS inactive
1: Delete list area from ... to      2: Display list area from ... to
3: Display or change list elements   4: Delete error messages
5: Error diagnosis                  6: Initialize
7: Trace funktion                   8: Special functions
9: Expert funktion
H: Help funktion                    E: Return to DOLOG
Input: 3
Address (1...160):17
  17A -                               New: 3
  17E -                               New:
  18A -                               New: 3
  18E -                               New:
  19A -                               New: N
Address (1...160): 33
  33A -                               New: DAP102 F4 1 1
  33E DAP102      F4 1 1
  34A - ?? -      F4 2 1              New: N
Address (1...160): E
Input: E
Initialization in progress....
Initialization completed without errors

DOLOG B:
```

Figure 53 Example of a EQL List Entry

If the PEAB addresses which are defined as equipped in the EQL list do not have a background of hardware, this leads to an I/O bus time error (PEAB time error) and to an extension of the running time for the VList.

3.10.2 PEAB Time Error

If an empty PEAB slot is entered as equipped in the EQL list or a PEAB module fails, a PEAB time error is registered via an interrupt for each futile attempt at access (e.g., with the END block). Marker 21 and/or marker 31 is set here to 1 (see special marker area). The last faulty PEAB address is saved in word 9.

The following is valid here:

- <9> = Slot reference with a malfunction on row O
- <9> = Slot reference + 1000 with a malfunction on row I

3.10.3 Watchdog Display - Signal Relay - Marker 60

The watchdog display registers the correct operation of the system with a applied signal relay. The relay drops out with

- undervoltage of the voltage to be monitored
- stationary VList
- running VList but any group error, i.e., marker 60 = 1
- running VList but an access of the permitted cycle time

Marker 60 can be affected by the user program (VList). If it is set to “1”, the signal relay drops out, and the watchdog display goes out.



Note Marker 60 is not standardized with the start of a VList, i.e., it is to be ensured that it has valency 0 for the initial start-up. Marker 60 can also be saved with the SY-KON Bsdol function just like any other bit.

3.10.4 Setting the Transmission Rate with the Software

The transmission rate for the UKA interface can be altered after the A500 has been switched on, This is done by altering the contents of word 71.

The hardware setting on the UKA is valid again after switching the A500 off and on again and after Reset or HE, if the “set” ALU pin is plugged in.

Table 26 Dependency of the Transmission Rate on the Contents of Word 71

Contents of Word 71	Transmission Rate
0	110
1	300
2	1 200
3	2 400
4	9 600
5	19 200

If the transmission rate of the UKA is altered, the transmission rate of the connected programming panels or operating devices must be adapted to it. In order to do this for the programming panels you must leave the called up program and restart (maximum: 9 600 baud). The respective status line must be adapted for the operating devices (e.g., DSG 110) (maximum 19 200 baud, see relevant description).

3.11 Documentation and Archiving

You can create and archive the complete documentation after the test has finished. The following belong to the documentation:

- Hardware settings
- User program with additional information

3.11.1 Documentation of the Hardware Settings

Documentation aids are available for the documentation of the hardware settings.

Documentation Aids

Documentation aids are DIN A3 forms. They serve the planning, configuration and documentation of the hardware (modules, devices) of the programmable controller with German/English entries specific to the modules, such as:

- Type designation of the hardware
- Terminals
- Plug designations
- Protective circuits and explanations of the jumpers determining the functions, etc.

The A3 forms are divided into 6 blocks with the following contents:

- A500 controller form block (1), ordering code A91V.12-234 720. It includes:

General	ALU 150	ALU 286	ALU 821	BIK 812
COP 82	DBK 021	DKV 023	KOS 882	MPV 003
SC 8256	SF 8128	SF 8512	UKA 024	UVL 84x
- A500 controller form block (2), ordering code A91V.12-234 721. It includes:

DNO 028	DNP 023	DNP 023-1	DNP 023-3	DNP 028
SAE 2	DTA 024	DTA 027	DTA 27.1	DTA 028
DTA 101	DTA 107	SCHWRA	SCHR-KL	KSB 1
- SFB I/O form block, ordering code A91V.12-234 787. It includes:
 - I/O modules and subracks with front connection
- PEAB I form block, ordering code: A91V.12-234 722. It includes:
 - binary input modules with rear connection
 - DKV 022, DNP 025, DTA 025, in preparation: DNP 026
- PEAB O form block, ordering code: A91V.12-234 723. It includes:
 - binary output modules and subracks with rear connection
- PEAB AS form block, ordering code: A91V.12-234 788. It includes:
 - analogue I/O modules with rear connection
 - intelligent function modules with rear connection

These forms are also available as a Ruplan data file (Technical Sales Office version).

The forms of DAP 104 shown in Figure 54 and Figure 55 convey the type of representation for the protective circuit and for the port for the process peripherals.

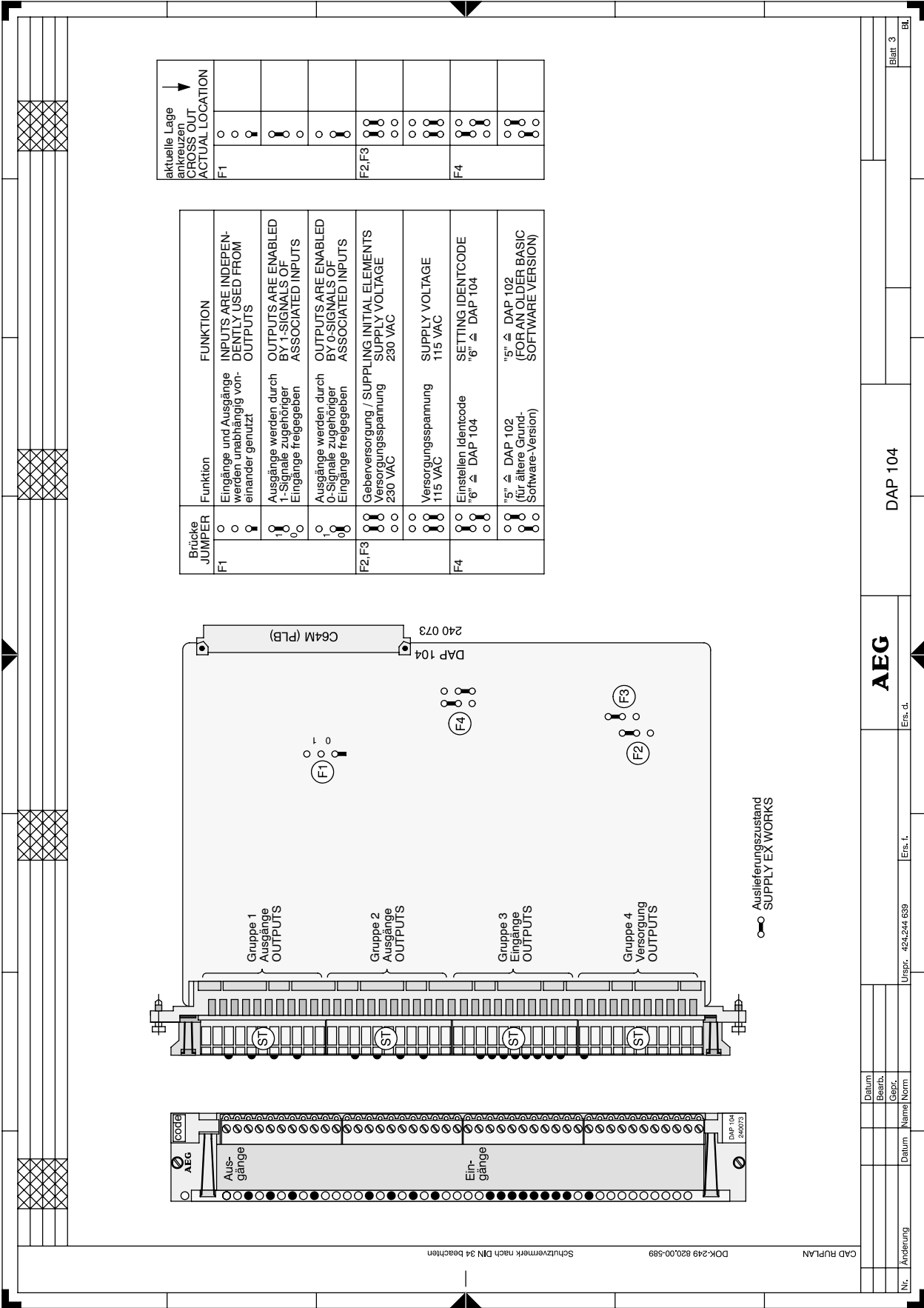


Figure 54 Reduced DIN A3 Form of the DAP 104, Page 1 (Protective Circuits)

3.11.2 Documentation of the User Program with Additional Information

This documentation is saved on a hard disk or diskette and can be output on a printer or screen. It includes the following for Dolog AKF, for example:

- ❑ "Survey" (program structure)
- ❑ "Program log" (user program)
- ❑ "Equipment list" including the specified parameters such as the number of:
 - ❑ Marker bits
 - ❑ Marker bytes
 - ❑ Marker words
 - ❑ Marker double words
 - ❑ Timers
 - ❑ Counters
- ❑ "Cross reference list"
- ❑ "Symbols and comments" (symbols and comments of the hardware addresses, e.g., inputs, outputs, markers)
- ❑ "Signal occupation list" (log of the signals used in the program)
- ❑ "Setup station"
- ❑ "Command file"
- ❑ "Contents of the signal memory"

Detailed descriptions can be found with the software kits.

3.11.3 Program Archiving

You can archive the user program with additional information on the following:

- ❑ Diskette
- ❑ Paper (as a print-out)

User programs which are to be archived or duplicated without additional information can also be saved on EPROMs.

- ❑ when using the ALU 150 on EPROM 27128 type, carrier module: SF 8516
- ❑ when using the ALU 011 on EPROM 27128 type, carrier module: ALU 011
- ❑ when using the ALU 061 on EPROM MME 001 module, carrier module: ALU 061

The user programs saved in this way can be restored completely (with line comments, network comments, parameter symbols and labels) in AKF (depending on the link mode).

For a detailed description, see the slip case of the "Dolog AKF → A350/A500" diskettes, "Linking programs" section (link mode).

Chapter 4

Specifications

All the specifications regarding the A500 according to VDI guideline 2880 Bl.1 are summarized in this chapter.

- ▣ User Program
- ▣ Power Supply Interface
- ▣ Process Interfaces
- ▣ Data Port
- ▣ Processor
- ▣ Memory
- ▣ Processing Times
- ▣ Physical Characteristics
- ▣ Environmental Characteristics

Specifications

4.1 User Program

Control instructions	<ul style="list-style-type: none"> □ Logic operations, comparisons, saving, controlling □ Times: 80 ms ... 32767 s □ Counting: forwards/backwards via software blocks □ Data transport and organization □ Fundamental arithmetic operations □ New value, initial value signals □ Analogue measurand processing □ Operating time system □ Sequence control system □ Mass flow, filler register, shift register □ Tesy text system (logs, diagnosis, dialogue) □ Networking for A500 ↔ A130, A350, A500, B500 (color video system) and program transfer, binary value transfer and digital value transfer, remote operation
Programming language	<p>Dolog B (block technic)</p> <p>Dolog AKF (instruction list, ladder diagram, function block diagram according to DIN 19 239)</p>
Programming	
□ Programming panels	P125, P300, P510, P610. For more details, see chapter 1.6.2
□ Video terminals	e.g., DEC VT 320 or a compatible device
Archiving the User Program	
□ on diskette relevant software	<p>with a programming panel: P125, P300, P510, P610</p> <p>Archive→A350/A500</p> <p>Dolog AKF→A350/A500</p> <p>Dolog B→A350/A500</p>
□ on EPROM	<p>with EPROM programming station</p> <p>EPS 2000 or EPS 386</p>

4.2 Interfaces

4.2.1 Supply Interface Mains Supply

- Controller modules $U_E = 24 \text{ VDC or } 230 \text{ VAC}$
- I/O with front connection $U_E = 24 \text{ VDC}$
- I/O with rear connection $U_E = 24 \text{ VDC for DNP 026, } U_E = 230 \text{ VAC for DNP 025}$

Operating Voltage

- Voltage limits $U_B = 24 \text{ VDC (nominal value)}$
 $20 \dots 30 \text{ VDC}$
- Periodic peak values $18 \dots 33 \text{ VDC (including ripples)}$
max. 5 % effectively or max. 16 % SS
→ relative vibration length according to DIN 40 110
(three-phase jumper without filtering is permitted)
- Ripples
- non periodic peak values max. 35 VDC for $t < 500 \text{ ms}$
max. 45 VDC for $t < 10 \text{ ms}$
- Reference potential of U_B M (M2)

Current input¹³⁾ for modules see chapter 4 (Specifications) of the relevant module description

Permitted mains system voltage dips $< 1 \text{ ms}$, repetition after 1 s at the earliest

Overvoltage protection see page 19

4.2.2 Process Interfaces

4.2.2.1 Configuration Limits

Structure with Front Connection

- Number of BIK for I/O max. 3
- Number of DEA xxx max. 16 per BIK
- Number of addresses max. 159. DEA-H1 and DEA-K1 need
(number of I/O modules) 2 addresses each
- Number of I/O points max. 5088

Structure with Rear Connection

- Secondary subracks max. 9 DTA 025
- Number of addresses max. 159
(number of I/O modules)
- Number of I/O points max. 5088

Mixed Structure

- Number of addresses max. 159
(number of I/O modules)
- Number of I/O points max. 5088

¹³⁾ The supply of the sensors and the working voltage for the actuators is described in 4.2.2.2 and 4.2.2.3.

4.2.2.2 Inputs

The most important information about the input modules¹⁴⁾ which can be used for A500 are summarized in the following table. Details, such as, e.g.,

- port
- for analogue inputs: accuracy and errors,

are explained in chapter 4 of the individual module descriptions

Table 27 Specifications for Binary Inputs

	DEP 112	DAP 102	DAP 103	DAP 104
Number of inputs	4x8 I	2x8 I	2x8 I	1x8 I
Type of networking	potential-free (optical coupler)	potential-free (optical coupler)	potential-free (optical coupler)	potential-free (transformer)
Sensor supply	U _B = 24 VDC	U _B = 24VDC	U _B = 24 ... 60 VDC	L = 115 / 230 VAC
Signal level				
- 1 signal	+12 ... +30 VDC	+18 ... +30 VDC	+18 ... +75 VDC	97 ... 127 VAC / 187 ... 250 VAC
- 0 signal	-2 ... +5 VDC	-2 ... +5 VDC	+2 ... +5 VDC	0 ... 45 VAC / 0 ... 90 VAC
Input current	7 mA for 24 VDC 8.5 mA for 30 VDC	7 mA for 24 VDC 8.5 mA for 30 VDC	5.5 mA for 24 VDC 7.5 mA for 60 VDC	10 mA for 115 VAC 16 mA for 230 VAC
Indicators	1 LED per input, 1 LED per group for sensor supply	1 LED per input, 1 LED per group for sensor supply	1 LED per input, 1 LED per group for sensor supply	1 LED per input

Detailed information about the limits can be found in chapter 4.2.1.

Table 28 Specifications for Analogue Inputs

	ADU 115 / DAU 104	ADU 116
Number of inputs	16x2 pole or 8x4 pole in 4 groups each with ADU 115 8x2 pole or (4x4 pole and 4x2 pole) with DAU 104	4x4 Inputs
Measuring range		
- Current	-1 ... +1 mA, -10 ... +10 mA, -20 ... +20 mA	-20 ... +20 mA, unipolar and bipolar
- Voltage	-0.05 ... +0.05 V, -0.5 ... +0.5 V, -1 ... +1 V, -5 ... +5 V, -10 ... +10 V	-10 ... +10 VDC, unipolar and bipolar
- Temperature above PT 100	-99.2 ... +100 °C, -200 ... +300 °C, -200 ... +600 °C, -200 ... +850 °C	-
- Resistor	1 ... 1000 ohm	-
Conversion time (per input)	22.5 ms with 50 Hz noise suppression and 2 pole port 19 ms with 60 Hz noise suppression and 2 pole port 25 ms with 50 Hz noise suppression and 4 pole port 21.5 ms with 60 Hz noise suppression with 4 pole port	1.6 ms for 16 values
Resolution of the transformer	13 bits including sign	11 bits including sign
Assignment to the resolution	maximum basic measurand = 100% → +4000 minimum basic measurand = 100% → -4000	max. basic measurand = 100% → +1000 max. basic measurand = 100% → -1000
Indicators	1 LED for supply voltage 1 LED for ready	1 LED for supply voltage 1 LED for ready

14) The electrical data of the input modules with front connection are listed in the following. The corresponding data of the modules with rear connection can be found in the relevant module descriptions and in the A500 catalogue.

4.2.2.3 Outputs

The most important information about the output modules¹⁵⁾ which can be used for A500 are summarized in the following table. Details, such as, e.g.,

- port
 - for semi-conductor outputs: properties of the semi-conductor outputs, switching capacity for incandescent lamps, signal level
 - with relay contacts: lifetime of the relay contacts, operating frequencies, protective circuits, minimum current
 - with analogue outputs: accuracy and errors,
- are to be found in chapter 4 of the individual module descriptions.

Table 29 Specifications for Binary Outputs

	DAP 102	DAP 103	DAP 104	DAP 106	DAP 112
Number of outputs	2x8 outputs	2x8 outputs	8 outputs	16 outputs	4x8 outputs
Design of the outputs	Semi-conductors	Relay contacts	Relay contacts	Relay contacts	Semi-conductors
Type of networking	potential-free (optical coupler)	potential-free (transformer)	potential-free (transformer)	potential-free (transformer)	potential-free (optical coupler)
U _s working voltage	24 VDC	24 ... 60 VDC / 24 ... 230 VAC	24 ... 60 VDC / 24 ... 230 VAC	24 ... 60 VDC / 24 ... 230 VAC	24 VDC
Load current	10 mA ... 2 A				10 mA ... 0.5 A
- 24 VDC, ohmic load		max. 2 A perm.	max. 2 A perm.	max. 2 A perm.	
- 230 VAC, cos phi = 1		max. 2 A perm.	max. 2 A perm.	max. 2 A perm.	
- 230 VAC, cos phi = 0.5		max. 1 A perm.	max. 1 A perm.	max. 1 A perm.	
permitted total current	8 A per group	6 A per group	16 A per group	32 A per module	2 A per group
Operating delay	<1 ms	approx 10 ms	approx. 10 ms	approx. 10 ms	<1 ms
Indicators	1 LED per output, 1 LED per group for working voltage 1 LED per group for overload	1 LED p. output, 2 LEDs f. supply of relay coils	1 LED p. output, 1 LED f. supply of relay coils	1 LED per output, 2 LEDs for supply of relay coils	1 LED per output, 1 LED per group for working voltage 1 LED per group for overload

Detailed information about the limits can be found in chapter 4.2.1.

Table 30 Specifications for Analogue Outputs

	DAU 104	DAU 108
Number of outputs	4 outputs, 2 pole	2x4 outputs
Ranges		
- Current output	-1 ... +1 mA, -2 ... +2 mA, -5 ... +5 mA, -10 ... +10 mA, -20 ... +20 mA	-20 ... +20 mA, unipolar and bipolar
- Voltage output	-0.5 ... +0.5 V, -1 ... +1 V, -2.5 ... +2.5 V, -5 ... +5 V, -10 ... +10 V	-10 ... +10 VDC, unipolar and bipolar
Conversion time	max. 20 ms per output	0.8 ms for 8 values
Resolution of the transforme	13 bits including sign	11 bits including sign
Assignment of the resolution	maximum basic measurand = 100% → +4000 minimum basic measurand = 100% → -4000	max. basic measurand = 100% → +1000 max. basic measurand = 100% → -1000
Indicators	1 LED for supply voltage 1 LED for ready	1 LED for supply voltage 1 LED for ready

¹⁵⁾ The electrical data of the output modules with front connection are listed in the following. The corresponding data of the modules with rear connection can be found in the relevant module descriptions and in the A500 catalogue.

4.2.3 Data Interface

4.2.3.1 RS 232 C (V.24) Programming Interface

Use	Connecting UKA 024 or ALU 0x1 and the programming panel (PADT)
Connector pin assignment	according to DIN 66 020, page 1 or EIA RS 232C; see also the module descriptions for UKA 024 and ALU 0x1
Transmission rates	110, 300, 1200, 2400, 9600, 19200 baud (bits/s), adjustable with jumpers on UKA and ALU
Data format	1 start bit 7 data bits, ASCII (7 bits per character) 1 parity bit, even parity 1 stop bit
Voltage level	according to 66 020
Inputs	1 signal <-3 VDC; 0 signal >+3 VDC
Outputs	1 signal <-5 VDC; 0 signal >+5 VDC

4.2.3.2 Communications Port (RS 232 C / Current Loop / Telecontrol Mode)

Use	Connecting KOS to its communication partner
Type of transmission	Modnet 1/N or Modnet 1/F
Transmission medium	Telecommunication cable
Transmission	with acknowledgement and broadcast
Bus arbitration	Master-Slave
Error immunity	HD = 4, longitudinal parity and vertical parity
Error correcting	by repetition
RS 232 C	
Connector pin assignment	according to DIN 66 020, page 1; or EIA RS 232 C see also the module description for KOS 152
Transmission rates	up to max. 19 200 bits/s; adjustable using the software
Voltage level	according to DIN 66 020
□ Inputs	1 signal <-3 VDC; 0 signal >+3 VDC
□ Outputs	1 signal <-5 VDC; 0 signal >+5 VDC
Current Loop	
Connector pin assignment	see the module description for KOS 152
Current level	20 mA, active/passive
Transmission rates	up to max. 9 600 bits/s; adjustable using the software
Telecontrol Operation	
Terminal assignment	see the module description for KOS 152
Transmission rates	see the module description for KOS 152

4.2.3.3 RS 485 Communications Port (Modnet 1/SFB)

Use	<ul style="list-style-type: none">□ Connection to the distributed inputs/outputs□ Networking with other programmable controllers
Connector pin assignment	according to RS 485; see the module description for BBS 1, chapter "Connector pin assignment"
Type of transmission	<ul style="list-style-type: none">□ Symmetrically serial, isolated□ Transmission with acknowledgement and broadcast□ Bus arbitration: Master-Slave□ Block transmission up to 20 bytes□ CRC mark of conformity□ Error correcting through repetition
Protective circuit	between 0 V and chassis (PE) with 100 kΩ, varistor and capacitor
Transmission rates	62.5 kbits/s, 375 kbits/s, 2 Mbits/s; see also chapter 4.6.2 "Permitted line lengths"
Cable termination	both sides 120 Ω
Number of nodes	max. 28
Permitted slave addresses	126

4.2.3.4 PMB (Parallel Microprocessor Bus)

Supply voltage	+5 VDC, -3 ... +4%
Data width	16 bits
Address width	20 bits
Plug and socket connectors	C construction according to DIN 41 612

4.2.3.5 PEAB (Parallel I/O Bus)

Supply voltage	+12 VDC, -12 VDC, ±5%
Data width	16 bits
Addressing	Slot references, subaddresses and DKC addresses
Plug and socket connectors	C connection according to DIN 41 612

4.2.3.6 PAB 1 (Parallel System Bus)

Use

Internal I/O bus for the DTA 112 and DTA 113 subracks. The data traffic is initiated by the "Busmaster" ALU or DEA 116, and the information transmitted from it to the "Slave" process peripheral modules or vice versa.

Supply voltage	+5 VDC, ±5%
Supply indicator	green LED on DEA 116
Max. permitted current input	7.6 A per subrack for I/O nodes
Address capacity	8 192
Data width	8 bits
Addressable nodes	max. 9
Interrupt level	1 (group interrupt)
Ready message	1
Transmission cycle time	approx. 1 μs for 1 byte, (depending on the bus master)
Plug and socket connectors	C construction according to DIN 41 612

4.2.3.7 PLB (Parallel Local Bus)

Use

Internal I/O bus for the subracks: DTA 101 (righthand half), DTA 102, DTA 103, DTA 112 and DTA 113. The data traffic is initiated by the "Busmaster" ALU or DEA 106 / DEA 156 and the information transmitted from it to the "Slave" process peripheral modules or vice versa. The PLB is only different from PAB 1 in the fact that it has a lower current input.

Supply voltage	+5 VDC, $\pm 5\%$
Supply indicator	green LED for DEA 106 and DEA 156
Max. permitted current input	
□ for DEA 106	0.8 A per subrack for I/O nodes
□ for DEA 156	3.6 A per subrack for I/O nodes
Address capacity	8192
Data width	8 bits
Addressable nodes	max. 9
Interrupt level	1 (group interrupt)
Ready message	1
Transmission cycle time	approx. 1 μ s for 1 byte, (depending on the bus master)
Plug and socket connectors	C construction according to DIN 41 612

4.3 Processor

Type	8086 word processor on ALU 150 80C186 word processor on ALU 011 80386 word processor on ALU 061
Word length	16 bits
Data processing	word-/double word-wise with process image, floating point processing with MAT 827 for ALU 150, 80C187 arithmetic processor on ALU 011 and 80387 arithmetic processor on ALU 061
Operating modes □	Cold restart (with initial state characteristics) or warm restart (initial state characteristics or non-volatile characteristics) □ Manual or automatic start
Monitoring	□ Monitoring the supply voltage for undervoltage or supply failure □ Program memory monitoring for data contents with a cyclical test with marks of conformity □ Time monitoring of the running program □ Monitoring the rechargeable battery for undervoltage □ Monitoring the signal memory for data contents at the time when the device was switched on □ Constant monitoring of the outputs for short-circuit and overload □ Time monitoring of the Modnet 1/SFB telegrams □ Insertion check of the PEAB modules

4.4 Processing Times

see chapter A.7 "Cycle time"

4.5 Memories

4.5.1 Signal and System Memory

Type of memory	32 kb RAM, (16 x 16 k / 1 bit), 2 kb of which can be addressed bit-by-bit, battery-backed via rechargeable battery
Carrier module	ALU 011, ALU 061 or ALU 150
Inputs/outputs	max. 5088 I/O points
Marker bits	10 000
Marker words, -double words, marker floating point words	adjustable from 100 to 10 000 ¹⁶⁾ , basic setting: 500
System markers	1 ... 100 (bit) 1 ... 100 (word, double word, floating point word)

4.5.2 Memory for the Basic Software

Type of memory	4 x 128 kb EPROM (segments 17 ... 32), for console functions, I/O routines, operating functions, Dolog B blocks, etc.
Carrier module	ALU 011, ALU 061 or ALU 150

4.5.3 Memory for the User Program

Type of Memory	
RAM	C-MOS elements, battery-backed
EPROM	EPROM elements, 128 kbytes each
Carrier Module	
RAM	ALU 011, ALU 061; for ALU 150: SC 8128, SC 8256
EPROM	ALU 011, ALU 061; for ALU 150: SF 8512
Capacity	
A500 with ALU 0x1	3 x 128 kb RAM ($\hat{=}$ segments 5 ... 16); segments 9 ... 16 can be converted to EPROM block-by-block (128 kb)
A500 with ALU 150	6 x 64 kb RAM ($\hat{=}$ segments 5 ... 16); segments 9 ... 16 can be equipped with EPROM block-by-block (64 kb)

¹⁶⁾ The number of double words and floating point words are counted as double for the summation.

4.5.4 Backup Rechargeable Battery

Carried ot PMB	to back up the RAM of the ALU, BIK, KOS, SC
Voltage (when idling)	3.6 V
Capacity	1.8 Ah

Operational Duration

at 20 °C	typically > 10 years, at least 5 years
at 50 °C	typically > 5 years, at least 2 years

Backup Duration With max. Capacity

at 0 °C	typically 7.5 months, at least 16 days
at 20 °C	typically 2.8 months, at least 13 days
at 40 °C	typically 1.2 months, at least 10 days

Storage duration	at least 5 years, typically > 10 years at -40 ... +70 °C
Undervoltage indication	through LEDs on ALU 0x1, UKA 024

4.6 Physical Characteristics

4.6.1 Design Data

Construction	INTERMAS, 19 inches
Format	(1 HE = 44.45 mm; 1 T = 5.08 mm)
<input type="checkbox"/> Controller	6 HE, 84 T
<input type="checkbox"/> Secondary subrack with front connection	6 HE, 40 T for DTA 102, DTA 112 or 6 HE, 84 T for DTA 103, DTA 113
<input type="checkbox"/> Secondary subrack with rear connection	6 HE, 84 T for DTA 025
<input type="checkbox"/> for modules	6 HE, 4 T / 6 HE, 8 T / 6 HE, 12 T (double Europe format according to DIN 41 4949)
Safety type according to DIN 40 050	IP 00
Operating position	vertical, aperture plates for the air circulation at the top and bottom
Ventilation	natural convection
Weight	see module descriptions

4.6.2 Permitted Line Lengths

Inputs and outputs (binary)	max. 400 m unshielded, max. 1000 m shielded
Inputs and outputs (analogue)	max. 100 m, twisted as pairs, shielded, reference conductor carried as well
RS 232 C (V.24)	max. 20 m shielded, max. permitted cable capacity ≤ 2.5 nF
RS 485 (Modnet 1/SFB)	max. 30 m for 2 Mbits/s (MBd) max. 300 m for 375 kbist/s (kBd) max. 1200 m for 62.5 kbits/s (kBd) Cable: Four wires or two wires (only four wires for 2 Mbits/s), twisted as pairs and shielded, ripple resistor 120 Ω /10 km for 10 kHz
Current loop	max. 1000 m shielded

4.6.3 Connection Mode Supply

□ DTA 101 (mains supply)	12 pole terminal block for a line cross-chapter of 0.25 ... 2.5 mm ²
□ DTA 107 (mains supply)	Terminal block for a line cross-chapter of 3x1.5 mm ² (VAC) or 2 x 2 x 2.5 mm ² (VDC)
□ DNP 02x, DNO 028	15 pole plug connector (H15M)
□ BIK 151, KOS 152	2 pole screw/plug-in terminal for a line cross-chapter of 0.25 ... 2.5 mm ²
□ DEA 106, 116, 156	11 pole screw/plug-in terminals for a line cross-chapter of 0.25 ... 2.5 mm ²

Inputs and Outputs

□ Front connection	11 pole screw/plug-in terminals for a line cross-chapter of 0.25 ... 2.5 mm ²
□ Rear connection	48 pole plug connector (E48M) according to DIN 41612 for MDL 48, MDL 48L
□ PEAB	64 pole socket connector (C64M) according to DIN 41 612 for modules, MDL 66.1, MDL 67
□ RS 232C (V.24)	25 pole socket for data cable YDL 14.1 (video terminal) or data cable YDL 37 with YDL 44 (programming panel)
Modnet1/SFB (RS 485)	9 pole socket for BBS 1 connector
Modnet 1/N, 1/F	25 pole according to DIN 66 020 for a current loop / RS 232 C
Modnet 2/NP (modem output)	KOAX socket, 10 mm (IEEE 802.4)

Creepage Distances and Clearances

□ Peripheral ports (screw/plug-in terminals)	according to VDE 0110, group C for 250 VAC
□ distances between circuit-board conductors	according to VDE 0110, group A

4.7 Environmental Data

4.7.1 Climatic (According to DIN 40 040, Page 1/6.70)

permitted ambient temp. for the operation acc. to KY category (operation without a fan)	\square ... +50 °C air inlet temperature ¹⁷⁾ without ADU 116, DAU 108, I/O with rear connection I/O \square ... +40 °C air inlet temperature ¹⁷⁾ with ADU 116, DAU 108, I/O with rear connection I/O
permitted ambient temp. for the operation acc. to KV category	0 ... +55 °C intake air
permitted storage temp. according to GP category	-40 ... +85 °C (without a battery) -40 ... +70 °C (with a battery)
relative humidity according to F category	75% in the middle of the year, without dew 95% on 30 consecutive days per year 85% on remaining days, occasionally
Air pressure	≥ 70 kPa (700 mbar) during operation or storage, ≥ 23 kPa (230 mbar) for transport

4.7.2 Mechanical (Shocks and Vibrations)

Impact load (shock load) according to DIN/IEC 68 part 2-27	30 g \rightarrow 294 m/s ² for 18 ms (test condition: 3 impacts per axis and direction)
Vibration load according to DIN/IEC 68, part 2-6	0.15 mm amplitude (single) for 10 ... 55 Hz 2 g \rightarrow 19.6 m/s ² for 55 Hz (test condition: 10 cycles, fre- quency alteration of 1 octave per minute)

17) The power dissipation of the module (given in the specifications of the corresponding module description) is to be taken into account with more difficult ventilation conditions.

4.7.3 Electrical

Static limits see chapter 4.2.1

Test voltage (dielectric strength) according to VDE 0160, issue 05.88

Electromagnetic Compatibility (EMC)

Noise immunity for interference carried by lines see Table 31

Noise immunity against electrostatic discharge according to IEC 801-2 5 kV (peak)

Noise immunity against electromagnetic fields based on IEC 801-3 10 V/m

Current impact via chassis 1 kA with 1 MHz basic frequency, reducing, saved energy: 0.94 J

Radio interference suppression acc. to VDE 0871 (for power supplies with 230/380 VAC or 24 VDC) Limit category A. Limit category B is observed with an additional filtering of the power supply with a interference suppression filter, e.g., from Messrs. Eichhoff, AZ 711 or AZ 712 type in accordance with the "General permit according to the gazette 1046/84".

Table 31 Noise Immunity for Interference Carried by Lines

Circuits	Impact voltage test acc. to ¹⁸⁾ IEC 255-4, VDE 0435 1.2 μ s / 50 μ s	Radio frequency IEC 255-4, VDE 0435 1 MHz	Spike/Burst acc. to test acc. to IEC 801-4 (draft)
24 VDC mains	2.5 kV (peak)	1.0 kV (peak)	2.0 kV (peak)
230 VAC mains	5.0 kV (peak)	2.5 kV (peak)	2.0 kV (peak)
Binary inputs	2.5 kV (peak)	1.25 kV (peak)	1.5 kV (peak)
Analogue inputs	2.5 kV (peak)	1.25 kV (peak)	1.5 kV (peak)
Binary outputs (semi-conductors)	2.5 kV (peak)	1.25 kV (peak)	1.5 kV (peak)
Analogue outputs	2.5 kV (peak)	1.25 kV (peak)	1.5 kV (peak)
Relay outputs	5.0 kV (peak)	2.5 kV (peak)	1.5 kV (peak)

18) without the device in operation

Chapter 5

Earthing and EMC-Measures

This chapter imparts basic knowledge for earthing and electromagnetic compatibility measures.

5.1 Earth Grounding and Earthing (Installation Guidelines)

Basic rules are to be observed for larger structures, the connection of external peripherals and power supplies in order to guarantee an operation free from malfunctions.

The following measures are generally to be carried out when configuring systems:

- ❑ Earth grounding all inactive metal parts, cf. 5.1.1
- ❑ Protective earthing according to VDE 0100, cf. 5.1.2
- ❑ Functional earthing, cf. 5.1.3
- ❑ Reference conductor system, cf. 5.1.4

5.1.1 Earth Grounding All Inactive Metal Parts

Earth grounding is the creation of a conductive connection of all the inactive metal parts of an electrical piece of equipment which may be touched without any danger despite voltage being present in the case of an error (VDE 0160 section 2.22). Toothed lock washers and Cu tape or braid is to be used for the earth grounding. the connections must conduct well, i.e. they must be designed free of lacquer, with a protection against corrosion and with low reactance. A cross-section of at least 16 mm² is required for Cu braid conductors.

5.1.2 Protective Earthing According to VDE 0100 ⊕

The protective earthing prevents too high a touch voltage and is necessary if the voltages supplied to the system or created by the system do **not** suffice the conditions of the functional extra-low voltage with safe isolation according to VDE 0160 (issue 5.88, section 5.5.s).

The required protection is achieved by connecting the central earth ground point coded with ⊕ to a low-resistant green-yellow coded protective conductor terminal (PE) or a protective earth conductor bar with the following cross-section:

- ❑ ≥3.5 mA for leakage currents, e.g., by interference suppression capacitors, PE conductors ≥10 mm² Cu per branch
- ❑ a minimum nominal cross-section of the relevant mains supply for the peripheral port

The protective earthing is to be carried out according to the type of mains present (cf. Figure 56).

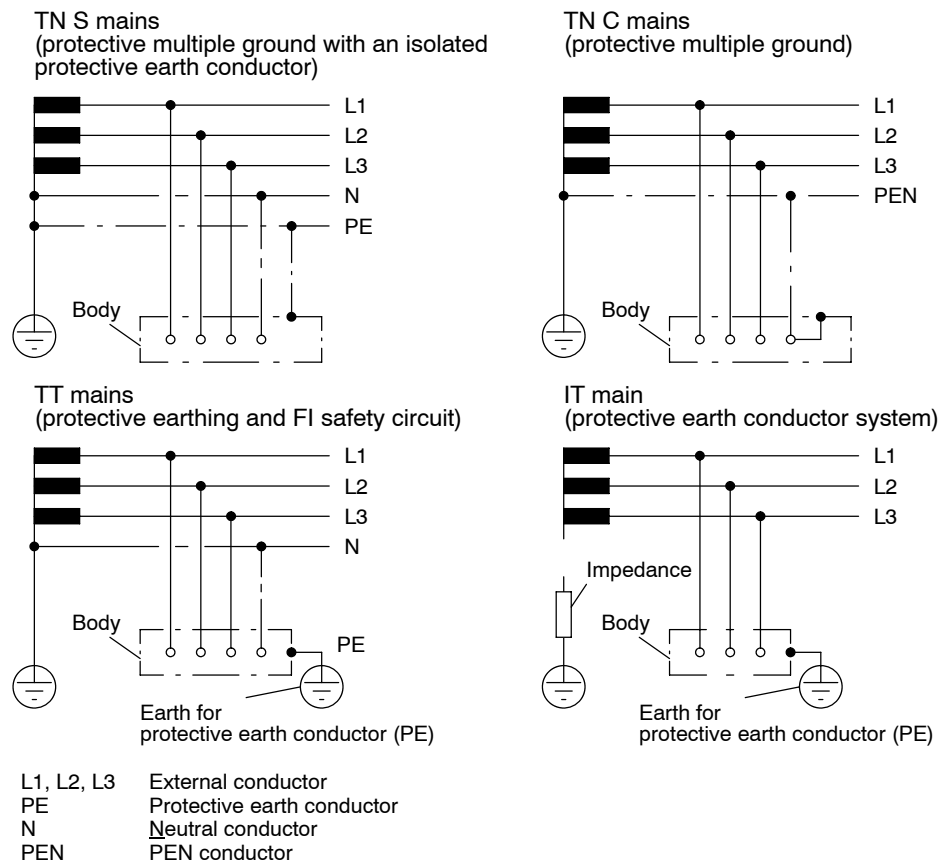


Figure 56 Types of Mains

5.1.3 Functional Earthing

The functional earthing serves to specify the electronic equipment of the reference system to a noise-free earth potential to discharge noise emissions (EMC) and to improve the interference suppression.

Protective earthing and functional earthing are carried together and centrally to the earth ground of the electronic equipment. However, measures for the functional earthing may not remove nor be able to remove the safety measures (even during the start-up).

5.1.4 Reference Conductor System

The reference conductor system is constructed in an isolated way and is connected to a defined point of the earth ground (as short a connection as possible, cross-sectional area of 6 mm²).

The following reference potentials are present in the A500:

- 0V reference potential of the internal electronics
- M1 galvanically isolated input circuits, e.g., of the U_B24 (24 VDC) or >24 VDC supply
- M2 supply of the logic section, supply of the analogue modules supply of the analog modules, supply of the sensors if the inputs are non-isolated
- M4 galvanically isolated U_S24 working voltage

The 0V and M2 potentials are galvanically isolated in the DNP power supplies. The M1 and M4 are also isolated by optical couplers or relays.

All the circuits of the A500 can be operated as potential-free, i.e., without a connection with the functional earth, if the protective circuit measures in section 5.4.2 are observed.

However, a non-isolation is to be created according to the following diagram in order to achieve a high EMC immunity:

❑ **Galvanic Connection of 0V and Earth Grounding in the Primary Subrack**

Check the factory presetting: 4 Z screws tightened, Z jumper in the DTA 101 on the depot slot (right).

The capacitive connection between the subrack earth ground and the 0V of the controllers has a galvanic short-circuit with 4 Z screws. The opened Z jumper (DTA 101 only) activates the capacitive connection between the subrack earth ground and the 0V of the I/O section. There is the possibility to close the Z jumper depending on the application (see Fig. Figure 57).

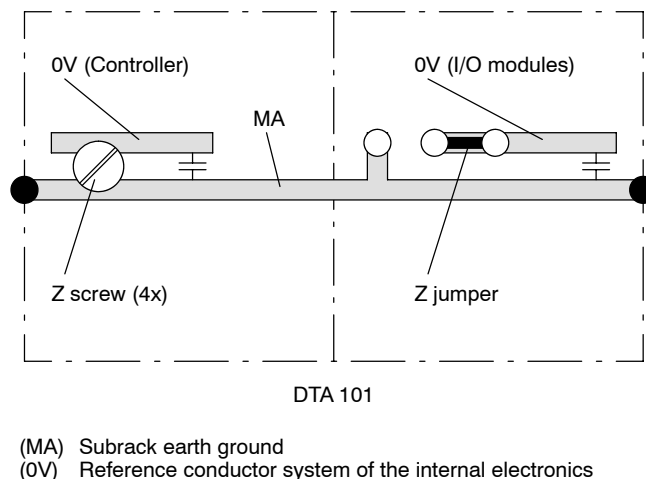


Figure 57 Diagram of the connection of 0V and MA

❑ **Capacitive Connection of 0V and Earth Grounding in the Secondary Subrack**

Check the factory presetting: Z jumper on depot slot (right).

There is the possibility to close the Z jumper (compact structure, short line lengths) depending on the application.

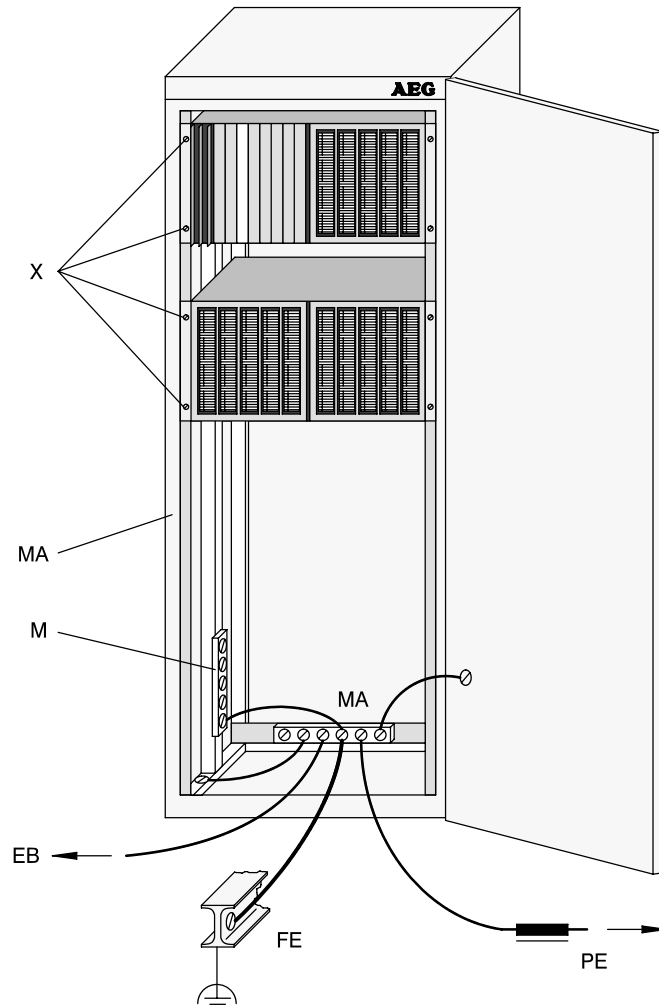
❑ **Connection of M1 and M2 with the Functional Earth.** This connection point preferably lies on the relevant power supply (mutual supply of modules and sensors, see section 3.2.2).

❑ **Connection of M4 with the Functional Earth.** The connection point preferably lies on the power supply for the working voltage. It is recommended to provide isolated power supplies

- ❑ for the supply of the actuators and
- ❑ for the supply of the modules and sensors

(see section 3.2.3).

5.1.5 Earthing System Measures for the Cabinet Structure



- (EB) Neighbouring cabinet/mounting rack
- (FE) Functional earth (environmental potential), e.g., iron carrier of the indoor construction, water line or heating pipe, neutral point of the building earthing system
- (M) Reference conductor system or reference conductor bar (solid copper bar or jumpered terminal block)
- (MA) Earth grounding which is used as a functional earth
- (PE) Protective conductor via a protective earth conductor choke, if necessary
- (X) Screws creating the galvanic connection to MA

Figure 58 Earthing System Measures for the Cabinet Structure

Ensure that the following connections have been created (to achieve the calm potential between the chassis, electronics and noise-free earth):

- the connection between the M reference conductor system and the MA cabinet earth grounding with an RH low-resistent line.
- the connection between the FE functional earth and the MA cabinet earth grounding with a line of a cross-section of at least 6 mm².
- The connection between the PE protective earth conductor and the MA cabinet earth grounding
If the PE protective earth conductor has interference, a protective earth conductor choke, e.g., 20 µH, 16 A; AEG E no. 424 193 199, must be connected in series.
- The connection between EB and MA cabinet earth grounding.

5.2 EMC Measures

5.2.1 Measures for the Installation and Wiring

The following line layouts and shielding measures are to be observed to avoid capacitive and inductive interference for signal lines:

5.2.1.1 Within a Cabinet

Cable Layout

- ❑ Signal lines (low voltages) and heavy current lines may not be laid in a single cable or cable duct (VDE 100, section 42a).
- ❑ Life sections and electronic equipment (EB) are to be installed in an isolated way.
- ❑ The 115/230 VAC Mains cables and signal lines are to be laid in isolated cable ducts at a distance of ≥ 10 cm to the 24/60 VDC signal lines. The arrangement of the cable ducts is to be taken from the following figure. Unavoidable intersections are to be laid as close to right angles as possible.

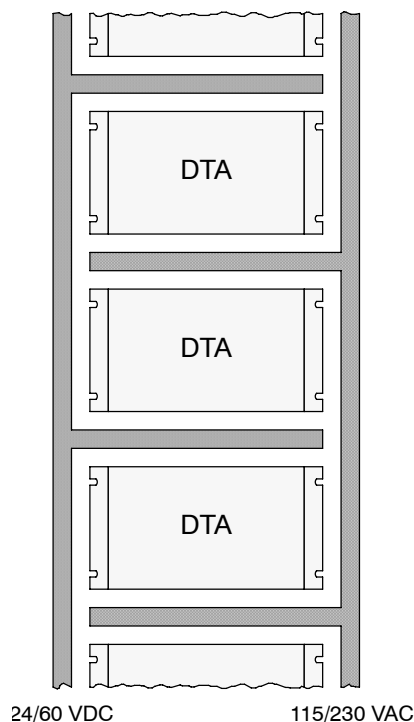


Figure 59 Cable ducts for 24 VDC and 230 VAC lines

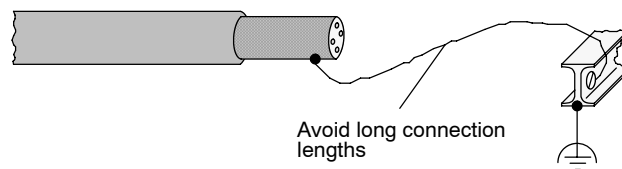
- ❑ Digital signal lines (24/60 VDC) may be laid unshielded in a mutual duct.

- ❑ Shielded bus cables, analogue process data cables and 24/60 VDC signal lines may be laid in a single duct.
- ❑ Isolated, shielded cables ($2 \times 0.5 \text{ mm}^2$, twisted) are to be used for each measured value with analogue process data cables. The shield may generally only be earthed on one side at the cabinet exit.
- ❑ The shields of the system field bus to the nodes (slaves) may not be earthed directly (potential isolation). A capacitive connection is recommended only; see section 3.7.3.2 (page 44).

Mechanical and Electrical Measures

- ❑ A sufficient number of shield terminals (cable earthing bar) is to be provided in the area of the cabinet entry terminals for the shields of in-coming and out-going process cables within and outside the cabinet. A large support is required here.

Wrong:



Correct:

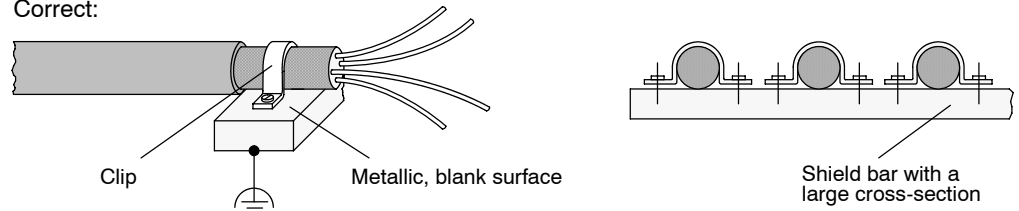


Figure 60 Example for Shield Braid Ports (Mechanics of the Shield Supports)

- ❑ The shield bar is to be connected with the cabinet chassis and the transom (earth ground) and the **central** earthing point in the cabinet as a good conductor.
- ❑ The fixing screws of all the modules are to be screwed down well at all costs (galvanic connection to the earth ground of the subrack). The cable pins must also be screwed tightly with the corresponding sockets.
- ❑ A socket outlet with earthing contact is to be provided for each cabinet group for the connection of programming panels. The protective earth of the socket must be connected to the same PE as the protective earth of the cabinet.
- ❑ Inductivities integrated in the same cabinet which are not directly controlled by the programmable controller (e.g., contactor and relay coils must be wired with suppressor elements (e.g., RC elements, varistors, diodes, etc.); see also section 5.4.1. A partitioning with separating sheet metal is required for the part of the cabinet, in which inductivities (especially transformers, valves and contacts) are installed. The partitioning sheet metal must be connected with the cabinet (earth ground) as a good conductor.

- ❑ The fixing screws of the subracks are to be tightened well at all costs (perfect, galvanic connection to the cabinet earth ground).
- ❑ Conventional fluorescent tubes should not be used for the cabinet lighting for reasons of noise immunity.

5.2.1.2 Outside Cabinets in Closed Buildings

- ❑ Digital signal lines for DC and AC and analogue signal lines must be laid in isolated cables. Use shielded cables (shield conductors with low induction) or filter I/O wires which are especially at risk or provide additional isolation of the peripheral I/O lines with an extreme noise level.
- ❑ Shielded lines are generally to be used for analogue signal lines. A shielded cable (2 x 0.5 mm², twisted) is to be used for each measured value for the connection to the individual sensors or actuators according to the branching. The shielded cable may not be laid together with lines supplying energy or similar electrical sources of interference; the distance must be > 0.5 m.
- ❑ Earthing of the cable shields on one side or both sides
 - ❑ A **single earthing** of the cable shield is necessary for all analogue instrument leads. It is to be used if only capacitive noise effects are expected.
 - ❑ A **double earthing** of cable shields can be necessary for longer signal lines which are subjected to RF effects. A low-resistent **equipotential bonding line** in parallel is necessary for the double earthing. The impedance may amount to a maximum of 10 % of the shield braid resistor.
- ❑ The central processing unit and external operating devices, such as, e.g., video terminal, are connected bit serially via shielded RS 232C data cables, e.g., YDL 052. These cables are to be connected with the earth ground of the devices on both dies via the metallic pin chassis; **tighten the fixing screws.**

5.2.1.3 Outside Buildings

- ❑ Always use shielded cables
- ❑ The shield must be capable of carrying current and connected with the earth on both sides
- ❑ Doubly shielded cables must be used for analogue signal lines, whereby the inner shield is to be earthed on one side only (see above)
- ❑ The signal lines must also be wired with protective elements for overvoltages which are to be provided at the entry point of the cable in the building or at the cabinet at the latest
- ❑ Overvoltage protection for system field bus lines
It is recommended to use an overvoltage protection (lightening ductor) in the remote line to protect the transmission equipment, e.g., Modnet 1/SFB, against overvoltages (lightening). The nominal discharge current should be at least 5 kA here.

5.2.2 Measures for the Power Supply

- Wiring the primary side of power supplies with varistors
- Capacitors with a small capacity and good RF properties in parallel with a possibly present filter capacitor
- Use of transformers with shielding winding and earthing of the shielding winding
- Wiring the secondary side of the power supply with overvoltage limiters, such as suppressor diodes and performance Zener diodes; see section 3.2.
- Filtering the mains voltage for the cabinet supply
Only the use of an interference suppression filter is required to prevent RF interference from the lines into the mains in a normal case for reasons of interference suppression. If greater conducted noise is to be expected in the mains supply, the use of a symmetrical mains filter, e.g., 380 V three-phase current, 50/60 Hz, 4 x 16 A, filter AEG E-No. 424 147 254, is recommended.

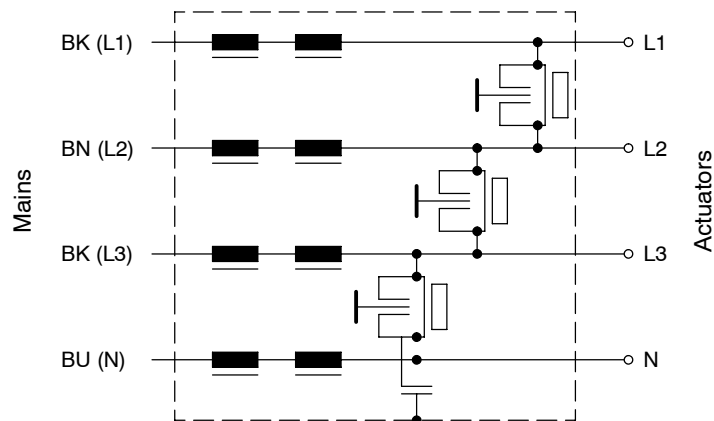


Figure 61 Circuit Diagram of a Mains Filter for Three-Phase Current

5.2.3 Measures Against Direct Noise Interference

Accommodating the electronic equipment in an enclosed chassis/cabinet made from steel sheet. The conventional periphery, e.g., coupling relays, contacts, switches, etc., is to be accommodated in a separate cabinet/chassis, if these do not serve the supply or monitoring. A chassis partitiant with partitioning sheet metal can be used as an alternative. See also section 5.2.1 "Measures for the installation and wiring within a cabinet".

5.2.4 Measures for the Sources of Interference

- A protective circuit of the inductivities is to be recommended for reasons of noise immunity (see section 5.4.1)
 - with clamping diodes for DC
 - with RC elements or varistors for AC / three-phase current
- Filtering the connection lines for AC; see section 5.2.2 "Measures for the current supply" (filtering the mains voltage)
- Partitioning external interference with earthed (MA) steel sheets if electronic equipment must be installed in the area of interference.

5.3 Interference Suppression

Individual components and partial systems which cannot be operated on their own are not subject to the commitments from the German Federal Post Office to produce evidence or the mark of approval according to the law for radio frequency devices.

The components of the A500 have interference suppression according to VDE 0871 limit category A so that an entire system erected with the components generally suffices this condition and observes the configuration guidelines. A prerequisite here is that all the devices and components acquired subsequently also have this degree of interference suppression and that the operating regulations for the interference suppression are observed, such as.

- Filtering the mains voltage with interference suppression filters (cf. 4.7.3)
- Discharging the interference by interference suppression capacitors (RC elements, cf. 5.4.1)
- Protective circuits of inductive actuators with clamping diodes (suppressor diodes) in order to prevent radio frequency interference voltages penetrating neighbouring lines (cf. 5.4.1)

It can happen that so-called general permits are requested. The general permit for the entire system can be obtained by the **user** at the local measuring point for interference suppression. It is generally relevant for systems in residential and mixed areas, authorities, hospitals and airports but not for within industrial areas. If problems should arise as far as the general permit is concerned, you should contact the company which set up the system. In cases of doubts he can contact.

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5.4 Technique of Peripheral Ports

5.4.1 Protective Circuits for Actuators

A protective circuit for the inductivities is to be recommended for reasons of noise immunity. Safety diodes are provided on the output modules to protect the **DC** electronic outputs (semi-conductors). However, these diodes do not offer any interference suppression for long lines.

If conventional contact elements are located in the output lines, e.g., for protective logic and safety interlocks, the contact elements must also be wired with clamping diodes (directly at the inductivity) (cf. Figure 35 and Figure 37).

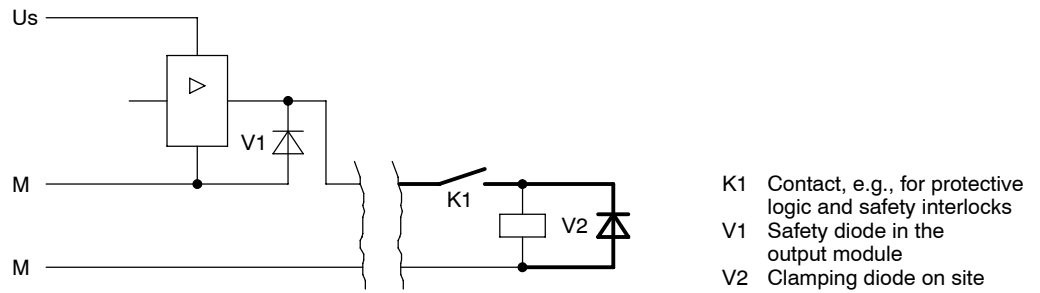


Figure 62 Wiring Inductive Contact Elements

Inductive **AC** actuators are to be wired directly at the inductivity, e.g., with interference suppression capacitors (RC elements) for the same reasons (see also Fig. Figure 36).

5.4.2 Wiring the Reference Conductor in an Isolated Structure

If the reference conductors of the process periphery are not earthed against the recommendation, e.g., as a safety measure, the corresponding reference conductors should be wired as follows to improve the noise immunity:

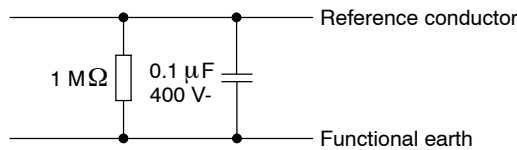


Figure 63 Wiring the Reference Conductor in an Isolated Structure

- The 1 MΩ resistor discharges the static charges
- The membrane capacitor (note the radio frequency input) short-circuits radio frequency interference

A piece of earth fault monitoring equipment can be used to monitor the earth fault of the U_S working voltage:

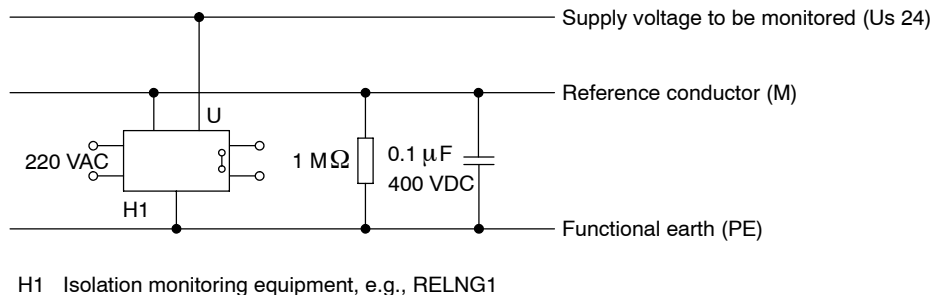


Figure 64 Monitoring the U_S Working Voltage for an Earth Fault

If the configuration covers several cabinets, the wiring is to be repeated for each cabinet.

5.5 Protective Logic and Safety Interlocks

Functions which especially serve the safety make additional configuration measures necessary (VDE 0160, section 4.1.2):

"A further piece of equipment which is independent from the electronic equipment is to be provided if necessary to avoid dangerous effects for people should a piece of electronic equipment (EB) fail, or other suitable measures are to be taken."

Additionally required electric/non-electric safety equipment is dependent on the relevant case of application (e.g., protection against accidentally restarting a motor/piece of equipment or overturning GS motors). VDE 0113, section 6.2.4.6, requires the following to protect against overtravelling:

"If overtravelling is dangerous, an additional sensor for limiting the path must be assigned to each path sensor which has an operational function in the operating cycle. The sensor for limiting the path stops the corresponding movement reliably."

A device which switches off the motor circuit immediately should be used as a second path sensor.

Emergency Stop Equipment (According to VDE 0113)

The emergency stop equipment should stop the machine immediately in the case of danger. The machine is to be stopped so that there is no danger for man nor machine. The emergency stop switch (RAL 3000 red push button, RAL 1004 yellow background) must be easily visible and be able to be reached easily, fast and without any danger by the user.

Circuit Techniques

The emergency stop equipment must be set up with electro-mechanical switch gear.

- ☐ the programmable controller can be switched off as well or
- ☐ the programmable controller can remain live and only dangerous movements are switched off. Safe movements which protect man and machine, e.g., removing parts from acid baths, opening pneumatic doors automatically, etc., are initiated by the programmable controller via a special program.

Appendix A

Programming in Dolog B

This chapter is concerned with the generation and editing of Dolog B programs. The following topics are discussed:

- program construction and program generation
- editing of programs
- calculation of delay times

A.1 Construction of a Dolog B Program (VList Wiring/Connection List)

The program construction of a Dolog B program and a Dolog AKF program differs in several points. In the following the construction of a Dolog B program is represented in detail. The construction of a Dolog AKF program can be drawn from the documentation belonging to the Dolog AKF software.

Programs for programmable controllers are always run cyclically. Only at the end of each program cycle are the signals taken over from the periphery into the signal memory and given out from the signal memory to the periphery (exceptions e.g. Dolog B blocks "AUS", "EIN", "BAUS", "BEIN", ... and analogue in and outputs).

A.1.1 Construction of a Linear VList

A VList is a series of block calls (UND, ODER, SPG, ZVG, ...). The last block of the VList is always the "END" block. When the END block is reached, the following takes place:

- output of the signals from the signal memory to the periphery
- read-in of the signals from the periphery into the signal memory
- jump back to the 1st block of the VList.

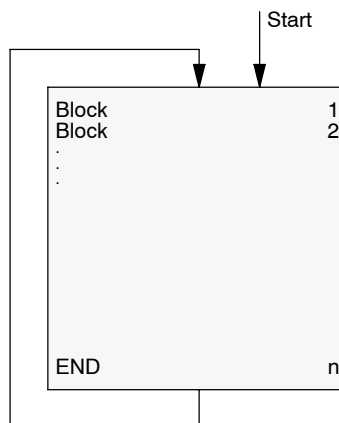


Figure 65 Construction of a Linear VList

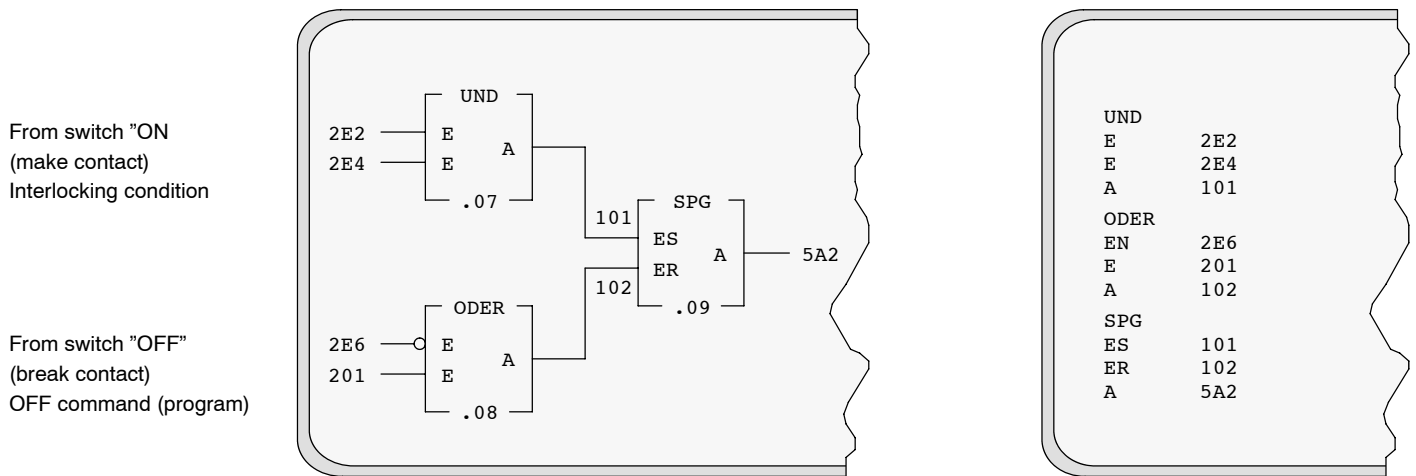


Figure 66 Part of a Program (Switching On and Off, Storing), Function Diagram (Left), VList (Right)

A.1.2 Structure of a VList With Jumps

A VList does not have to be constructed in linear form. With the aid of jump blocks it is possible to run individual parts of a VList dependent on the process state (signal from the periphery).

- A part of the VList is skipped depending on a condition
- A part of the VList is run depending on a condition

A.1.2.1 A Part of the VList is Skipped Depending on a Condition

When the block SPB (jump near, conditioned) is reached, the enable condition (EF) is fulfilled, a part of the VList is skipped. At the point for the jump target the block SZ (jump destination near) is set which is allocated to the SPB.

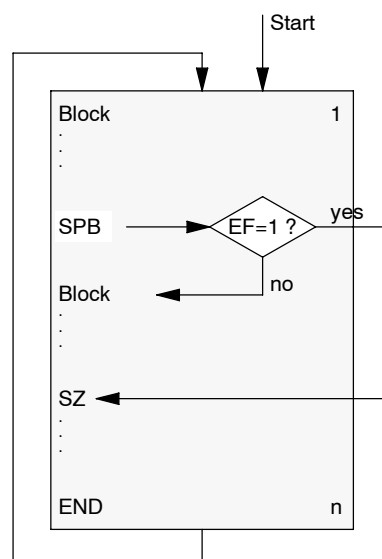


Figure 67 VList with a Conditioned Jump Block



Caution Jumps backwards are also possible. But these lengthen in general the running time of the VList. Especially careful programming is necessary so that endless loops are avoided. Endless loops lead to the fact that the END block is never processed. This results in no further in-or outputs. Such behaviour is monitored and warning is given (UKA signal relay drops).

If an endless loop is run on the A500 it is no longer possible to stop the program using an operating or programming device. The program can only be stopped by switching off the A500 (or by resetting if this is permissible). When the A500 is switched on again, it must be ensured that there is no automatic start (see start-up characteristics).

A.1.2.2 A Part of the VList is Run Depending on a Condition

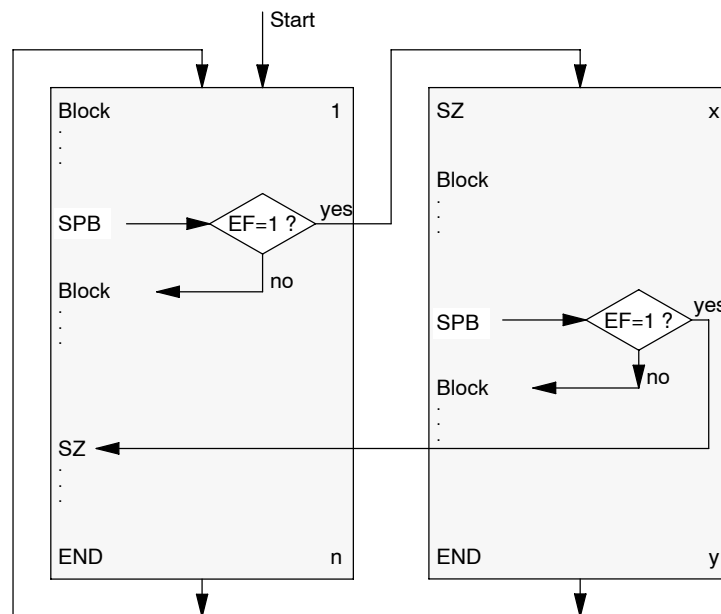


Figure 68 VList with a Conditioned Jump Block

On reaching the first SPB when the enable condition is fulfilled, a jump takes place to one of the VList parts separated from the first part of the VList. At the end of this VList part there can be:

- ☐ a backwards jump
- ☐ a jump to another part of the first part of the VList
- ☐ an END block.



Note After voltage recovery in a subrack with SES 2 modules the SES 2 sends interrupts to the ALU again when the VList is restarted.

A.1.3 Construction of a VList with Subroutines

If certain parts of a VList are required several times then these can be integrated as subroutines. A subroutine can be started in a VList from various locations. If a subroutine is run, then a backwards jump takes place and the VList is operated further from the point following the jump location.

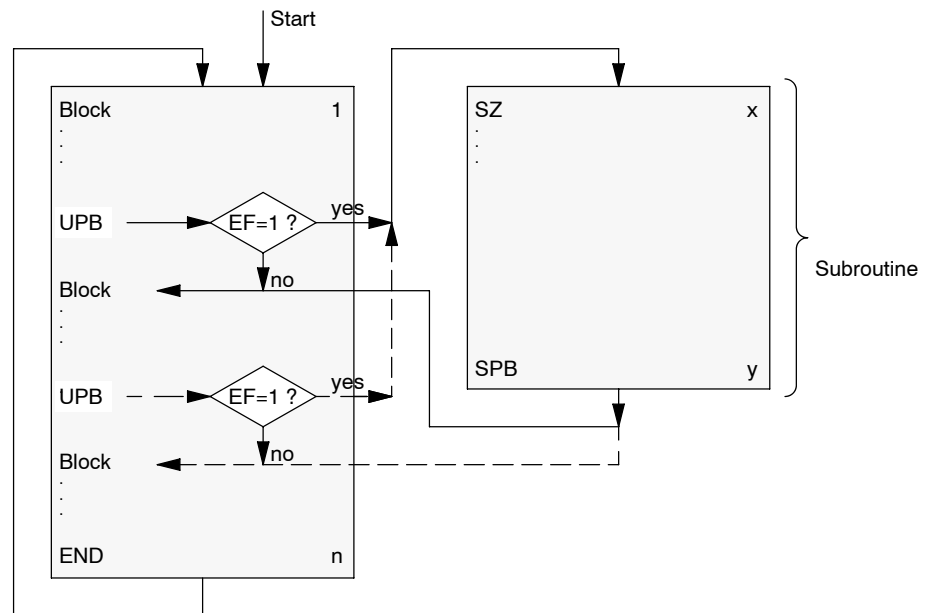


Figure 69 VList with a Subroutine

A VList can be constructed with a combination of jumps and subroutines. This technique facilitates a structured programming which makes them easier to understand. In addition a possible necessary error search is facilitated by rational homogeneous program parts. Jumps and subroutines are not limited to one memory area.

A.1.4 Interrupt VList

With the aid of the spontaneous input module SES 2 (hardware) spontaneous, i.e. (almost) delay-free inputs of binary process signals are possible via the PEAB. These inputs do not take place therefore, when the END block is first reached, but rather they are taken over immediately into the signal memory.

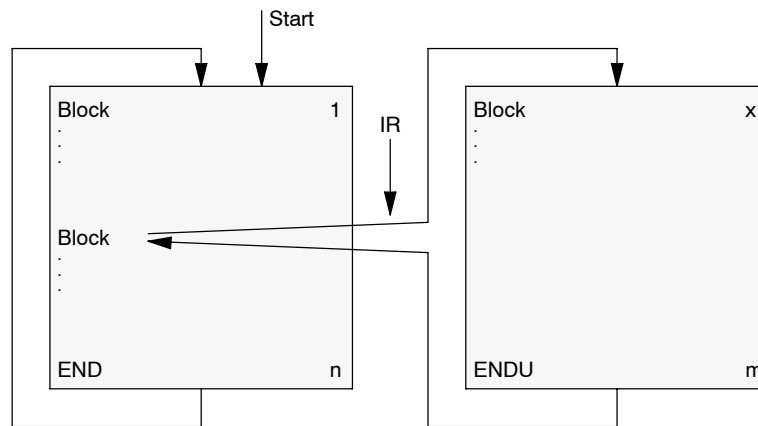


Figure 70 Interrupt VList

The SES 2 reacts to a signal change. If this occurs, an interrupt is caused. As a result, the running program is interrupted immediately (even in the middle of a block) and is branched to an interrupt VList. If this is worked through, a backwards jump takes place to the point at which the VList was interrupted.



Note Every interrupt VList must end with the block ENDU. In this way no outputs can take place. Should an output occur, this must take place via Dolog B blocks such as e.g. AUS, BAUS, ...

The following preconditions must be fulfilled for the interrupt processing:

- ☐ The interrupt module SES 2 must exist.
- ☐ The RAK jumper on the DUA of each subrack (DTA 025) must be opened at the point at which the SES 2 is plugged in (see description of the subrack).
- ☐ In the equipment list 3 must be entered on the location address below which the SES 2 is found on the A series.
- ☐ With the Bsdol function AUL the interrupt must be enabled and the start address of the interrupt VList be defined.

A.2 Program Input

As an example the following short program should be entered (comp. Fig. 66):

```
UND
E   2E2
E   2E4
A   101
```

```
ODER
EN  2E6
E   201
E   2E2
A   102
```

```
SPG
ES  101
ER  102
A   2A2
```

```
END
```

A DTA 101 equipped with a DAP 102 to the right of DEA is in an undefined state, e.g. after a voltage failure without RAM backup or when started for the first time. In this case proceed as follows:

- Step 1** Prepare A500 as described in chapter 3.9 and carry out the steps mentioned in chapter 3.9.3. A500 signals now e.g. with "Dolog B:" or "Dolog B, ALU 150, V5.0:". You are on the level of the operating communication system Bsdol. You can call now any Bsdol function.
- Step 2** Enter "LN". All system internal lists of A500 are standardized now.
- Step 3** Enter "BES" in order to enter the I/O equipment mounting. For this proceed as described in chapter 3.10.1 (page 98). Exception: For DEA address 2 should be entered in place of 33.
- Step 4** Enter "ASB" for setting up the memory area. For the given example it is sufficient to set up one memory area e.g. memory area 1 of 1 kB (e.g. 1 to 1024) in segment 13. Table 23 (page 90) gives recommendations about segments where memory areas can be set up. A list of current allocation of memory area of your A500 can be obtained on the screen when "DSB" is entered.
- Step 5** Enter "SBN" to standardize the memory areas set up in step 4.
- Step 6** Enter "AV" and set the contents of the marker 60 to 0. Exit the function "AV" with "E".
- Step 7** Enter "M". You are now in the program input mode of A500. As memory area state one of the memory areas generated in step 4, e.g. Memory area 1.
- Step 8** Enter "UND". You have called the UND block now. Assign the inputs and output with the addresses 2E2, 2E4 and 101. The block automatically presents the first input. When assignment is done and <CR> is pressed the next input is presented and so on. The block presents the output when <CR> is pressed twice. At the end press <CR> twice to exit the block.

- Step 9** Enter "ODER". You have called the ODER block now. Input and output assignments are done in the same way as in case of the UND block.
- Step 10** Enter "SPG". You have called a flip-flop with initial state now. Assign to the inputs "ES" and "ER" and to the output "A" markers 101, 102 and the reference number 2A2. The block automatically presents the first input. When it is assigned and <CR> is pressed the next input is presented and so on. Enter <CR> at the end to exit the block.
- Step 11** Enter "END". You have called the END block.
- Step 12** Enter "E" to exit the program input mode. Step 13 Enter "S" to start the program. Start address is the number of the memory area where the program is stored in step 7. When started the watch-dog lamp on the UKA turns on when marker 60=0.
- Step 13** Now you can test your program by simulating the inputs on the DAP 102.
- Step 14** Enter "HE" to stop the program. As soon as the program stops the watch-dog lamp on the UKA turns off.

For extensive programs a number of further Bsdol functions are available. These are listed in the chapter A.4 in order of their calls and in chapter A.5 in the alphabetical order. A detailed documentation is given in the user manual Bsdol functions. The page references in chapter A.5 refer to this manual.



Note When the program is running the watch-dog lamp is on only when the marker 60=0. In the undefined state of A500 it can be 0 or 1. It is not set to 0 automatically in step 2 while standardizing the lists. Therefore step 6 is required.

A.3 Measures to Take when the Program Crashes

If a program crashes (e.g. the end block was forgotten in the program input and the VList started) the system variables may be destroyed. These can be restored with the function SYRES, providing that they were backed-up before with the function SYCON and the segment 16 is write protected or stored on EPROM.

If a program crashes, it is no longer possible to stop the program with a programming panel. The program can only be stopped by switching off the programmable controller (or reset if this is permissible). When the A500 is switched on again, it must be insured that no automatic start takes place (see chapter "Startup Characteristics").

A.4 List of Bsdol Functions (in order of their logical use)

In the following chapters only the relevant Bsdol functions are mentioned. A detailed description of all the functions is contained in the handbook of the Bsdol functions. As only the input of Dolog B programs is possible online, here only the essential functions are described. For Dolog AKF, see the corresponding instruction manual.

A.4.1 Online Parameters

Table 32 Bsdol Functions for Online Parameterizing

Bsdol Function	Meaning
LN	Standardize lists. All system internal lists are standardized, e.g. the equipment list. Only LN has to be carried out with an undefined memory content.
BES	Equipment list input.
AEB	Display, modify EPROM component part list. If user programs exist on EPROM, then this function must inform the system to which segment they are located. To run a program from EPROM, another memory area must be opened via the corresponding segment.
DSB	Documenting memory occupancy list. The RAM and EPROM areas are output.
ASB	Display and modification of memory occupancy list. Definition of the memory areas in the RAM and EPROM areas.
AUL	Display and modification interrupt lists (interrupt list). Input of the addresses which are required for an interrupt and the start addresses of the interrupt VList.
RAMZU-KOM	Allocation of a memory area for the comments. In order to comment on a program, a comment memory must first of all be defined.
SYKON be	Backup system variables. The system variables defined so far are stored in segment 16. In order to prevent these data from inadvertently being written over, segment 16 should be write protected (setting on the UKA) after a valid system backup has been made.
SBN	Standardize memory area. Standardize a memory area by writing NOPs. The functions M and MK require a standardized memory area.
AKOM	Input and alteration of comments. I/O bits, markers, digital values and memory areas may be allocated comments and symbolic names.
AV	Display signal memory valencies. Bit, words, double words and floating point words can be displayed and their content altered.
RAMZU-P500	Allocation of a memory area for programming devices. For some functions which are only possible with a programming device, a free memory area in the A500 is necessary (e.g. back documentation in a function block diagram with simultaneous status display with Dolog B, in general necessary for Dolog AKF).

A.4.2 Online Programming

Table 33 Bsdol Functions for Online Programming

Bsdol Function	Meaning
M	Program input. Only possible in the standardized memory area.
K	Program correction. Programs can only be corrected with this function and also re-input. The memory area must not be standardized.
AM	Display and modification block parameter.
MK / KK / AMK	As M, K and AM, but without the comment display.

A.4.3 Online Testing

Table 34 Bsdol Functions for Online Testing

Bsdol Function	Meaning
S	VLists start with jump destination generation (only Dolog B). A Dolog B program is started in any freely selectable memory area. Jump destinations (SZ or SZW) are produced.
START	Start without jump destination generation. Starts a program in a freely selectable memory area (both a Dolog B program as well as a Dolog AKF program). For Dolog B programs no jump destinations are generated, for AKF programs this is not necessary.
HE	Stops at the end. Stops a running program when the END block is reached or at the end of the program.
TI	Test start with internal signal standard. Starts a program in any memory area for a limited number of runs (max. 1000). No signals are read in or out from the periphery. The program functions exclusively with values from the signal memory.
TP	Test start with peripheral signal standard. As TI. Signals are, however, read in and also output from the periphery.
W	Restart after test stop. Starts a program which has stopped after carrying out TI or TP.
AFL	Display and modifications force list. Input of the signals to be forced and their valencies.
SFL	Status input force list. The force list input with AFL is activated. In this way the valencies for each signal which are input in the force list are set dominating (independently of the process state).
ONSTAT	Online status display. Simultaneous display of max. 18 signals (bit, words, double words, floating point words) and their representation during a running program.
ONUM (and	Online changeover (only Dolog B). If a program is started with the function S, then a changeover can be activated from the started memory area to a different memory area in this way also to another program) without stopping the program.
ASPT	Display, modification, input memory test. Input of a list of segments which should be monitored.
SSPT	Start, stop memory test. The segments entered with ASPT are monitored to see whether their contents change.
SUL	Scrolling. Supplies the cross references for a signal in the VList.

A.4.4 Online Documenting

Table 35 Bsdol Functions for Online Documenting

Bsdol Function	Meaning
DBES	Documenting equipment list.
DSB	Documenting memory occupancy list.
DSBK	Documenting memory occupancy list with comments.
DEB	Documenting EPROM component part list.

DFL	Documenting force list.
DSYKON	Documentation of the backed-up system variables. Outputs which lists, which bit and word areas were stored with SYKON.
DKOM	Documenting the comments. Outputs the comments input with AKOM.
RAMZU-QL	RAM allocation for cross reference lists. A working memory is defined in which the cross references produced by the function QL are filed.
QL	Produces cross reference and occupancy list. The lists are produced and filed in the memory defined with RAMZU-QL.
AQL	Display of cross references. Outputs the cross references produced by QL for each signal.
DQL	Documenting of cross references. Outputs the cross references produced with QL for all signals or groups of signals.
DBL	Documenting of the occupancy list. Outputs the occupancy list produced with QL.
DM	Program printout. Outputs a freely selectable part of the VList.
DMK	Program printout with comments. As DM. Comments are also output.
DW	Documenting words. Outputs a freely selectable digital value area. (Printout as words: -32768 ... 32767)
DDW	Documenting double words. Outputs a freely selectable digital value area (output as double words: -2.147.483.648 ... 2.147.483.647).
DSPT	Documenting memory test. Outputs the list of the segments to be monitored produced by the ASPT.
PRZE	Determines test mark. Determines the test marks for the entire contents of the segment.

A.5 List of the Bsdol Functions (sorted topicwise)

Table 36 List of the Bsdol Functions

Function	Meaning	Page
Standardizing Functions		
AAW	Display and modification of number digital values	21-02-16
AEB	Display and modification of EPROM component part list	21-02-12
ASB	Display and modification of memory occupancy list	21-02-07
BES	equipment list Input	21-02-02
DBES	Documenting equipment list	21-02-05
DEB	Documenting EPROM component part list	21-02-13
DSB	Documenting memory occupancy list	21-02-09
DSYKON	Documenting the system variables backed up with SYKON	21-02-21
DSYKON-DBS	Documenting of the backed up system variables for DBS 001	
LN	Standardize lists	21-02-01
SBN	Standardize memory area	21-02-15
SYKON	Back up system variables	21-02-17
SYKON-DBS	Back up system variables for DBS 001	
SYRES	Restore system variables	21-02-20
Programming Functions		
AM	Display and modify block parameters	21-03-05
AUL	Display and modify interrupt lists	21-03-12
DM	Documenting program	21-03-03
DUL	Documenting interrupt lists	21-03-16
K	Program correction	21-03-07
M	Program input	21-03-01
SBK	Copy memory area	21-03-10
SBD	Duplicate memory area	
Programming Functions with Comment		
AKOM	Display, input and modify comments and symbolic names	21-04-05
AMK	Display and modify block parameters with comment	21-04-16
DKOM	Document the comments	21-04-08
DMK	Document program with comments	21-04-14
DSBK	Document memory occupancy list with comments	21-04-10
KK	Program correction with comments	21-04-20
MK	Program input with comments	21-04-12
RAMZU-KOM	RAM allocation for comments	21-04-01
Cross Reference Functions		
AQL	Display cross reference lists	21-05-06
DBL	Document the occupancy list	21-05-09
DQL	Document the cross reference lists	21-05-04
QL	Produce cross reference and occupancy list	21-05-02
RAMZU-QL	RAM allocation for cross reference list	21-05-01
SUL	Scrolling	21-05-10

Function	Meaning	Page
Test functions		
ADW	Display and modify double words	21-06-11
AFL	Display and modify force list	21-06-23
AGW	Display and modify floating point words	21-06-14
AS	Display and modify signals	21-06-06
ASPT	Display, modify and input memory test	21-06-38
AV	Display signal memory valencies	
AW	Display and modify words	21-06-08
DDW	Document double words	21-06-13
DFL	Document force list	21-06-25
DGW	Document floating point words	21-06-16
DSPT	Document memory test	21-06-42
DW	Document words	21-06-10
HE	Stop at the end	21-06-05
ONSTAT	Online status display	21-06-27
ONUM	Online changeover	21-06-33
S	Program start with jump destination generation	21-06-01
SFL	Status input force list	21-06-26
SSPT	Start, stop memory test	21-06-40
START	Program start without jump destination generation	21-06-04
TEST	Test function	21-06-43
TI	Test start with internal signal standard	21-06-17
TP	Test start with peripheral signal standard	21-06-19
W	Restart after test stop	21-06-21
Special Functions		
AH	Display and modify memory contents hexadecimal	21-08-05
PRZE	Determine test marker	21-08-09
RAMZU-P500	RAM allocation for status display on P500	21-08-15
RAMZU-TRACE	Stating memory area for Modnet 1/SFB trace	
TESY	Call up the TESI editor	27-06-01
VLU	VLists conversion	21-08-10
WAD	Address conversion with decimal input	21-08-03
WAH	Address conversion with hexadecimal input	21-08-04
WAR	Address conversion with relative input	21-08-01
Y	Modifying Bsdol control markers	21-08-07
Networking Functions		
ASPE	Operating function "display and modify the interlock bits"	28-10-07
BESU	Transmit Equipment list	28-12-15
BESV	Compare Equipment list	28-12-15
BU	Transmit bit area	28-12-12
BV	Compare bit area	28-12-12
DSTA	Control function "display the status table"	28-10-06
DWU	Transmit double word area	28-12-14
DWV	Compare double word area	28-12-14
FB	Start remote control	28-12-06
HU	Transmit HEX data area	28-12-15
HV	Compare HEX data area	28-12-16
IK	Control function "initializing the delta networking"	28-10-04
RAMZU-FB	RAM allocation for remote control	28-12-05
RAMZU-FERN	RAM allocation for remote control	
SBU	Transmit memory area	28-12-11
SBV	Compare memory comparison	28-12-11
TRACE	Trace function	28-10-08
WU	Transmit word area	28-12-13
WV	Compare word area	28-12-13
ZSE	Destination station end	28-12-06

A.6 List of Dolog B Blocks

Table 37 List of all Dolog B-Blocks

Block	Meaning	Page
ABS	Absolute value formation simple word	23-16-10
AB100	Control block (only with RK 1, 2)	
ACOS	Arc cosine function	29-47-02
ACW	Output after the code conversion from word	23-14-11
ADE	Addition simple word, 15 bit plus operational sign	23-16-01
AEK	Change message with identification	23-18-15
AEM	Change message	23-18-13
AEQ	Comparison of simple words	23-07-01
ALARM	Input in the alarm list B500	23-20-01
ALM	Output after loading from markers	23-14-07
ANST1	Increase limiter 1. order	29-28-01
ANST2	Increase limiter 2. order	
AR1	General rational section 1. order	29-27-01
ASIN	Arc sine function	29-47-01
ATAN	Arc tangent function	29-47-03
AUS	Direct output of a pin series	23-14-02
AVI	Output multiplier	26-05-20
AWA1	Analogue value output with MWA 16PN, 8 bit	23-14-29
AWA3	Analogue value output with MWA 16PN, 10 bit	23-14-31
AWA8	Analogue value 8 x U/I	23-14-33
AWE	Analogue value input with ADU S9, MWE 32	23-14-13
AWE4	Analogue value input with AEM 2511, EMU 2610	23.14.16
AWE13	Analogue value input with ADU I13.2	23-14-20
AWE16	Analogue value input 16 x U/I	23-14-25
ASDB5		
BALK	Bar block	27-13-31
BAUS		
BAW	Bit output from word	23-10-08
BEIN		
BEW	Bit input after word	23-10-07
BILD	Function block diagram (marking in the VList)	23-02-04
BILD-KOM	Diagram block with comments	23-02-07
BISA4	Bit collector for 4 bit	23-11-01
BISA8	Bit collector for 8 bit	23-11-01
BIS16	Bit collector for 16 bit	23-11-01
BIVE4	Bit distributor for 4 bit	23-12-01
BIVE8	Bit distributor for 8 bit	23-12-01
BIV16	Bit distributor for 16 bit	23-12-01
BSPC1		
BSPC5		
BUAE		
BURK1		
BURK2		
BWEIN		
COS	Cosine function	29-46-02

Block	Meaning	Page
DABS	Absolute value formation double word	23-16-11
DADD	Addition double word, 31 bit plus operational sign	23-16-05
DAEQ	Comparison of double words (equivalence)	23-07-02
DBSA5		
DCR	Decrementer (-1)	23-16-13
DDIV	Division double word, 31 bit plus operational sign	23-16-08
DGW1	Convert double word → floating point	29-62-02
DIE	Division simple word, 15 bit plus operational sign	23-16-04
DLA1	Double word loading with condition	23-10-03
DLA2	Double word loading with condition	23-10-03
DLA4	Double word loading with condition	23-10-03
DLA5	Double word loading with condition	23-10-03
DLBW	Loading binary signals in digital value, 31 bit plus operational sign	23-10-10
DLWB	Loading digital value in binary signals, 31 bit plus operational sign	23-10-12
DMUL	Multiplication double word, 31 bit plus operational sign	23-16-07
DOZ1		
DR	Three point controller	29-31-01
DSUB	Subtraction double word, 31 bit plus operational sign	23-16-06
DUR		
DWDN	Code conversion BDC (31 bit + operational sign) → BCN (40 bit)	23-13-04
DWND	Code conversion BCN (40 bit) → BCD (31 bit + operational sign)	23-13-06
DWSA4	Double word collector for 4 double words	23-11-03
DWSA8	Double word collector for 8 double words	23-11-03
DWS16	Double word collector for 16 double words	23-11-03
DWVE4	Double word distributor for 4 double words	23-12-03
DWVE8	Double word distributor for 8 double words	23-12-03
DWV16	Double word distributor for 16 double words	23-12-03
DZRG	Count-down counter, 31 bit, basic position	23-06-06
DZRH	Count-down counter, 31 bit, retentive behaviour	23-06-08
DZVG	Count-up counter, 31 bit, basic position	23-06-02
DZVH	Count-up counter, 31 bit, retentive behaviour	23-06-04
DZVR	Count-up/down counter, 31 bit, retentive behaviour	23-06-11
ECW	Input and code conversion after word	23-14-09
EIN	Direct input of a pin series	23-14-01
ELM	Input and loading in markers	23-14-05
END	Program end	23-02-01
ENDU	End block for interrupt VList	23-02-02
EWM	First value message	23-18-05
EWMV	First value message can be linked	23-18-09
EX	Exponential function	29-48-01
FEA	Flanking recognition 0 → 1 or 1 → 0	23-08-03
FLA	Flanking recognition 1 → 0	23-08-02
FLE	Flanking recognition 0 → 1	23-08-01
FRB	Fill register bit	25-02-01
FRW	Fill register word	25-03-01

Block	Meaning	Page
GABS	Absolute value formation	29-44-01
GADD	Adder	29-40-01
GAEM	Change message	29-72-01
GAEQ	Compare	29-60-01
GAWA3	Floating point analogue output with MWA 16PN	29-13-01
GAWA8		
GAWE1	Floating point analogue value input with ADU S9, MWE 32	23-14-36
GAWE4	Floating point analogue value input with AEM 2511, EMU 2610	23-14-39
GAWE16		
GAWS	Analogue value switch	29-61-01
GBGRZ	Analogue value limiter	29-69-01
GDIFF	Differentiator	29-22-01
GDIV	Divider	29-41-01
GDW1		
GINT	Integrator	29-23-01
GINTB	Integrator with limiter	29-23-03
GIW1	Convert floating point → double word	29-63-02
GKSA4	Floating point value collector for 4 bit	23-11-04
GKSA8	Floating point value collector for 8 bit	23-11-04
GKS16	Floating point value collector for 16 bit	23-11-04
GKVE4	Floating point word distributor for 4 bit	23-12-04
GKVE8	Floating point word distributor for 8 bit	23-12-04
GKV16	Floating point word distributor for 16 bit	23-12-04
GLA1	Load floating point word with condition	23-10-05
GLA2	Load floating point word with condition	23-10-05
GLA4	Load floating point word with condition	23-10-05
GLA5	Load floating point word with condition	23-10-05
GMAXI	Maximum value selection	29-66-01
GMINI	Minimum value selection	29-65-01
GMUL	Multiplier	29-41-02
GNEG	Controllable operational sign reverse	29-43-01
GPGON	Interpolate polygonalpath	29-68-01
GQAD1	Square	29-45-01
GQAD2	Square with operational sign	29-45-03
GRAD1	Route	29-42-01
GRAD2	Route with operational sign	29-42-03
GRZMH	Limiting value signal with hysteresis	29-73-01
GSPM	Peak value formation	29-71-01
GSUB	Subtractor	29-40-02
GVD1	Differentiating section with delay 1. order	29-24-01
GVERH	Ratio former	29-64-01
GVORL	Initial load formation	29-67-01
GVZ1	Delay section 1. order	29-25-01
GVZ2	Delay section 2. order	29-25-03
GVZ1NL	Non-linear delay section 1. order	29-26-01
GWV	Limit value comparison	23-17-01
HAD		
ICR	Incrementer (+1)	23-16-12
IGW1	Convert integer → floating comma	29-62-01
IMA		
INV	Invert word	23-03-10
IPR		
IST		

Block	Meaning	Page
KAS	Control of output dependent on chain step	26-05-17
KET	Organization block chain	26-05-01
KOM	Comment block	23-02-06
KPT	Complement (operational sign reverse)	23-16-09
KSS	1. chain step after a junction	26-05-10
KTE	Chain end	26-05-15
KTS	Chain step	26-05-07
KXS	1. chain step in a branch	26-05-09
KXV	Exclusive OR branch of a chain	26-05-08
LAB		
LA1	Load word with condition	23-10-01
LA2	Load word with condition	23-10-01
LA3	Load word with condition	23-10-01
LA4	Load word with condition	23-10-01
LA5	Load word with condition	23-10-01
LA6	Load word with condition	23-10-01
LBF	Load bit field	23-10-16
LBS	Indirect loading of marker track (bit track)	23-10-13
LBW	Load bit track after word (15 bit plus operational sign)	23-10-09
LB500	control intervention B500 → A500	23-20-05
LDF	Load data field	23-10-15
LDSG	Load segment	23-10-18
LEB	Delete bit area (bit track)	23-09-02
LED	Delete double word area	23-09-03
LEG	Delete floating point word area	23-09-04
LEW	Delete word area	23-09-01
LG	Common (decadic) logarithm	29-48-03
LIN	Measuring value linearization	23-17-11
LN	Natural logarithm	29-48-02
LWB	Load word after bit track (15 bit plus operational sign)	23-10-11
MAP		
MARK	Mark block	27-13-37
MUE	Multiplication simple word (15 bit plus operational sign)	23-16-03
MWB	Average value formation (31 bit plus operational sign)	23-17-09
NOP	Zero operation (block without effect)	23-02-03
NWM	New value message	23-18-01
ODER	Logical OR	23-03-02
PID	Complex block PID regulator	29-20-01
PLA		
POLY		
POS		
POT		
POV		
PRT	Protocoll block	27-13-07

Block	Meaning	Page
REF		
REG	System block regulating	24-03-01
RK	Regulating circuit lists organization	24-03-04
RKA	Regulating circuit VLists commencement	24-03-07
RKB1	Regulator circuit operating block (with RKDB)	29-21-01
RKB2	Regulator circuit operating block (without RKDB)	29-21-01
RKE	Regulator circuit VLists end	24-03-08
RVLA	Regulator VLists begin	24-03-03
RVLE	Regulator VLists end	24-03-06
SAB	Output block	25-04-06
SAS	Output block (in the bit area)	25-05-08
SAW	Output block (in the word area)	25-05-07
SB	Shift register bit	23-19-01
SBVE	Preadjust memory area	23-10-20
SEB	Input block	25-04-05
SEIG	Read in interface, device related	27-13-05
SEIN	Read in interface	27-13-03
SES	Input block (from the bit area)	25-05-06
SEW	Input block (from the word area)	25-05-05
SFW	Shift word (or circular)	23-19-03
SHF	Shift field	23-19-07
SHW	Shift word	23-19-05
SIN	Sine function	29-46-01
SPB	Conditional jump, near	23-15-01
SPG	Memory with basic position	23-04-01
SPH	Memory with retentive behaviour	23-04-02
SPM	Determining peak value (measuring)	23-17-07
SRB	Shift register bit processing	25-04-02
SRW	Shift register word processing	25-05-02
STA	Step begin	26-05-12
STE	Step end	26-05-16
STP	Step process-dependent	26-05-13
SUE	Subtraction simple word (15 bit plus operational sign)	23-16-02
SWB	Conditional jump, far	23-15-03
SWM	Threshold value message	23-17-05
SWN		
SZ	Jump destination, near	23-15-11
SZL	Step with time standard, long	26-05-15
SZN	Step with time standard, normal	26-05-14
SZW	Jump destination, far	23-15-12
TAN	Tangent function	29-46-03
TEA	Text output	27-13-21
TEE	Text input	27-13-13
TEEI	Text input, interrupt controlled	27-13-17
TEEZ	Text input with time limit	27-13-15
TEV	Compare text	27-13-23
TKA		
TKE		
TOTZ	Dead time block	
UND	Logical AND operation of signals	23-03-01
UPB	Conditional subroutine jump, near	23-15-05
UWB	Conditional subroutine jump, far	23-15-08
UZONE	Dead, dead zone	29-70-01

Block	Meaning	Page
VAB		
VAN	Closing delay, 100 ms clock pulse	23-05-01
VAL	Closing delay, 1 s clock pulse	23-05-03
VBS	Comparison of 2 bit tracks	23-07-04
VWS	Comparison of 2 word tracks	23-07-03
WAG	Converting ASCII → floating point	27-13-29
WAH	Converting ASCII → HEX	27-13-27
WDE	Convert double word to simple word	23-13-02
WDN	Convert BCD code to BCN code	23-13-03
WED	Convert simple word to double word	23-13-01
WND	Convert BCN code to BCD code	23-13-05
WORD INPUT	Word by word input of a pin series	23-14-03
WORD OR	Word OR	23-03-04
WORD AND	Word AND	23-03-07
WOSA4	Word collector for 4 simple words	23-11-02
WOSA8	Word collector for 8 simple words	23-11-02
WOS16	Word collector for 16 simple words	23-11-02
WOVE4	Word distributor for 4 simple words	23-12-02
WOVE8	Word distributor for 8 simple words	23-12-02
WOV16	Word distributor for 16 simple words	23-12-02
WXOR	Word XOR via word field	23-03-11
XOR	Exclusice OR	23-03-03
ZR	Two point regulator	29-30-01
ZRG	Count-down counter, 15 bit, basic position	23-06-05
ZRH	Count-down counter, 15 bit, retentive behaviour	23-06-07
ZVG	Count-up counter, 15 bit, basic setting	23-06-01
ZVH	Count-up counter, 15 bit, retentive behaviour	23-06-03
ZVR	Forwards/reverse counter, 15 bit, retentive behaviour	23-06-09

A.7 Cycle Time

 **Note** The given times are only valid for ALU 150.

A.7.1 Structure of the Program Cycle

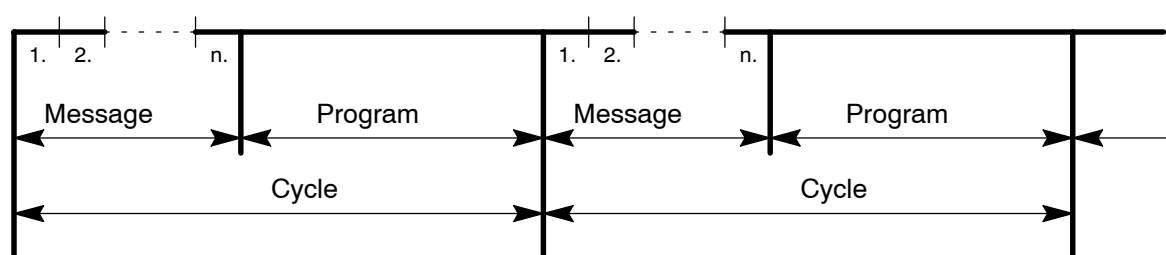



Figure 71 Structure of the Program cycle

The program cycle comprises two parts - processing time of the program and processing time of the binary I/O. With this the scan time can be estimated using the following equation (corresponding to VDI 2889 page 1):

$$t_z = t_{\text{End}} + \sum t_i$$

where t_z = cycle time
 $\sum t_i$ = delay time of the individual blocks
 t_{End} = delay time of the END block (program end with Dolog AKF).
 In this way the I/O are produced.

 **Note** It is to be noted that the delay time of the program can vary by conditional jumps, subroutines, interrupt programs and the regulated delay time system. The influence of these program parts must be taken into consideration in the design.

1N messages further run on the RS 485 interface enabling the processing of the program end to be lengthened by a maximum of one Modnet 1N long message. This is avoided in the use of particular BIK for Modnet 1N networking.

A.7.2 Delay Time of the END Block (or Program End in Dolog AKF)

In each VList cycle the end block is processed once. The delay time of the END block is derived from the basic time plus the times for the:

- PEAB I/O modules
- remote I/O modules

$$t_{\text{End}} = \text{basic time} + t_{\text{PEAB}} + t_{\text{BB1}} + t_{\text{BB2}} + t_{\text{BB3}} + t_{\text{BB4}}$$

where

- t_{PEAB} = number of the 16 bit PEAB I/O groups x 0.145 ms
- t_{BB1} = number of the DEA 10x6 modules on Modnet 1/SFB x, the corresponding delay time see Table 38
- t_{BB2} = number of the DEP/DAP 112 modules on a Modnet 1/SFB x, the corresponding delay time see Table 38
- t_{BB3} = number of the DAP 102 modules on a Modnet 1/SFB x, the corresponding delay time see Table 38
- t_{BB4} = number of the DEA-H1/K1 modules on a Modnet 1/SFB x, the corresponding delay time see Table 38

The following times are applicable:

- Basic time: 4.032 ms
- PEAB I/O (per 16 bit) 0.145 ms
- remote I/O: see Table 38

Table 38 Delay Time of Remote I/O

Delay Times in ms for	62.5 KBd	375 KBd	2 MBd
DEA-H1/K1	10.0	2.5	1.7
DEA 1x6	9.0	2.5	1.9
DEP/DAP 112	1.0	0.5	0.3
DAP 102	2.0	0.8	0.6



Note The cycle time is reduced when several BIKs are used for the planned number of I/O modules. If more than one BIK is available, the individual BIK are directed one after the other. The I/O are then obtained almost parallel. As the directing time for 62.5 KBd and 375 KBd is much shorter than the transmission time of the message, the delay time is reduced. A decisive factor for the entire cycle time is then primarily the Modnet 1/SFB with the most I/O modules.

In the 2 MBd the delay time gains through the use of several BIK is not decisive.

A.7.3 Delay Time of Direct Binary and Analogue I/O on the Modnet 1/SFB

Direct I/O blocks interact in their design directly on the Modnet 1/SFB. They then carry out the I/O message task in the block. The direct I/O blocks are possible on any point in the program.

The following blocks exist:

- BEIN Direct binary input, 16 bit
- BAUS Direct binary output, 16 bit
- BWEIN Direct input in the word area, 16 bit
- AWE16 Direct analogue input, 1 to 16 channels of an ADU 116
- GAWE6 Direct analogue input, floating point format, 1 ... 16 channels of an ADU 116
- AWA8 Direct analogue output, 1 to 8 channels of an DAU 108
- GAWA8 Direct analogue output, floating point format, 1 ... 16 channels of an DAU 108

Table 39 Delay Time of Direct Binary and Analogue I/O on the Modnet 1/SFB

Delay Time in ms for	62.5 KBd	375 KBd	2 MBd
BEIN	12.5	3.5	2.3
BAUS	9.5	1.5	1.3
BWEIN	11.4	3.5	2.3
AWE16 / GAWA6			
1 channel	10.2	3.3	2.5
4 channels	11.6	4.6	3.6
8 channels	14.3	5.8	4.5
12 channels	16.1	7.0	5.8
16 channels	18.9	7.9	7.0
AWA8 / GAWA8			
1 channel	9.5	1.9	1.5
4 channels	11.4	2.8	2.0
8 channels	13.7	4.0	2.8

Interrupts, e.g. time interrupts of the delay time system are permitted between the individual message requests. This provides the opportunity to address the I/O blocks via the delay time system and to carry them out independently from the program end (block END). Interrupting a started I/O or Modnet 1/SFB message is not possible.

On activation one of the above blocks the program or the processing of the block END (program end for Dolog AKF) is stopped when using the delay time system for the duration of a Modnet 1/SFB message, without, however, interrupting the running Modnet 1/SFB messages.



Note

- Use the direct I/O blocks (e.g. BAUS) only from the regulating delay time system (RVL, RKVL)
- Use the maximum channel number in analogue I/O blocks (e.g. AWE16)
- When lower cycle times are necessary, routing of the various message types can be recommendable, e.g. for each BIK for:
 - networking via Modnet 1/SFB
 - analogue and direct binary I/O
 - cyclic I/O.
- In an individual case the optimum distribution is to be determined.

A.7.4 Processing of the END block for Dolog B or of the program end for Dolog AKF

In addition to the processing of I/O at the programmed further functions are processed. This is done in a defined sequence:

1. Processing of ONSTAT ¹⁹⁾, dynamic status display for Dolog AKF on the PADT, online status display in the graphic function block diagram for Dolog B on the PADT etc.
2. Outputs forcing
3. Output of the binary I/O via PEAB and Modnet 1/SFB
4. Input of the binary I/O via PEAB and Modnet 1/SFB
5. Processing of the operating panel DBK 021
6. Processing of the link-up
7. Processing of the Bsdol functions AS, AW, ADW, AV etc.
8. Inputs forcing



Caution

- **since forcing is done only after ending program processing, I/Os, which are processed by direct blocks, should not be forced.**
- **for ONSTAT ¹⁹⁾, the dynamic status display for Dolog AKF on the PADT and the online status display in graphic function block diagram for Dolog B on the PADT etc. The forced values are not displayed.**
- **for Bsdol functions AS, AW, ADW, AV etc. the values without forcing are displayed for inputs. For outputs however, the forced values are displayed.**

¹⁹⁾ The Bsdol function ONSTAT is available only for basic software versions up to 13.3.

A.7.5 Notes on the Regulating Delay Time System

On the construction of regulation circuits via the Modnet 1/SFB the longer Modnet 1/SFB delay times compared to the PEAB delay times are to be taken into account. The following data can be used as standard values for the design (in an individual case the exact limiting values are to be determined concretely):

Maximum number of regulation circuits (approx.)	50	25	15
Scanning time in seconds:	1.0	0.4	0.2

For detailed data on regulating see the relevant publication.

A.7.6 Delay Times of the Dolog B Blocks (for ALU 150)

Table 40 Delay Times of the Dolog B Blocks

Type	Function	Parameter/ Address	Running time for	in μ s
ABS	Absolute value formation simple word	3/12		74
AB100	Operating block (only with RK 1, 2)			
ACOS	Arc cosine function	5/16	<EF> = 0: <EF> = 1:	60 580
ACW	Output after code conversion from the word	4/14		762 + 212 x <WT>
ADE	Addition simple word, 15 bit plus operational sign	4/14		90
AEK	Change message with identification	8/22	<EF> = 0: <EF> = 1:	104 150 + 7 x nB
AEM	Change message	6/18	<EF> = 0: <EF> = 1:	89 128 + 10 x nB
AEQ	Comparison of simple words	5/16		78
ALARM	Entering in the alarm list	7/20		
ALM	Output after loading from markers	4/14		735 + 211 x <WT>
AND	Logical AND operation of signals	< 31/1+ 4E+ 3A		4 each I/O
ANST1	Increase limiter 1. order	13/32	<EF> = 0: <EF> = 1:	70 490
ANST2	Increase limiter 2. order			
AR1	General rational section 1. order	12/30	<EF> = 0: <EF> = 1:	100 640
ASIN	Arc sine function	5/16	<EF> = 0: <EF> = 1:	60 550
ATAN	Arc tangent function	6/18	<EF> = 0: <EF> = 1:	50 430
AUS	Direct output of a pin series (via PEAB)	2/10	<EF> = 0: <EF> = 1:	58 177
AWA1	Analogue value output with MWA 16PN, 8 bit	7/20	<EF> = 0: <EF> = 1:	81 143 + 147 x nK
AWA3	Analogue value output with MWA 16PN, 10 bit	7/20	<EF> = 0: <EF> = 1:	82 143 + 146 x nK
AWA8	Analogue value output 8 x U/1			
AWE1	Analogue value input with ADU S9, MWE 32	7/20	<EF> = 0: <EF> = 1:	83 148 + 480 x <KN>
AWE4	Analogue value input with AEM 2511, EMU 2610	11/28	<EF> = 0: <EF> = 1:	83 148 + 480 x <KN>
AWE13	Analogue value input with ADU I13.2			
AWE16	Analogue value input 16 x U/I			
A5DBS				
BALK	Bar block			
BAUS	Direct output via Modnet 1/SFB			
BAW	Bit output from a word	4/14	<EF> = 0: <EF> = 1:	59 91
BEIN	Direct input via Modnet 1/SFB			
BEW	Bit input after a word	4/14	<EF> = 0: <EF> = 1:	59 104
BILD	Function diagram (marking in the VList)	1/3		2
BILD-KOM	Diagram block with comments	2/8+1 each row		40
BISA4	Bit collector for 4 bit	6/18	<EF> = 0: <EF> = 1:	53 150
BISA8	Bit collector for 8 bit	10/26	<EF> = 0: <EF> = 1:	53 250
BIS16	Bit collector for 16 bit	18/42	<EF> = 0: <EF> = 1:	53 447
BIVE4	Bit distributor for 4 bit	6/18	<EF> = 0: <EF> = 1:	53 152

Type	Function	Parameter/ Address	Running time for	in μ s
BIVE8	Bit distributor for 8 bit	10/26	<EF> = 0: <EF> = 1:	50 254
BIV16	Bit distributor for 16 bit	18/42	<EF> = 0: <EF> = 1:	55 455
BSPC1 BSPC5 BUAE BURK1 BURK2 BWEIN	Direct input in word via Modnet 1/SFB			
COS	Cosine function	5/16	<EF> = 0: <EF> = 1:	60 600
DABS	Absolute value formation double word	3/12		84
DADD	Addition double word, 31 bit plus operational sign	4/14		103
DAEQ	Comparison of double words (equivalence)	5/16		92
DBSA5				
DCR	Decremeter (-1)	3/12	<EF> = 0: <EF> = 1:	49 68
DDIV	Division double word, 31 bit plus operational sign	5/16		206
DGW1	Converting double word \rightarrow floating point word	3/12	<EF> = 0: <EF> = 1:	50 80
DIE	Division simple word, 15 bit plus operational sign	5/16		143
DLA1	Double word loading with condition	3/12	<EF> = 0: <EF> = 1:	108 135
DLA2	Double word loading with condition	3/12	<EF> = 0: <EF> = 1:	110 146
DLA4	Double word loading with condition	3/12	<EF> = 0: <EF> = 1:	110 155
DLA5	Double word loading with condition	3/12	<EF> = 0: <EF> = 1:	109 152
DLBW	Loading binary signals in double word, 31 bit plus operational sign	3/12	$0 < nB \leq 32$	$89 + 17 \times nB$
DLWB	Loading double word in binary signals, 31 bit plus operational sign	3/12	$0 < nB \leq 32$	$86 + 19 \times nB$
DMUL	Multiplication double word, 31 bit plus operational sign	4/14		186
DOZ1				
DR	Three point controller			
DSUB	Subtraction double word, 31 bit plus operational sign	4/14		102
DUR				
DWDN	Code conversion BCD (31 bit + operational sign) \rightarrow BCN (40 bit)	5/16	<EF> = 0: <EF> = 1; $0 < nB \leq 40$:	51 $635 + 40 \times nB$
DWND	Code conversion BCN (40 bit) \rightarrow BCD (31 bit + operational sign)	5/16	<EF> = 0: <EF> = 1; $0 < nB \leq 40$:	46 $526 + 19 \times nB$
DWSA4	Double word collector for 4 double words	6/18	<EF> = 0: <EF> = 1:	148 283
DWSA8	Double word collector for 8 double words	10/26	<EF> = 0: <EF> = 1:	191 468
DWS16	Double word collector for 16 double words	18/42	<EF> = 0: <EF> = 1:	293 834
DWVE4	Double word distributor for 4 double words	6/18	<EF> = 0: <EF> = 1:	145 282
DWVE8	Double word distributor for 8 double words	10/26	<EF> = 0: <EF> = 1:	198 463
DWV16	Double word distributor for 16 double words	18/42	<EF> = 0: <EF> = 1:	292 830
DZRG	Count-down counter, 31 bit, basic setting	7/20	<EF> = 0: <EF> = 1:	188 198
DZRH	Count-down counter, 31 bit, retentive behaviour	7/20	<EF> = 0: <EF> = 1:	187 197
DZVG	Count-up counter, 31 bit, basic position	7/20	<EF> = 0: <EF> = 1:	196 210
DZVH	Count-up counter, 31 bit retentive behaviour	7/20	<EF> = 0: <EF> = 1:	193 206
DZVR	Count-up/down counter, 31 bit, retentive behaviour	13/32	<EF> = 0: <EF> = 1:	191 194

Type	Function	Parameter/ Address	delay time for	in μ s
ECW	Input and code conversion after word	5/16	<EF> = 0: <EF> = 1:	47 $673 + 104 \times \langle WT \rangle$
EIN	Direct input of a pin series (via PEAB)	2/10	<EF> = 0: <EF> = 1:	63 196
ELM	Input and loading in markers	4/14		$695 + 102 \times \langle WT \rangle$
ENDU	End block for interrupt VList	0/6		
EWM	First value message	9/24	<EF> = 0: <EF> = 1:	65 198
EWMV	First value message can be linked	12/30	<EF> = 0: <EF> = 1:	65 242
EX	Exponential function	5/16	<EF> = 0: <EF> = 1:	120 590
FEA	Flanking recognition $0 \rightarrow 1$ or $1 \rightarrow 0$	3/12		59
FLA	Flanking recognition $1 \rightarrow 0$	3/12		60
FLE	Flanking recognition $0 \rightarrow 1$	3/12		60
FRB	Fill register bit	11/28		340
FRW	Fill register word	11/30		303
GABS	Floating point word absolute value formation	5/16		150
GADD	Floating point word adder	5/16		220
GAEM	Floating point word change message	7/20	<EF> = 0: <EF> = 1:	80 150
GAEQ	Floating point word comparison	8/20	<EF> = 0: <EF> = 1:	50 220
GAWA3	Floating point word analogue value with MWA 16PN	11/28	<EF> = 0: <EF> = 1:	80 $420 + 300 / K$
GAWA8	Floating point word analogue output			
GAWE1	Floating point analogue value input with ADU S9, MWE 32	14/34	<EF> = 0: <EF> = 1: without limit: with limit:	80 $370 + 970 / K$ $680 + 1060 / K$
GAWE4	Floating point analogue value input with AEM 2511, EMU 2610	17/40	<EF> = 0: <EF> = 1: without limit: with limit:	70 $420 + 840 / K$ $770 + 920 / K$
GAWE16	Floating point analogue value input			
GAWS	Floating point analogue value switch	7/20	<EF> = 0: <EF> = 1:	40 150
GBGRZ	Floating point analogue value limiter	10/26	<EF> = 0: <EF> = 1:	40 220
GDIFF	Floating point differentiator	8/22	<EF> = 0: <EF> = 1:	80 230
GDIV	Floating point divider	5/16		340
GDW1	Floating point conversion in double word	5/16	<EF> = 0: <EF> = 1:	50 150
GINT	Floating point integrator	10/26	<EF> = 0: <EF> = 1:	80 260
GINTB	Floating point integrator with limit	17/40	<EF> = 0: <EF> = 1:	40 620
GIW1	Conversion floating point word	5/16	<EF> = 0: <EF> = 1:	40 220
GKSA4	Floating point word collector for 4 bit			
GKSA8	Floating point word collector for 8 bit			
GKS16	Floating point word collector for 16 bit			
GKVE4	Floating point word distributor for 4 bit	6/18	<EF> = 0: <EF> = 1:	144 355
GKVE8	Floating point word distributor for 8 bit	10/26	<EF> = 0: <EF> = 1:	195 605
GKV16	Floating point word distributor for 16 bit	18/42	<EF> = 0: <EF> = 1:	293 1106
GLA1	Floating point word loading with condition	3/12	<EF> = 0: <EF> = 1:	107 167
GLA2	Floating point word loading with condition	3/12	<EF> = 0: <EF> = 1:	109 167
GLA4	Floating point word loading with condition	3/12	<EF> = 0: <EF> = 1:	111 173

Type	Function	Parameter/ Address	Running time for	in μ s
GLA5	Floating point word loading with condition	3/12	<EF> = 0:	111
			<EF> = 1:	173
GMAXI	Floating point word maximum value selection	12/30	<EF> = 0:	40
			<EF> = 1:	220
GMINI	Floating point word minimum value selection	12/30	<EF> = 0:	40
			<EF> = 1:	240
GMUL	Floating point word multiplier	5/16		220
GNEG	Floating point word operational sign reverse	6/18	<EF> = 0:	50
			<EF> = 1:	130
GPGON	Floating point word progression interpolating	6/18	<EF> = 0:	40
			<EF> = 1:	
			with 8 restart points	550
			with 60 restart points	750
GQAD1	Floating point word square	5/16		150
GQAD2	Floating point word square operational sign	4/14		150
GRAD1	Floating point word route	5/16		220
GRAD2	Floating point word route with operational sign	4/14		220
GRZMH	Floating point word limit value signal with hysteresis	10/26	<EF> = 0:	60
			<EF> = 1:	390
GSPM	Floating point word top value formation	9/24	<EF> = 0:	70
			<EF> = 1:	200
GSUB	Floating point word subtractor	5/16		220
GTZONE	Floating point word dead zone	8/22	<EF> = 0:	60
			<EF> = 1:	350
GVD1	Floating point word differential section with delay 1. order	12/30	<EF> = 0:	80
			<EF> = 1:	440
GVERH	Floating point word ratio former	7/20	<EF> = 0:	40
			<EF> = 1:	280
GVORL	Floating point word initial load formation	8/22	<EF> = 0:	40
			<EF> = 1:	220
GVZ1	Floating point word delay section 1. order	11/28	<EF> = 0:	80
			<EF> = 1:	440
GVZ2	Floating point word delay section 2. order	14/34	<EF> = 0:	70
			<EF> = 1:	850
GVZ1NL	Non-linear delay section 1. order	13/32	<EF> = 0:	80
			<EF> = 1:	150
GWV	Limit value comparison	10/26	<EF> = 0:	90
			<EF> = 1:	117 + 9 x MW
HAD				
ICR	Incrementer (+1)	3/12	<EF> = 0:	54
			<EF> = 1:	67
IGW1	Conversion integer \leftrightarrow floating point	3/12	<EF> = 0:	80
			<EF> = 1:	130
IPR				
IST				
INV	Inverting word	3/12	<EF> = 0:	59
			<EF> = 1:	72
KAS	Control of outputs depending in chain step	8/22		75
KET	Organization block chain	15/36		
KOM	Comment block	1/6+1 each row		41
KPT	Complement (operational sign reverse)	3/12		60
KSS	1. chain step after a junction	1/8		*
KTE	End of chain	0/6		*
KTS	Chain step	1/8		*
KXS	1. chain step in a junction	1/8		*
KXV	Exclusive OR junction of a chain	1/8		*

Type	Function	Parameter/ Address	Running time for	in μ s
LAB				
LA1	Load word with condition	3/12	<EF> = 0: <EF> = 1:	55 94
LA2	Load word with condition	3/12	<EF> = 0: <EF> = 1:	56 93
LA3	Load word with condition	3/12	<EF> = 0: <EF> = 1:	55 112
LA4	Load word with condition	3/12	<EF> = 0: <EF> = 1:	57 104
LA5	Load word with condition	3/12	<EF> = 0: <EF> = 1:	56 113
LA6	Load word with condition	3/12	<EF> = 0: <EF> = 1:	57 120
LBF	Load bit field	6/18	<EF> = 0: <EF> = 1; <WN> = 10:	51 # 208 #
LBS	Indirect loading of marker track (bit track)	5/16		
LBW	Load bit track after word (15 bit plus operational sign)	3/12	$0 < nB \leq 16$	$83 + 16 \times nB$
LB500	Key contact B500 \rightarrow A500	17/40	<EF> = 0:	44
LDF	Load data field	6/18	<EF> = 0: <EF> = 1:	45 $206 + 9 \times \langle WN \rangle$
LDSG	Load segment	6/18	<EF> = 0: <EF> = 1; <WN> = 132:	57 1503
LEB	Delete bit area	3/12	<EF> = 0: <EF> = 1: B = 1: B = 100: B = 1000:	58 110 307 536
LED	Delete double word area	3/12	<EF> = 0: <EF> = 1; 10 DW:	110 207
LEG	Delete floating point word area	3/12	<EF> = 0: <EF> = 1; 10 GW:	$148 + 6 \times \langle DW \rangle$ 110 206
LEW	Delete word area	3/12	<EF> = 0: <EF> = 1:	53 $74 + 3 \times W$
LG	Common (decadic) logarithm	6/18	<EF> = 0: <EF> = 1:	120 450
LIN	Measuring value linearization	7/20	<EF> = 0: <EF> = 1:	78 216
LN	Natural logarithm	6/18	<EF> = 0: <EF> = 1:	120 450
LWB	Load word after bit track (15 bit plus operational sign)	3/12	$0 < nB \leq 16$	$83 + 16 \times nB$
MAP				
MARK	Marking block			
MUE	Multiplication simple word (15 bit plus operational sign)	4/14		131
MWB	Average value formation (31 bit plus operational sign)	6/18	<EF> = 0: <EF> = 1:	79 137
NOP	Zero operation (block without effect)	0/1		1
NWM	New value message	9/24	<EF> = 0: <EF> = 1:	65 212
OR	Logic OR	< 31/1+ 4E+ 3A		4 each I/O
PID	Complex block PID regulator	53/112	<EF> = 0: <EF> = 1:	1400 3000
PLA				
POLY				
POS				
POT				
POV				

Type	Function	Parameter/ Address	Running time for	in μ s	
PRT	Protocol block	12/20	KOS: <EF> = 0: <EF> = 1: No output: With output:	240 530 1050	
REV					
REG	System block regulating	4/14		100	
RK	Regulating circuit list organization	4/14		100	
RKA	Regulating circuit VLists start	1/8		100	
RKB1	Regulating circuit operating block (with RKDB)	25/56	<EF> = 0: <EF> = 1:	250 700	
RKB2	Regulating circuit operating block (without RKDB)	36/78	<EF> = 0: <EF> = 1:	250 650	
RKE	Regulating circuit VLists end	1/8		100	
RVLA	Regulating VLists start	1/8		100	
RVLE	Regulating VLists end	1/8		100	
SAB	Output block	4/14		195	
SAS	Output block (in the bit area)	4/14		230	
SAW	Output block (in the word area)	4/14		236	
SB	Shift register bit	7/20	<EF> = 0: <EF> = 1:	113 265	
SBVE	Preset memory area	5/16	<EF> = 0: <EF> = 1; <WN> = 132:	56 226	# #
SEB	Input block	5/16		175	
SEIG	Read in interface, device related				
SEIN	Read in interface	1/8	<EF> = 0: <EF> = 1:	103 702	
SES	Input block (from the bit area)	5/16		230	
SEW	Input block (from the word area)	5/16		235	
SFW	Shift word (or circular)	6/18	<EF> = 0: <EF> = 1:	60 116	
SHF	Shift field	6/18	<EF> = 0: <EF> = 1; <WN> = 10:	59 588	
				200 + 29 x <WN>	
SHW	Shift word	6/18	<EF> = 0: <EF> = 1; <WN> = 10:	51 170	
SIN	Sine function	5/16	<EF> = 0: <EF> = 1:	604 600	
SPB	Conditional jump, near	2/10	<EF> = 0: <EF> = 1:	51 65	
SPG	Memory with basic setting	3/12		62	
SPH	Memory with retentive behaviour	3/12		64	
SPM	Ascertaining peak value (measuring)	5/14	<EF> = 0: <EF> = 1:	75 102	
SRB	Shift register bit processing	9/24	<HR> = 10: <HR> = 100:	360 800	
SRW	Shift register word processing	10/26		249	
STA	Step start	1/8			*
STE	Step end	0/6			*
STP	Step dependent on process	0/6			*
SUE	Subtraction simple word (15 bit plus operational sign)	4/14		99	
SWB	Conditional jump, distant	3/12	<EF> = 0: <EF> = 1:	46 118	
SWM	Treshold value message	8/22	<EF> = 0: <EF> = 1:	78 142	
SWN					
SZ	Jump destination near	1/8		39	
SZL	Step with time standard, long	4/14			*
SZN	Step with time standard, normal	4/14			*
SZW	Jump destination wide	2/10		40	

Type	Function	Parameter/ Address	Running time for	in μ s
TAN	Tangent function	5/16	<EF> = 0: <EF> = 1:	40 500
TEA	Text output	7/20	KOS: <BT> = 0: <BT> = 1:	160 670
TEE	Text input	9/24	<BT> = 0: <BT> = 1:	218 430
TEEI	Text input, interrupt control	8/22	KOS: <EF> = 0: <EF> = 1:	270 390
TEEZ	Text input with time limit	7/20	KOS: <BT> = 0: <BT> = 1:	230 430
TEV	Compare text	11/28	<BT> = 0: <BT> = 1:	190 1570
TKA TKE TOTZ	Dead time			
UPB	Conditional subroutine jump, near	3/12	<EF> = 0: <EF> = 1:	61 65
UWB	Conditional subroutine jump, far	5/16	<EF> = 0: <EF> = 1:	51 140
UZONE	Dead, dead zone			
VAB	Opening delay, 100 ms clock pulse	4/14	<E>= 0: <E>= 1:	109 126
VAL	Closing delay, 1 s clock pulse	5/16	<E>= 0: <E>= 1:	120 126
VAN	Closing delay, 100 ms clock pulse	4/14	<E>= 0: <E>= 1:	108 115
VBS	Comparing 2 bit tracks	6/18	<EF> = 0: <EF> = 1; <WN> = 10:	57 207
VWS	Comparing 2 word tracks	8/18	<EF> = 0: <EF> = 1; <WN> = 10:	163 229
WAG WAH	Converting ASCII \rightarrow floating point Converting ASCII \rightarrow HEX	7/20	<EF> = 0: <EF> = 1:	140 1760
WDE WDN	Converting double word to simple word Converting BCD code to BCN code	3/12 5/16	<EF> = 0: <EF> = 1; $0 < nB \leq 20$:	74 51 284 + 18 x nB
WED WEIN	Converting simple word to double word Word by word input of a pin series	2/10 3/12	<EF> = 0: <EF> = 1:	58 68 204
WND	Converting BCN code to BCD code	5/16	<EF> = 0: <EF> = 1; $0 < nB \leq 20$:	51 310 + 19 x nB
WOR WOSA4	Word OR Word collector for 4 simple words	6/18	<EF> = 0: <EF> = 1:	50 127
WOSA8	Word collector for 8 simple words	10/26	<EF> = 0: <EF> = 1:	53 205
WOS16	Word collector for 16 simple words	18/42	<EF> = 0: <EF> = 1:	53 358
WOVE4	Word distributor for 4 simple words	6/18	<EF> = 0: <EF> = 1:	52 126
WOVE8	Word distributor for 8 simple words	10/26	<EF> = 0: <EF> = 1:	52 210
WOV16	Word distributor for 16 simple words	18/42	<EF> = 0: <EF> = 1:	51 355
WUN WXOR	Word AND Word XOR via words field	4/14	<EF> = 0: <EF> = 1; <WN> = 10:	53 193

Type	Function	Parameter/ Address	Running time for	in μ s
XOR	Exclusive OR	< 31/7+ 3A		4 each I/O
ZR	Two point controller			
ZRG	Count-down counter, 15 bit, basic position	7/20		149
ZRH	Count-down counter, 15 bit, retentive behaviour	7/20	<EF> = 0:	148
			<EF> = 1:	147
ZVG	Count-up counter, 15 bit, basic position	7/20		148
ZVH	Count-up counter, 15 bit, retentive behaviour	7/20		144
ZVR	Count-up/down counter, 15 bit, retentive behaviour	13/32	<EF> = 0:	163
			<EF> = 1:	170

nB means: number of bits in a bit track

means: The delay time at <WN> = 10 and <WN> = 20 is the same size.

* Measured delay times for the basic load of the sequence control system KET, STP, SZN, SZL

1. KET <EF> = 0: 306 ms
2. KET <EF> = 1:
 1. ONE step active 780 ms
 2. Relay condition fulfilled 1,2 ms

Additional delay times for branches: KXV, KXS, KSS

1. Step active 30 ms
2. Step active 95 ms 75 ms
3. Step active 170 ms 75 ms
4. Step active 245 ms 75 ms

Appendix B

Module Descriptions

The module descriptions are arranged alphabetically according to their abbreviations.

ALU 011, ALU 012, ALU 021

Central Processing Unit

Module Description

The ALU 01n is one of the central processors for the programmable controller A500. It can be operated in the following subracks: DTA 024, DTA 27.1, DTA 028 (rear connection)
DTA 101, DTA 107 (front connection)

it cannot be operated in: DTA 150 (A350)

The following functions are realized on the module:

- ❑ Central processor (CPU) with 80C186 processor, clock frequency 16 MHz
- ❑ Expandable 80C187 numeric coprocessor, clock frequency 16 MHz
- ❑ Matching controller for the parallel I/O bus (PEAB)
- ❑ Memory bus controller (PMB)
- ❑ Memory for the basic software and user programs up to 768 kbyte RAM or EPROM or mixed (standard equipment: 512 kbyte EPROM)
- ❑ Memory for process data and special areas (unalterable equipment: 256 kbyte RAM)
128 kbytes for signal memory, data fields for networking capability etc.
128 kbytes free for user programs
- ❑ Serial RS 232C interface (V.24)
- ❑ Hardware clock, DCF77 clock (dependent on the configuration)

1 General

1.1 Front and side view (module from index .30 upwards)

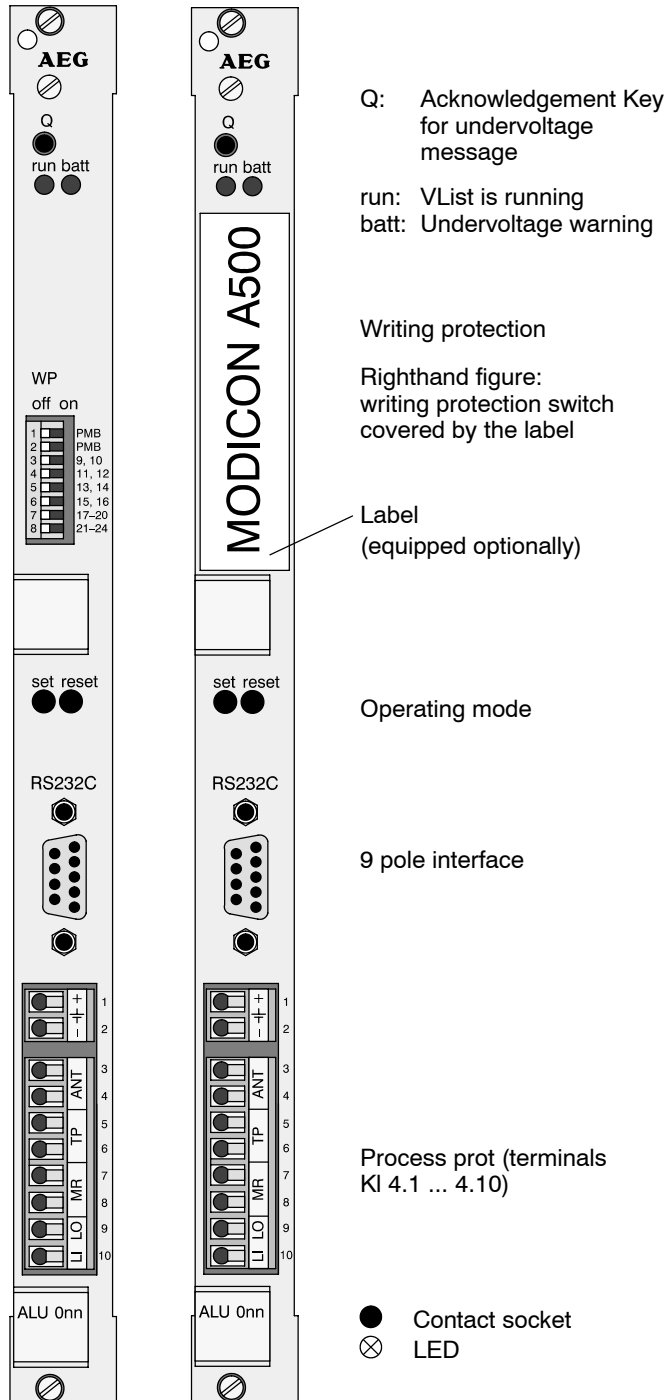
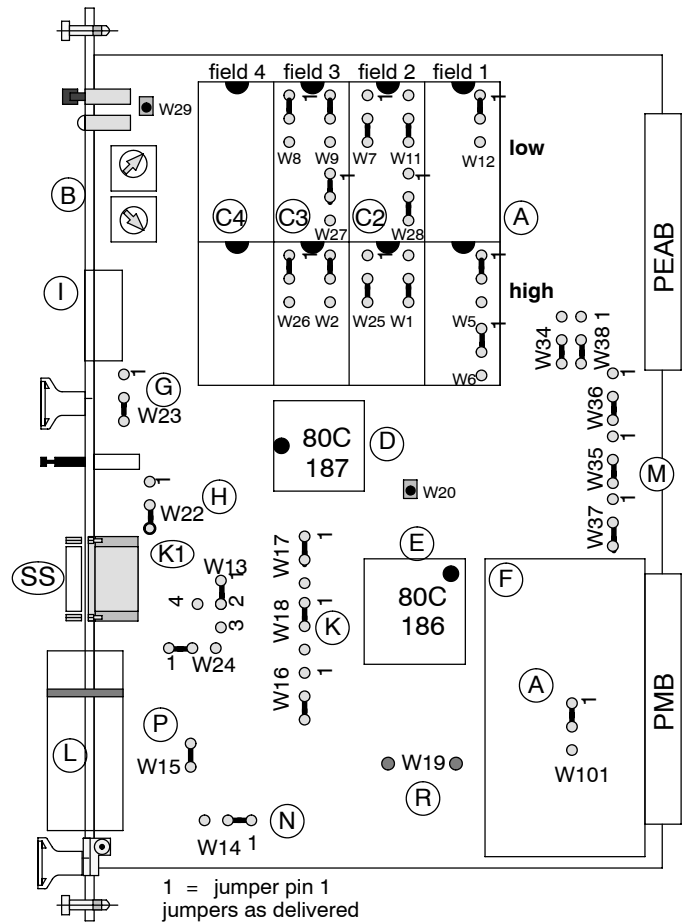


Figure 72 Front view of ALU 011 (from module index .30)



A:	Bit string activation	(3.2)
B:	Status bit	(3.6)
C:	Memory equipment	(3.2)
D:	Numeric processor	
E:	Central processor	
F:	Bit string board	
G:	RAM insertion	(3.2)
H:	"reset" enable	(3.7)
I:	Writing protection	(3.2)
K:	W16, W17, W18 start-up characteristics	(3.4)
K1:	W13 starting characteristics	(3.4)
	W24 backup ext. recharg. battery	(3.5.1)
L:	Terminals	(3.11)
M:	PMB utilization	(3.3)
N:	Rechargeable battery is charging	(3.5)
P:	Testing station only (always connected)	
R:	W19 for program scan time	(3.4.2)
SS:	RS 232C (V.24) interface	(3.8.1)

Figure 73 Overview of the configuration elements of the ALU 011 (starting from module index .30)

1.2 Front and side view (module index .2029)

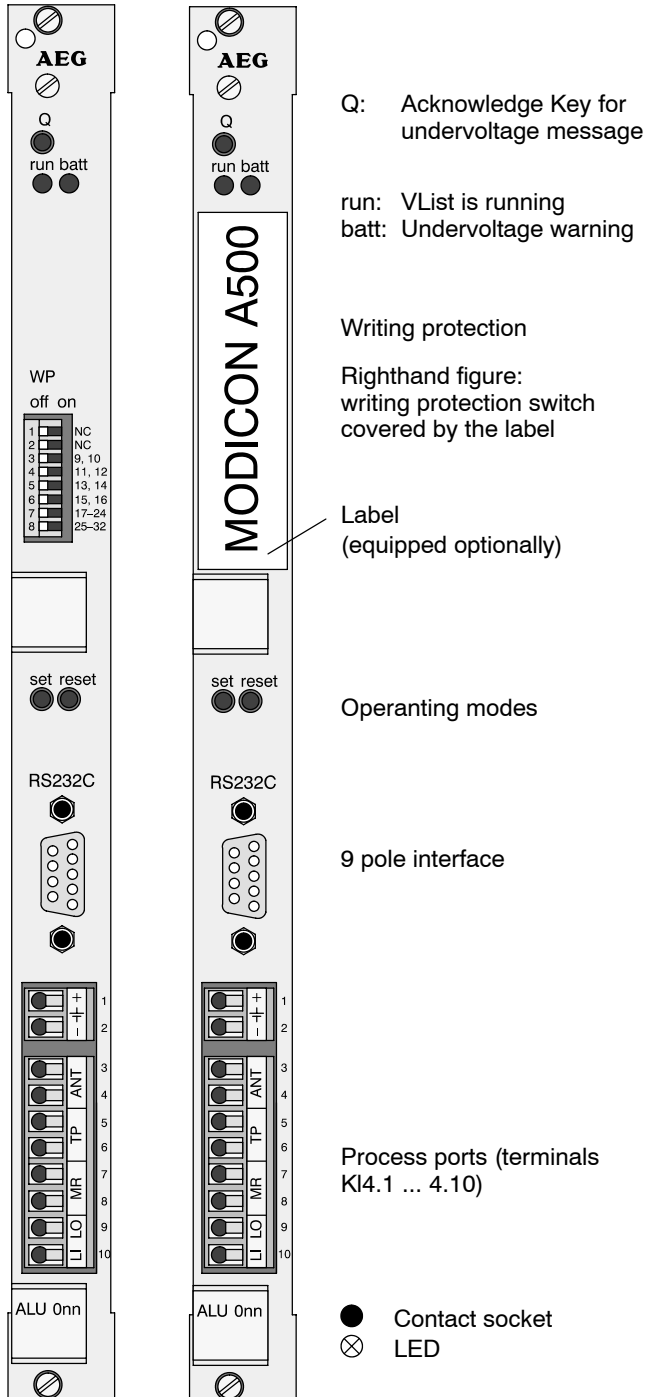
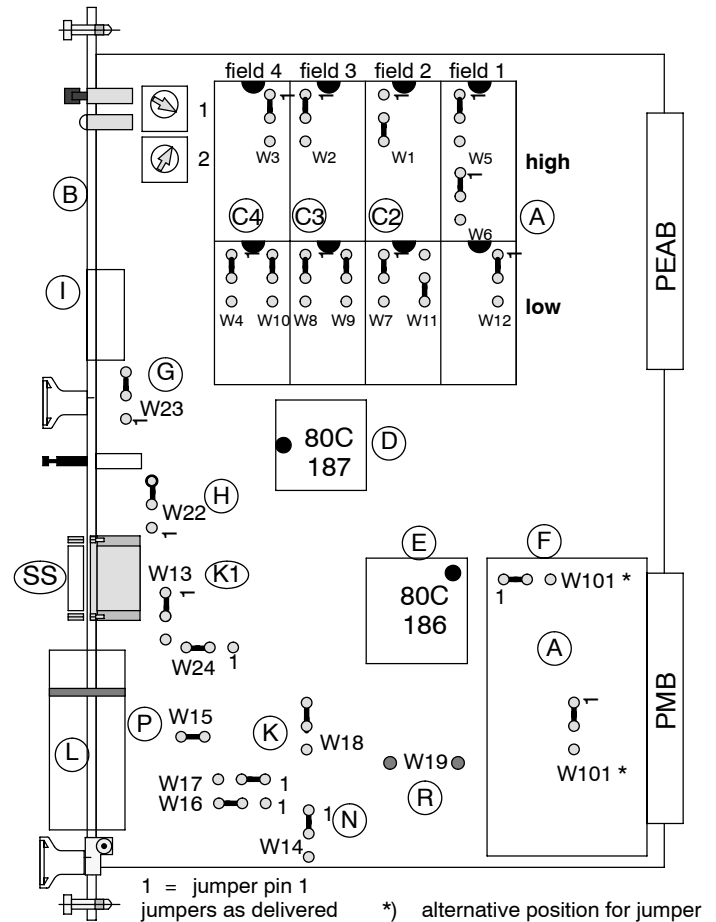


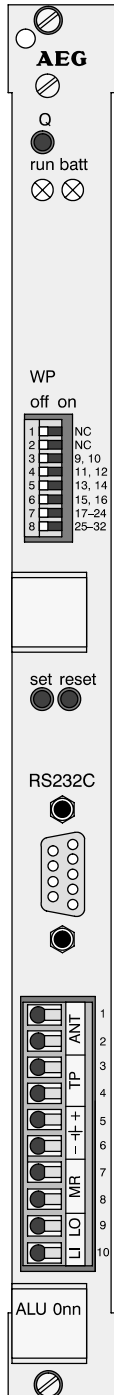
Figure 74 Front view of the ALU 011 ... 019 (index .2029)



A:	Bit string activation	(3.2)
B:	Status bits	(3.6)
C:	Memory equipment	(3.2)
D:	Numeric processor	
E:	Central processor	
F:	Bit string board	
G:	RAM insertion	(3.2)
H:	"reset" enable	(3.7)
I:	Writing protection	(3.2)
K:	W16,17,18 start-up characteristics	(3.4)
K1:	W13 starting characteristics	(3.4)
	W24 Backup ext. recharg. battery	(3.5.1)
L:	Terminals	(3.11)
N:	Rechargeable battery is charging	(3.5)
P:	W15 testing station only (always connected)	
R:	W19 for program scan time	(3.4.2)
SS:	RS 232C (V.24) interface	(3.8.1)

Figure 75 Overview of configuration elements of the ALU 011 ... 019 (index .2029)

1.3 Front and side view (module index .16)



Q: Acknowledgement Key
undervoltage message
run: VList is running
batt: Undervoltage warning

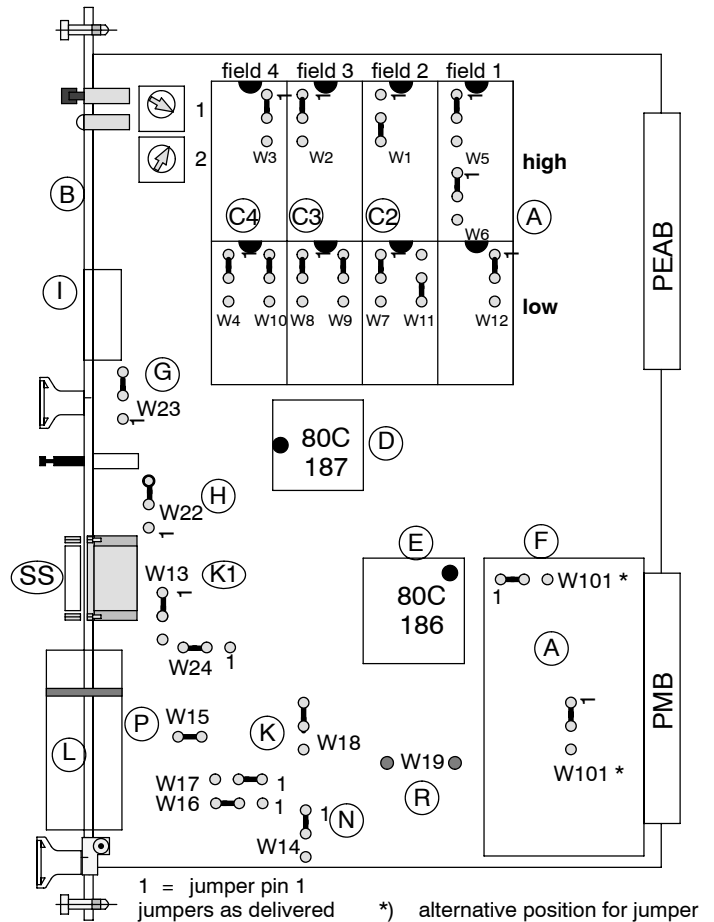
Writing protection

Operating mode

9 pole interface

Process port (terminals
KI 4.1 ... 4.10)

● Contact socket
⊗ LED



A:	Bit string activation	(3.2)
B:	Status bit	(3.6)
C:	Memory equipment	(3.2)
D:	Numeric processor	
E:	Central processor	
F:	Bit string board	
G:	RAM insertion	(3.2)
H:	"reset" enable	(3.7)
I:	Writing protection	(3.2)
K:	W16,17,18 start-up characteristics	(3.4)
K1:	W13 starting characteristics	(3.4)
	W24 Backup ext. recharg. battery	(3.5.1)
L:	Terminals	(3.11)
N:	Rechargeable battery is charging	(3.5)
P:	W15 Testing station only (always connected)	
R:	W19 for program scan time	(3.4.2)
SS:	RS 232C (V.24) interface	(3.8.1)

Figure 76 Front view of ALU 011 ... 019 (module index .16)

Figure 77 Overview of the configuration elements of the ALU 011 ... 019 (module index .16)

1.4 Front and side view (module upto index .19)

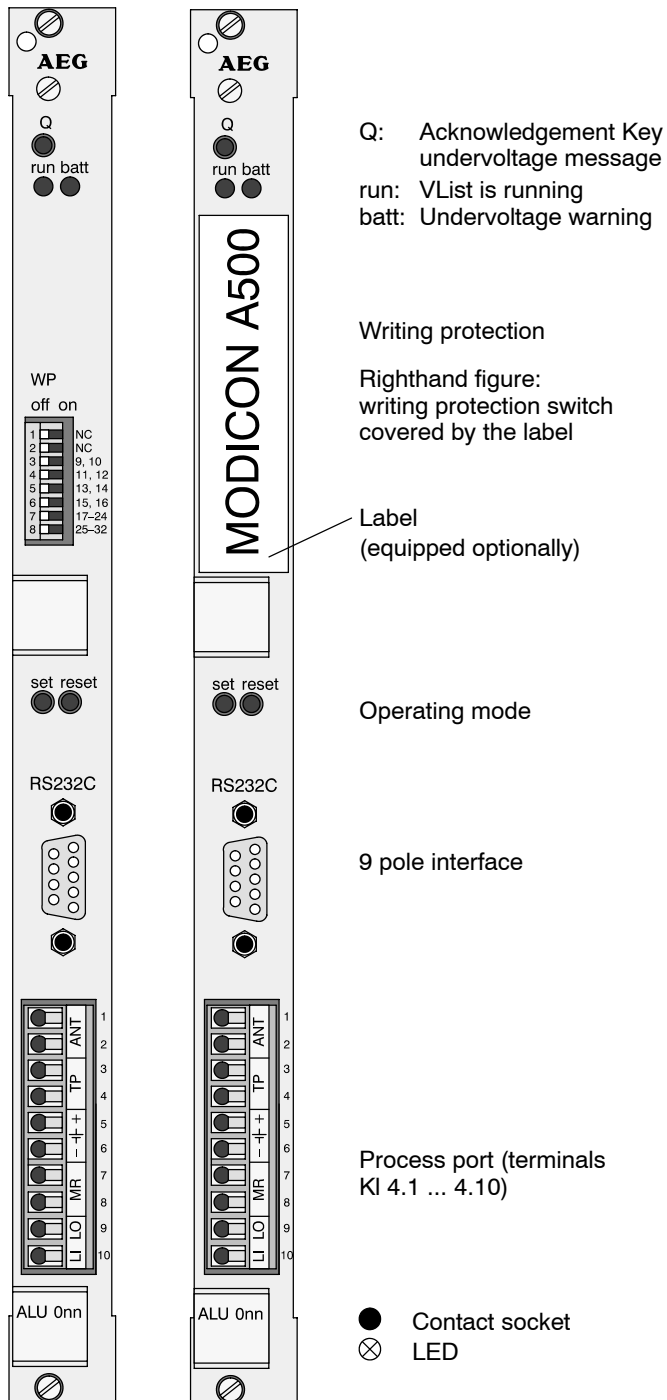
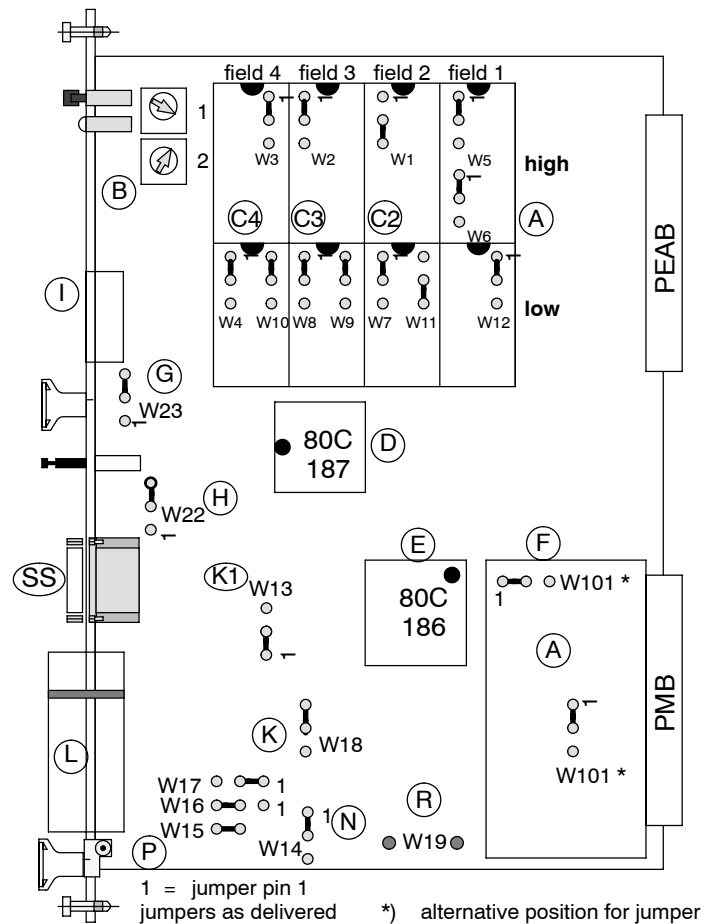


Figure 78 Front view of ALU 011 ... 019 (upto module index .19)



A:	Bit string activation	(3.2)
B:	Status bit	(3.6)
C:	Memory equipment	(3.2)
D:	Numeric processor	
E:	Central processor	
F:	Bit string board	
G:	RAM insertion	(3.2)
H:	"reset" enable	(3.7)
I:	Writing protection	(3.2)
K:	W16,17,18 start-up characteristics	(3.4)
K1:	W13 starting characteristics	(3.4)
L:	Terminals	(3.11)
N:	Rechargeable battery is charging	(3.5)
P:	W15 Testing station only (always connected)	
R:	W19 for program scan time	(3.4.2)
SS:	RS 232C (V.24) interface	(3.8.1)

Figure 79 Overview of the configuration elements of the ALU 011 ... 019 (upto module index .19)

1.5 Variants

The ALU variants are intermediate stages with various functional details which can be read with the E number and its revision index. When ordered it is delivered with the highest index available at the time.

ALU 011 E No. 424 272 546

- ❑ Index .0109:
 - ❑ without DCF77 clock, this cannot be retrofitted.
 - ❑ only KOS 1521 and KOS 8211 can be used (due to the timing adaptation)
 - ❑ rechargeable battery port via terminal 4.5/4.6 without overvoltage protection
 - ❑ individually modified with interrupt signals (like ALU 019)
- ❑ from index .10:
 - ❑ KOS 152 and KOS 821 can be used again (instead of KOS 1521 and KOS 8211)
- ❑ Index .1019:
 - ❑ Rechargeable battery port is not available
- ❑ from index .15:
 - ❑ DCF77 clock can be retrofitted
- ❑ from index .20:
 - ❑ altered rechargeable battery port with terminal 4.1/4.2 with overvoltage protection
 - ❑ LAR 830/831 application: 16 MHz clock (MST2) cannot be used
 - ❑ VPU 852 application: cannot be used!
- ❑ from index .30. Functionally compatible with ALU 019:
 - ❑ All characteristics of ALU 019 are part of the ALU 011; the ALU 011 replaces the ALU 019.
 - ❑ The clock MST2 is available as 4 MHz clock (e.g. for the application of LAR 830/831).

ALU 012 E No. 424 276 422 No price list product

- ❑ from index .10
 - ❑ equipped with DCF77 clock, otherwise same as ALU 011 from index .10

ALU 019 E No. 424 274 988 No price list product

- ❑ from index .10:
 - ❑ without DCF77 clock
 - ❑ designed to process two additional interrupt signals (HLD,HLDA) for the connection of intelligent modules with their own processor (A82 bus)
 - ❑ otherwise like ALU 011 starting from index .10



Note All characteristics of ALU 019 are also part of the ALU 011 with index ≥ 30 ; this ALU 011 substitutes now the ALU 019 (see also chapter 3.3).

ALU 021 E No. 424 277 559

- ❑ Functional compatibility with ALU 011 / from index .30 upwards, however equipped with basic software of version 6.



Note The present module description here after deals with the ALU 011 from module index .30. The corresponding front and side views are presented on page 168.



Note Versions containing English software see 'Ordering codes'.

1.6 Physical Characteristics

The hardware of the ALU 011 ... 019 modules consists of a printed board in double eu-rope format (6HE) and front panel of width 4T with various operating, indicating and port elements as well as the basic software. The power dissipation of the module requires a slot breadth of 8T with an additional dummy plate of 6HE/4T (air supply) with natural convection. A slot of breadth 4T is allowed with forced cooling. However, in this case the small distance to the neighbouring module to the right should be considered while inserting/ removing the module.

The current version of the basic software is equipped in the EPROM memory area.

The main integral parts of the modules are:

- ❑ 80C186 microprocessor for the processor
- ❑ 80C187 microprocessor can be retrofitted as a numeric coprocessor
- ❑ Memory slots with the standard equipment
 - 2 x 128 kbyte RAM for signal memory (bit string, word area) and programs
 - 2 x 128 kbyte EPROM (or RAM) for user programs and basic software
 - 2 x 128 kbyte EPROM (or RAM) for basic software
 - 2 x 128 kbyte EPROM or basic software
- ❑ Real time clock with date and calendar functions (in preparation)
- ❑ Optional RAM backup via rear side bus connector or front side interface connector
- ❑ Front interface for programming panels
- ❑ Rear interface for I/O bus (PEAB) and memory bus (PMB)
- ❑ Rechargeable battery charging circuit with test functions
- ❑ DIP switch panel for RAM insertion and for setting the writing protection
- ❑ Monitoring functions for program run and rechargeable battery voltage
- ❑ Operating mode selection for user program

1.7 Mode of functioning

ALU 011 ... 019 combine in one module the central processor of A500, an additional numeric coprocessor, 512 kB RAM (max. 384 kB of it can be used by the user), 512 kB EPROM as well as the required controller monitoring elements. With this a separate memory module as well as the monitoring module (UKA nnn) are rendered unnecessary and the PEAB slot 1, reserved for this, is available with limitations. The central processor fulfills the following tasks:

- ❑ Creating the internal processing clock pulse
- ❑ Organisation of the internal data traffic on the I/O bus between all the units
- ❑ Writing of the process input signals into the signal memory
- ❑ Processing the user program
- ❑ Saving any intermediate results (markers) in the signal memory
- ❑ Outputting the process output signals from the signal memory
- ❑ Operating the serial interface for program transfers
- ❑ Monitoring of the signal and program memories, processor operation, program loop, supply voltage, and rechargeable battery voltage (not ambient temperature)

For an already equipped hardware clock for log functions the operating function is not available at present.

Depending on the size of the memory allocation, the equipment with a coprocessor and the size of the input/ output, processing speed of 2 to 3 times that of the ALU 150 is available.

2 Operating and indicating elements

The module has the following operating and indicating elements starting at the top of the front panel:

- Acknowledgement key

Q

for the indication of the rechargeable battery under-voltage and program enable inspite of indicated under-voltage
- green LED

run

ON user program is running over END; scan monitoring time is not exceeded

OFF user program or processor operation is faulty
- red LED

"batt"

ON rechargeable battery under-voltage at the time when the system is switched on or after a rechargeable battery test

OFF "good" rechargeable battery voltage or it was not tested
- DIP switch

WP1, WP2

WP3 ... WP8

RAM insertion

writing disable for 6 separate address areas (the DIP switches are covered by the "Modicon A500" label)
- Contact socket

set

reset

Boot loading/ hot restart, see start-up characteristics

break, see start-up characteristics



Warning The possibilities of the "reset" socket should not be used in the standard operation of the system. The program abortion does not guarantee a stopping procedure in accordance with the commands with the data being saved.

- 9 pole connector

RS 232C interface socket connector to connect programming panels or for the supply of an external backup voltage
- 2 + 8 pole terminal

screw /plug-in terminal for the supply and special signals (ext. signals, external backup voltage, error message etc)

3 Configuration

The following should be configured for the module:

- ☐ Equipment of the memory area (if these are different from the delivery status)
- ☐ Memory mode, writing disable areas, RAM insertion
- ☐ Transmission rate
- ☐ Type of the RAM backup
- ☐ Program mode (rotary switch)
- ☐ Program running time (resistor balancing to W19)
- ☐ Terminal assignment
- ☐ Coprocessor (optional) for numerical operations

3.1 Overview of the configuration elements/ indicators

The spatial arrangement for equipment, operation and setting jumpers as well as the section numbers of the relevant configuration measures is given in Figure 73.

3.2 Memory functions

The memory area of the module is divided into 4 fields (see Figure 81). Two sockets for 32 pole RAM or EPROM memory elements are assigned to each of them.

Written EPROM elements are to be plugged in according to HIGH bytes and LOW bytes. The black semicircles in the fields (see Figure 81) show the positions of the marking notches the memory elements should possess.

The DIP switches WP1 ... WP8 (see also Figure 72) are assigned to two functions.

- ☐ With WP1 and WP2 combined with W23 the size of the PMB window for RAM insertion is set.
- ☐ With WP3 ... WP8 the writing protection for the segments 9 ... 24 is set.

Memory write protection WP3 ... WP8:

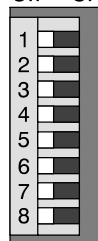
Segments 1 ... 8 from the total of 32 segments of the whole memory areal always have writing enabled. With segments 9 ... 24 6 groups are formed for setting the writing protection, to which switches are assigned. These switches can be operated from a front panel part which is covered by a label. The switches are effective only when equipped with RAM.

With the DIP switches WP3 ... WP8 writing protection is set for the segments given in the label

- ☐ in position ON (writing disabled) or
- ☐ in position OFF (writing enabled) = delivery status

WP

off on

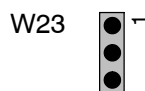


WPx	Segm.	HEX Address	Capacity
3	9 + 10	40000 ... 4FFFF	64 kbytes
4	11 + 12	50000 ... 5FFFF	64 kbytes
5	13 + 14	60000 ... 6FFFF	64 kbytes
6	15 + 16	70000 ... 7FFFF	64 kbytes
7	17 ... 20	80000 ... 9FFFF	128 kbytes
8	21 ... 24	A0000 ... BFFFF	128 kbytes

Switch position

- ☐ writing enabled
- ☐ writing disabled

RAM insertion



WP1, 2
off on
1 ☐ PMB
2 ☐ PMB

When field 2 is equipped with EPROM and a RAM > 128 kbytes is required (available in field 1), a RAM area of 64 kbyte or 128 kbyte, which is otherwise not in field 1, can be activated using the jumper W23 and DIP switches WP1, WP2. However, this increase in RAM is obtained at the cost of the EPROM address area of the ALU. The possibilities obtained through this measure are given in Table 41.

Table 41 RAM insertion

W23	WP1	WP2	Meaning	ALU capacity	Insertion
1 - 2	OFF	OFF	64 KB PMB window on segment 3/4	128 K RAM	-
2 - 3	OFF	OFF	(as delivered)	256 K EPROM	-
2 - 3	OFF	ON	64 KB PMB window on segment 3/4 RAM from segm. 3/4 → inserted to segm. 15/16	128 K RAM 192 K EPROM	64 K RAM
1 - 2	OFF	ON	64 KB PMB window on segment 3/4 RAM from segm. 3/4 → inserted to segm. 11/12	128 K RAM 192 K EPROM	64 K RAM
2 - 3	ON	OFF	128 KB PMB window on segment 3...6 RAM from segm. 3/4 → inserted to segm. 15/16	64 K RAM 192 K EPROM	128 K RAM
1 - 2	ON	OFF	128 KB PMB window on segment 3...6 RAM from segm. 3/4 → inserted to segm. 11/12	64 k RAM 192 K EPROM	128 K RAM
2 - 3	ON	ON	128 KB PMB window on segment 3...6 RAM from segm. 3...6 → inserted to segm. 13...16	64 K RAM 128 K EPROM	128 K RAM
1 - 2	ON	ON	128 KB PMB window on segment 3...6 RAM from segm. 3...6 → inserted to segm. 11...14	128 K RAM 128 K EPROM	128 K RAM

3.2.1 Field 1: data area

Always S RAM elements are equipped in field 1 as memory. 128 kbytes of free capacity are available for the user programs; the rest is reserved for the signal memory , data fields for networking capabilities etc.

Activation of the bit string function

For the use in A500 the ALU 011 is equipped with the bit string board (single bit addressing) and S RAM elements with $t < 100$ ns access time (delivery status). For the activation of the bit string function the corresponding jumpers must be set as shown in Figure 80 (delivery status).

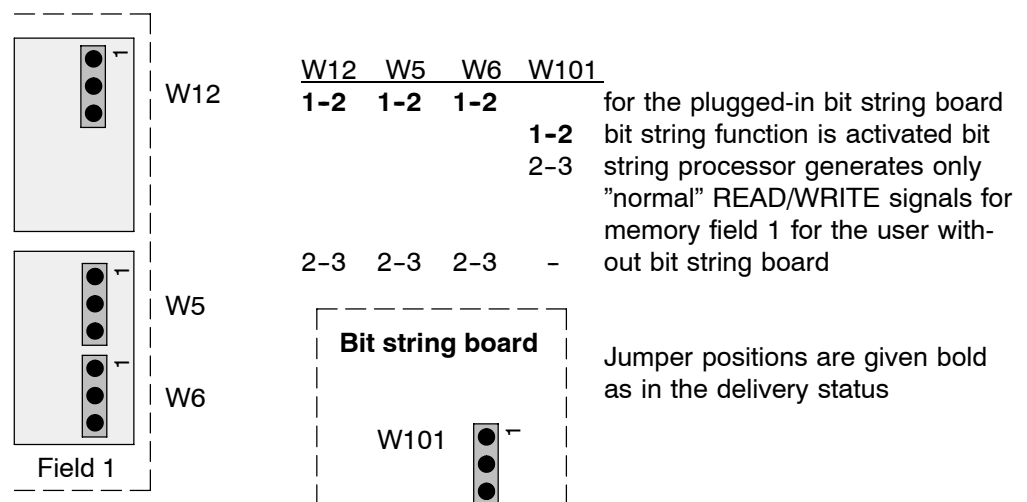


Figure 80 Jumpers for bit string activation (ALU 011)

Bit string boards with and without DCF77 clock have the same layout but different equipment mounting.

3.2.2 Field 2 ... 4: User program, basic software

The standard equipment mounting contains

- for user programs 256 kbyte S RAM elements in field 2 and
- for basic software 2 x 256 kbyte EPROM elements in field 3 and 4

As delivery status the basic software is equipped, including the front panel label. For the correct equipment with the actual version see the following table.

Table 42 Actual basic software on EPROM for ALU 011 (ALU 021)

Type	Slot	Ident-No	Current No	Version
BSW183EN	field 3 (1L)	271 596.xx	1 of 4	V5.05
(BSW184EN)	field 3 (1H)	(275 147.xx)	2 of 4	(V6.)
	field 4 (2L)		3 of 4	
	field 4 (2H)		4 of 4	

Other equipment variants with respect to the memory type can be realized by means of jumpers and are to be taken from the following figure.

In addition field 4 is prepared for inserting 2MB EPROM. Only AEG Modicon manufactory is able to change the soldering jumpers for this option.

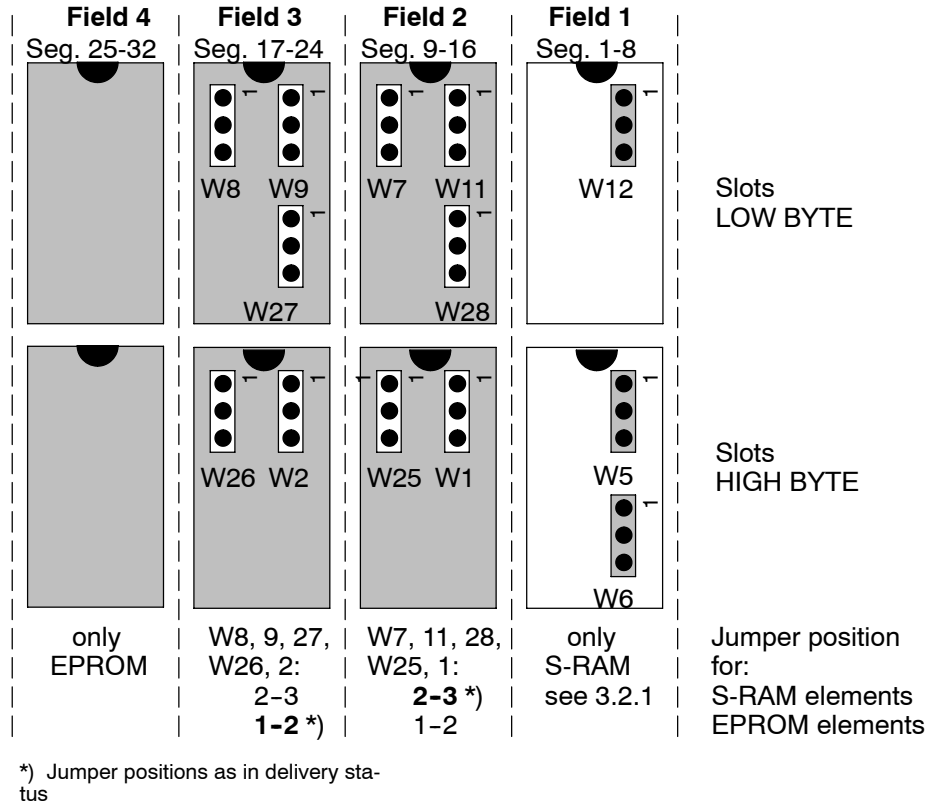


Figure 81 Selecting RAM/EPROM equipment mounting of the ALU 011

3.3 Use of the module in the PMB'-area (Part of ALU 019)

For the extension of the PMB to PMB' the module is equipped with the HOLD/HLDA function. Assuming that the jumper positions are correct, a second ALU functions like a memory module. The jumpers and their plugging position should be taken from the following table and their location from Figure 73.

Table 43 PMB' use

W37	W35	W36	W38	W34	Meaning
2-3	2-3	2-3	2-3	2-3	Use in PMB area (= delivery status)
1-2	1-2	1-2	1-2	1-2	Use in PMB' area

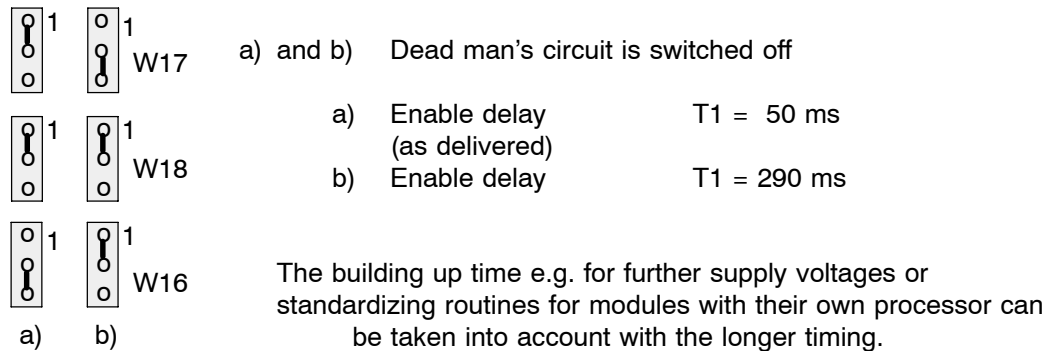
3.4 Start-up characteristics

The start-up characteristics of a programmable controller depend on several conditions:

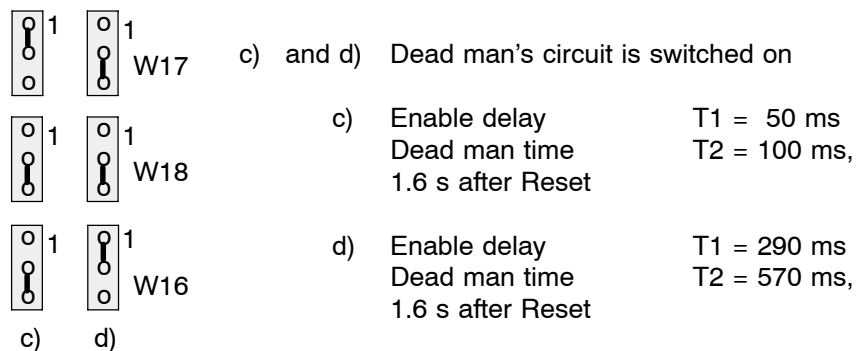
- ❑ Mains supply / battery backup (watchdog 1)
- ❑ State of the basic software (watchdog 1)
- ❑ State of the user software (watchdog 2)
- ❑ Process state (cold restart / hot restart)

3.4.1 Monitoring of the supply and basic software (watchdog 1 with jumpers W16, W17 and W18)

The disable signal for the start enable of the programmable controller is removed T1-ms after obtaining the setpoint values of the supply when the voltage is switched on or when it returns. The same is valid if the 5 V supply falls below 4.65 VDC so that battery operation had to be switched on.

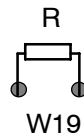


The dead man's circuit is switched on with W18 in position 2-3, whereby the following functions and 2 other timings are activated. The dead man's circuit expects an initial ready message from the basic software within 1.6 sec after the delay of T1 and then other regular messages within T2 (every 100 or 570 ms). A "reset" is otherwise initiated.



3.4.2 Monitoring of the user software (Watchdog 2 with W19 solder tag)

The scan time of the running software is monitored with this circuit. The circuit operates the dead man's relay and the "run" LED. If the monitoring time is exceeded, the pilot relay drops out and the green "run" LED goes out.



The monitoring time is set to approx. 1.1 s by the factory. It can be varied between 220 ms and 600 ms by soldering in an R resistor on the W19 tags. The corresponding resistor value is to be taken from the following diagram (delivery without resistor).



Warning The short-circuiting of the solder tags is not allowed. R permissible: $\geq 220 \text{ k}\Omega$

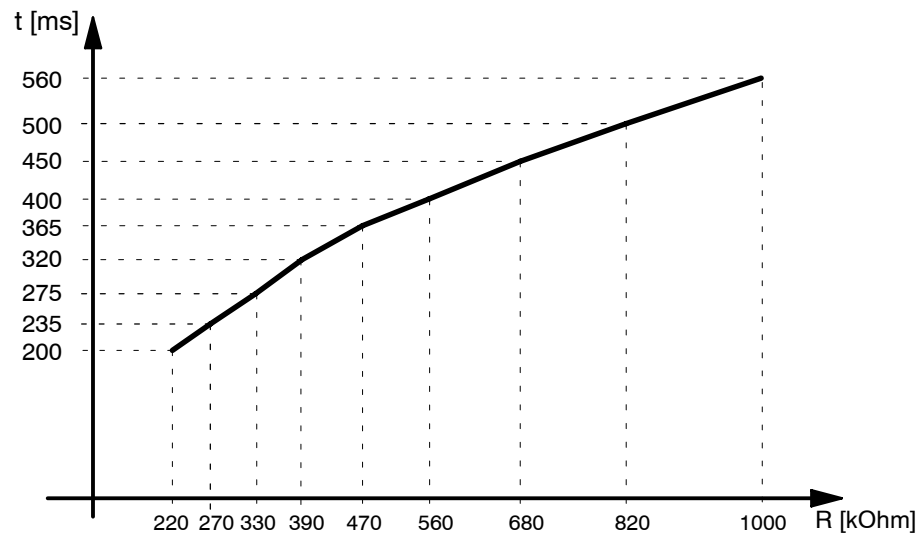
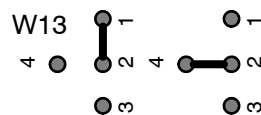


Figure 82 Resistor for the scan time monitoring on the ALU 011

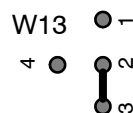
3.4.3 Starting the user program

The type of program start is set with the W13 jumper. Its action corresponds to the M5 jumper for the UKA 024 monitoring module.



Automatic start

The signal DSR (2-1) or DCD (2-4) is switched through to the ALU (the selection of DSR or DCD depends on the software). The user program of the programmable controller is started automatically when the supply voltage is switched on (delivery status: 2 - 1)



Manual start

The signal DSR/DCD is interrupted and set to "high" for the ALU. The programmable controller remains as stopped when the supply voltage is switched on and must be started manually via the programming panel.

3.4.4 Starting dependency on the state of the controlled process

The process can be continued with boot loading or a hot restart after an interruption depending on the type of the process to be controlled. For this purpose there are the "set" and "reset" contact sockets on the front panel for the following functions:

Boot loading Boot loading of the program → Pins "set" and "reset" are plugged in.

- ☐ at the start of the program
- ☐ when the mains is switched on
- ☐ with an automatic reset by the activated basic software monitoring

Some initialization cycles are executed with boot loading. Blocks with initial state characteristics are standardized here with Dolog B programming. Blocks which are not processed in these cycles are not standardized (e.g. interrupt Vlists) Further standardizations which are beyond this scope are to be realized by the user by means of program.

From basic software 5.05 upwards the Bsdol function "SSN" is available. With this the system RAM contents of the ALU can be brought in a defined state. This function, which is locked for operation during the V list run and for remote operation, must be carried out at the beginning of each boot loading. For this proceed as follows:

1. Remove the "reset" plug on the ALU
2. Go to the level of the Bsdol system and ente <SSN>.
3. Answer the question, if this function should be really carried out, with "yes".
4. Leave the function <SSN> by plugging and removing the plug "reset". Now you are again on the level of the Bsdol system.



Note The function "SSN" can be called under AKF 35 by selecting the menu point video terminal emulation.

Cold restart: Program execution to be continued with cold restart → pin "set" plugged in, pin "reset" free

Hot restart: Program execution to be continued with hot restart → Pins "set" and "reset" free

The programmable controller principally continues the program at the point of the interruption with the saved signal memory data.

3.5 Backup battery and monitoring the backup



Warning If the module is disconnected from the subrack without the connection of an external battery, data loss can occur!

3.5.1 Supplying the backup voltage

Three different sources can be selected for the supply of the S RAM elements:

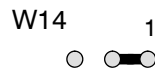
- ☐ central rechargeable battery in the subrack
- ☐ external rechargeable battery via screw/plug-in terminals
- ☐ external battery via interface connector (for service purposes only)

To backup the CMOS elements a rechargeable battery is to be used as it is installed in subracks with rear connections (NiCd 3.6 V/ 1.8 Ah, see ordering details). The supply is obtained via the PMB.

The optional supply via the interface connector of the front panel (to disconnect the module; for the connector pin assignment, see 3.8.1) is isolated with diodes from the PMB supply and protected against overvoltages up to ± 15 V.

The third backup possibility is the direct supply to the PMB via screw/plug-in terminals 1/2. If PMB nodes are also backed up via this front connection, the voltage fall for the safety circuit (approx. 100 Ohms) should be taken into account.

Backup with a central rechargeable battery



The rechargeable battery of the subrack of the controller is charged with this jumper position. The supply is obtained via PMB. The charging current amounts to approx. 100 mA. (status as delivered)

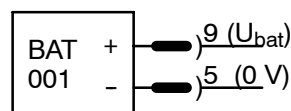
Backup with batteries which cannot be recharged:



The charging current for the central rechargeable battery of the subrack is interrupted with this position of jumper W14; in this case the controller can also be backed up with batteries which cannot be charged up.

Backup with an external voltage

If an additional backup voltage is supplied via the 9 pole interface connector (RS 232C), the module can be disconnected without any information loss, so that jumper W14 is accessible for the change of the type of backup.



Only the lithium battery block BAT 001 (3.6 V) with a 9 pole plug connector, which supplies via the contacts 9 and 5, is available (see also Figure 84).



Caution The terminal voltage of the battery must be at least 2.3 V.

Operating the rechargeable battery via the screw/plug-in terminals on the front panel

A connected rechargeable battery is charged up and loaded like a rechargeable battery installed in the subrack, whereby its terminal voltage must be at least 2.0 VDC. A distinction is made between 2 physical techniques:

- | | |
|---|--|
| $+ U_{\text{Akku}} \begin{array}{c} \text{---} 1 \\ \text{---} \end{array}$
$\text{GND} \begin{array}{c} \text{---} 2 \\ \text{---} \end{array}$ | Physical arrangement of the 2 + 8 terminals according to Figure 85
For backup operation W24: 1-2 must be plugged in |
| $\begin{array}{c} 1 \\ \text{---} \end{array}$
$\text{---} \text{---} \text{---}$ | W24 Supply via front terminals is enabled (as delivered) |
| $\text{---} \text{---} \text{---}$
$\text{---} \text{---} \text{---}$ | Supply via front terminals is interrupted. |



Caution Externally supplied backup voltages may amount to max. 5 V.

3.5.2 Monitoring functions

At the time, when the mains supply is switched on, the battery voltage (rechargeable battery voltage) is tested. If undervoltage is detected, the markers M23 and M33 are set to "1" and the red LED "bat" lights up. The program execution is blocked, because data loss can occur. If it is irrelevant, e.g. at boot loading, the program disable is removed with the acknowledgement key Q (Figure 72 or Chapter 2).

If the operating voltage of +5 V for CMOS supply is on the memory elements and if a rechargeable battery test is not carried out, the rechargeable battery is charged up with approx. 100 mA. If the operating voltage drops below 4.65 V, the supply of the entire memory is switched over to battery operation.

Battery test

The battery test is initiated and repeated cyclically (e.g. test repetition every 30 min.) with the program running. The rechargeable battery is loaded here for 2.5 ms with approx. 350 mA. The charging procedure is interrupted during this time.

Effect of the measured value:

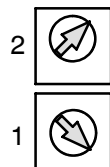
UBatt > 2.0 V: The quality of the rechargeable battery is normal

UBatt < 2.0 V: The quality of the rechargeable battery is insufficient. Markers 23 or 33 are set and the red LED "bat" lights up

Q key If the battery voltage does not remain

LED "bat" permanently below 2.0 V after the load test, the message can be acknowledged with the Q key (marker is reset, the red LED goes out).

3.6 Setting status bits



The status bits can be preset with the two code switches (Figure 73, B). Out of the 16 switch positions only 0 ... 7 are used for A500 programmable controllers. Transparent mode and diagnosis mode (positions 8...15) are reserved for B500 systems.

Switch functions:

Switch 1: Baudrate

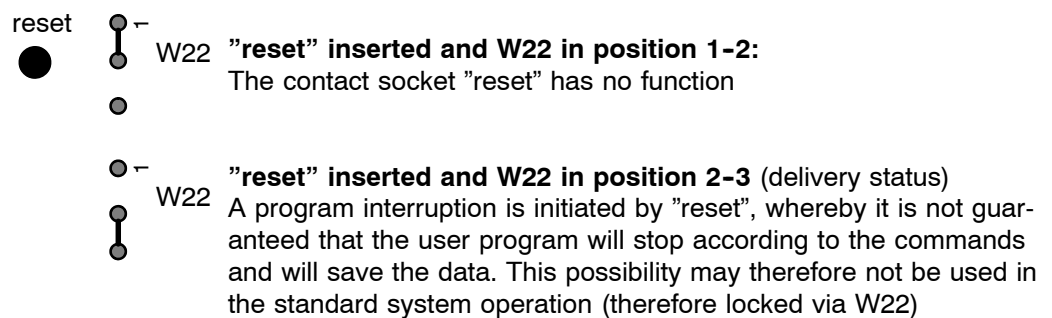
Switch 2: Automatic restoration of "B1", "E" and "G".

Position	Code switch 1:		Code switch 2:		
	Transparent-mode-B500	Baudrate "Bd"	System variable autom. restaur. "B1"	Singel bit Entry "E"	Sensor bit standardization "G"
0	no	-	no	no	no
1	no	-	yes	no	no
2	no	1200	no	yes	no
3	no	2400	yes	yes	no
4	no	9600	no	no	yes
5	no	19200	yes	no	yes
6	no	9600	no	yes	yes
7	no	19200	yes	yes	yes
8	yes	-	no	no	no
9	yes	-	yes	no	no
A	yes	1200	no	yes	no
B	yes	2400	yes	yes	no
C	yes	9600	no	no	yes
D	yes	19200	yes	no	yes
E	yes	9600	no	yes	yes
F	yes	(Diagnosis)	yes	yes	yes

Position as delivered

Figure 83 Code switches on ALU 011

3.7 Program abortion



3.8 RS 232C Interface (V.24)

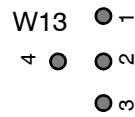
3.8.1 RS 232C connector (programming panel or backup battery BAT 001)

Figure 11 shows the terminal assignment of the RS 232C socket for 2 different connection possibilities. The metallic chassis of the socket is connected to the front panel.

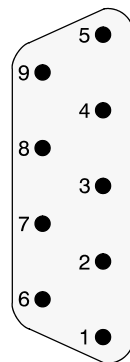
1. Programming panels

"RS 232C" column This is the universal signal assignment of the ALU interface. The "data terminal equipment is ready for service" input (S1, port 4) is not used when operating the system programming panels YDL 052.

Switching over of DSR/DCD connections:



- 2-1: The signal DSR/DCD of the interface module is switched over to pin 6 (as delivered)
- 2-4: Signal DSR/DCD is switched over to pin 1.
- 2-3: DSR/DCD is set to HIGH and is activ permanently.



Con- nection	RS 232C (V.24)	BAT 001	Meaning of the signals
1	M5 (DCD)		Reception signal level of the partner
2	D2 (RxD)		Received data
3	D1 (TxD)		Transmitted Data
4	S1 (DTR, optional)		"Ready for service" of ALU
5	E2 (0V)	Bat -	Signal ground GND
6	M1 (DSR)		"Ready for service" of the partner
7	S2 (RTS)		"Ready for transmission" of ALU
8	M2 (CTS)		"Ready of transmission" of the partner
9		Bat +	Backup voltage with reference to E2

● Occupied connector piont
 ○ Non-occupied connector piont

Figure 84 Terminal assignment of the interface connector on ALU 011 (looking at the connector side)

2. Backup battery

"BAT 001" column: shows the terminal assignment of the BAT 001 battery block (with a 9 pole connector) for backing up the CMOS elements with a disconnected module. See also chapter 3.5.1.

3.8.2 YDL 052 programming cable

The ALU 011 is connected to a programming panel (e.g. P500-AT) via the serial interface RS 232C with the YDL 052 cable (from index .02). Figure 84 shows the names of applied signals.

3.9 Hardware clock

The hardware clock manages the parameters.

Time: second, minute and hour

Calendar: Week day, date, month and year. Leap years are corrected automatically.

The clock is set by the software. There are no settings to be done by the hardware.

The time information is saved in the digital words from 60 to 64 and is therefore available for other routines as well.

The clock is operated on the backup battery of the subrack; therefore it runs also when the supply voltage is switched off.

3.10 DCF77 clock for ALU 012 (no price list product)

The DCF77 clock equipped on the bit string board is to be connected to the externally installed antenna via the front terminals 4.3/4.4. The starting pulse of the clock (synchronizing pulse) is available at terminals 4.5/4.6 disconnected optically. The collector of NPN transistor is connected to terminal 4.5 via the protective resistor and the emitter to terminal 4.6.

3.11 Process interface

Screw-/plug-in terminals 4.1 ... 4.10 from production index .20

The changed physical arrangement, with respect to production index < .20, and terminal assignments as shown in Figure 85 prevent the wrong plugging of the terminals so that no inadmissible voltages can reach the CMOS backup input.

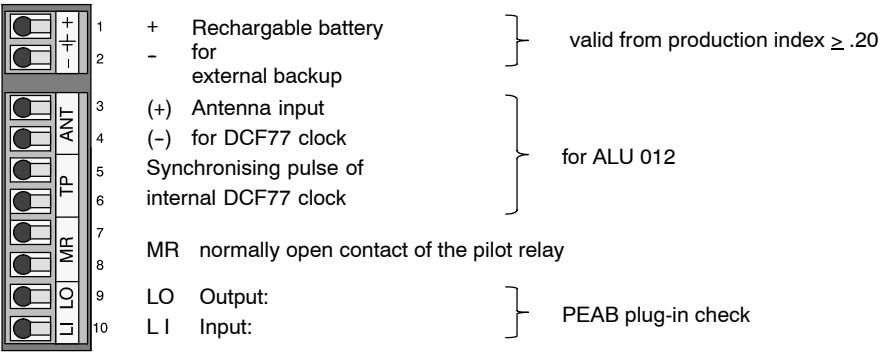


Figure 85 Assignment of the (2+8) pole terminal on the front panel

Plug-in check terminal 4.9/4.10

If the plug-in check of modules is not foreseen or realized otherwise in the system, terminals 4.9 and 4.10 are to be connected via a wire jumper. The relevant error message is prevented in this way (chapter 3.13.2, marker 20/30).

3.12 Documentation

3.12.1 Graphical symbols (circuit diagram symbols)

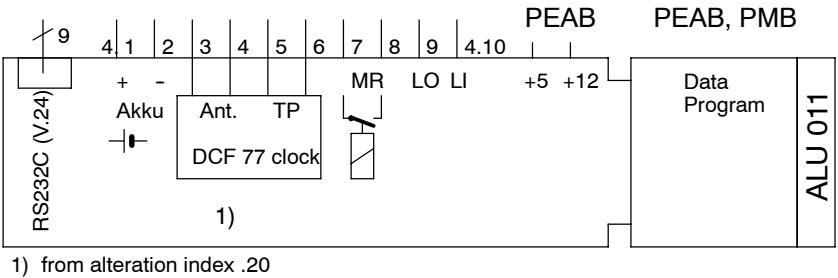


Figure 86 Graphical symbols of ALU 011 ... ALU019

3.12.2 Documentation aids

For the project specific documentation DIN A3 form sheets are available for the (Ruplan) processing. Forced or standard settings of wiring elements are already entered here. These form sheets are

- ☐ included in the form block for conventional processing (see ordering details)
- ☐ included in the A500 data base for Ruplan processing (technical sales office version) (in preparation)

3.13 Software notes

3.13.1 EQL list

The basic software of the ALU enters zero in the EQL list for the reserved slot of the previous monitoring module (e.g. UKA 024) so that its explicit standardization is not required.

3.13.2 Assignment of markers to error indications or messages

Table 44 Reserved markers

Type	Marker	Indicator for an error	Comments
Plug-in check	20/30 *	- - -	The ALU cyclically checks whether the plug-in check is alright with the program running (LI-LO loop is closed) if yes <20>, <30> = 0
Monitoring the battery backup	23/33 *	LED 'bat'	The ALU checks whether there is undervoltage for the battery after the PC has been started, if yes <23,33> = 1 after the start of the program. This corresponds to a data loss, if there is undervoltage for the battery when the mains is switched on (see section 3.5.2 Q key)
Battery status test	28/38 *	LED 'batt'	The ALU checks whether there is an undervoltage for the battery with the program running (e.g. every 30 min.); If yes <28>, <38> = 1.
Program run check	60	LED 'run':ON :OFF	<60> = 0: No group error has occurred <60> = 1: Group error has occurred; the normally closed of the pilot relay opens The marker is to be set by the user program. If this is not carried out, ensure that <60> = 0 when the program is started

*) since bootloading/hot restart



Caution Marker 60 is to be defined by the user.

4 Specifications

4.1 Allocation	
Product family	Modicon
Device	A500
Structure	reserved slot in the subracks of the controller (DTA 024, DTA 27.1, DTA 028, DTA 101, DTA 107)
4.2 Supply interface	
internal (system bus)	typ. +5 V / 2.4 A (max. 2.9 A)
RS 232C (V.24)	typ. +12 V/ 100 mA (max. 120 mA) (without PEAB load!)
CMOS backup	≤ 0.5 mA with 3.6 V
4.3 Data interface	
PEAB	parallel I/O bus
RS 232C (V.24) Transmission rate	serial interface according to DIN 66 020, non-isolated 1200 ... 19200 baud
4.4 Processor type	
Intel 80C186	Microprocessor (16 bit) for processor
Intel 80C187	Numeric coprocessor (16 bit)
Clock frequency	16 MHz
4.5 Memory modules	
RAM/EPROM construction	32 pole DIL chassis
RAM/EPROM capacity	128 kbytes per module
RAM/EPROM access time	70/ 120 ns
4.6 Basic software	
ALU 011DE / 012DE	BSW183DE - Dolog V 5.xx (512 kbytes)
ALU 011EN / 012EN	BSW183EN - Dolog V 5.xx (512 kbytes)
ALU 021DE	BSW184DE - Dolog V 6.xx (512 kbytes)
ALU 021EN	BSW184EN - Dolog V 6.xx (512 kbytes)
4.7 Software clock	(software in preparation)
Frequency stability	± 50 ppm
Temperature characteristics	- 10 °C ... + 70 °C, +10 /-120 ppm
4.8 Physical characteristics	
Module	Double Europe format according to DIN 41 494
Format	Size 6HE /4T
Weight	550 g
4.9 Type of connection	
PEAB, PMB	2 C64M plug connectors according to DIN 41 612
RS 232C (V.24)	9 pole sub-D socket connector
Special signals	10 pole or (2 + 8) pole screw-/plug-in terminal for cable cross-sections 0.25 ... 2.5 mm ²

4.10 Environmental characteristics

Standards	VDE 0160
System data	see user manual of A500
Slot width	8T (4T dummy front plate) with natural cooling 4T with forced cooling
Operating temperature	
with 8T width	0 ... 40 °C with natural convection 0 ... 55 °C with forced cooling
with 4T width	0 ... 40 °C with forced cooling
Power dissipation	typ. < 13.5 W (max. 16 W)

4.11 Ordering details

Module ALU 011	424 272 546
(with basic software in German)	
Module ALU011EN	424 276 451
(with basic software in English)	
Module ALU 021	424 277 559
(with basic software in German)	
Module ALU021EN	424 277 560
(with basic software in English)	
EPROM (128 kbytes)	424 075 325
RAM (128 kbytes)	424 075 323
intel 80C187	424 075 292
Programming cable YDL 052	424 244 878
Lithium battery BAT 001	424 241 541
Dummy plate 6HE/4T	424 280 031
A3 form block	A91V.12 - 234 720

Subject to technical alterations!

ALU 061, ALU 071

Central Processing Unit

Module Description

The ALU 061 resp. ALU 071 is one of the central processors for the A500 programmable controllers. It can be operated in the following sub-racks: DTA 024, DTA 27.1, DTA 028 and DTA 107 but not in the DTA 101 due to the weaker DNO 028.

The following functions are realized on the module which consists of two printed boards:

Central processor (CPU)

- Matching control for the parallel I/O bus (PEAB)
- Memory bus control (PMB)
- Data and address bus with a breadth of 32 bits, dynamic switch-over of the breadth of the data bus from 32 to 16 bits, therefore compatible down to the 8086 microprocessor
- Memory for basic software
(standard equipment 512 kbyte EPROM)
- 128 kbyte memory for process data and max. 384 kbyte memory for user programs in RAM/EPROM
(standard equipment: 128 kbyte system RAM)
- Serial interface (RS232C, V.24)
- Real-time clock

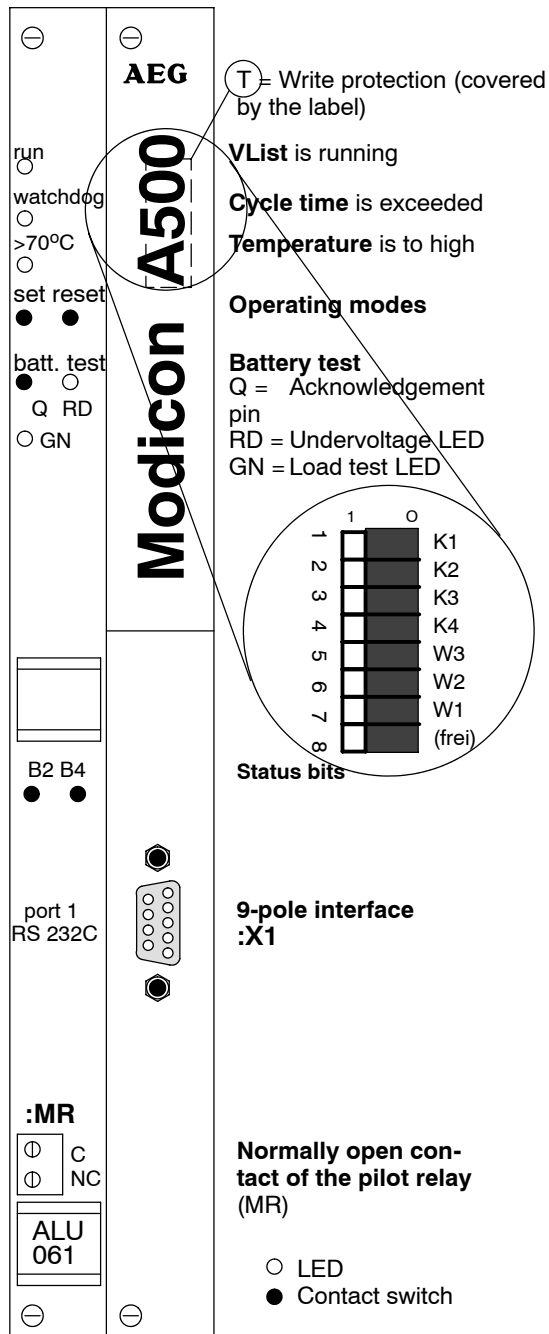
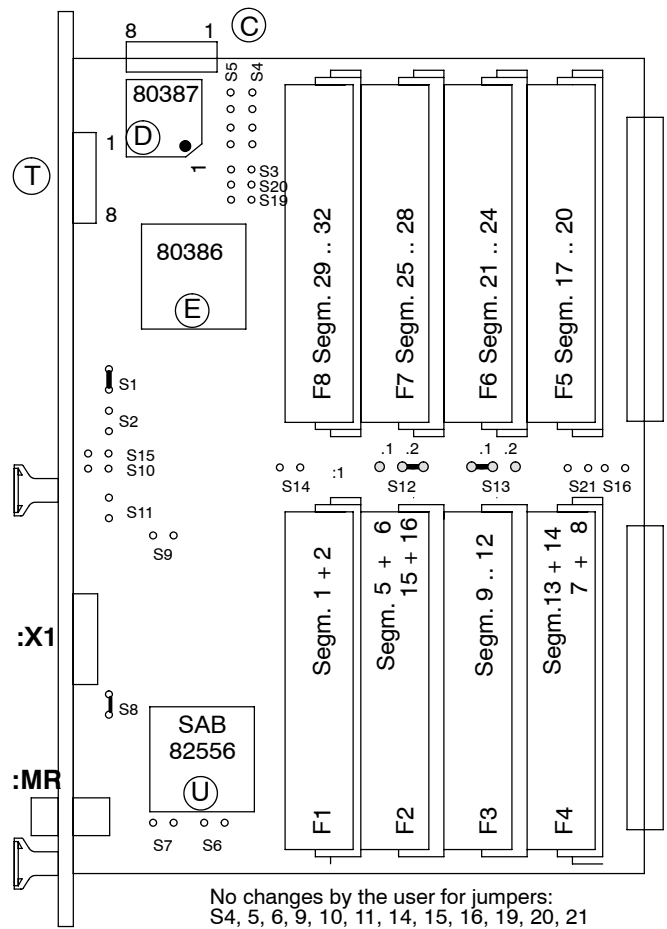


Figure 87 Front View of the ALU 061 resp. ALU 071



Fn:	Memory Fields	(3.2.3)
F2...F4:	User Software Module,	128 kbytes or 512 kbyte for F1
F5...F8:	Basic SW Module (ALU061)	128 kbytes or 512 kbytes for F8
F7, F8	Basic SW Module (ALU071)	128 kbytes
(C):	Setting Status Bits	(3.4)
(D):	Numeric Data Processor	
(E):	Central Processor	
MR:	Pilot Relay	(3.7.1)
S1, 2:	Type of Memory	(3.2)
S8:	Start-Up Characteristics	(3.1)
(T):	Switches for Baud rate, Write Protection	(3.4)
(U):	Interface Controller	
X1:	Interface Connector	(3.7.2)

Figure 88 Survey of the Configuration Elements for ALU 061 resp. ALU 071

1 General

The ALU 061 resp. ALU 071 unites the central processor of the device, an expandable numeric data processor, 128 kbyte RAM for the system RAM, 384 kbyte RAM/EPROM for user programs and a 512 kbyte EPROM for the basic software in one module. For ALU 071 from version 6.xx an obligatory software basic part may be added by a loadable basic software part. Specified RAM equipments result in jumper variations (see chapter 3).

The connection of the CPU with the A500 busses of PEAB and PMB and the necessary monitorings for the controller are accommodated on another pluggable printed-board assembly. A separate memory module and the monitoring module (UKA nnn) is therefore unnecessary so that the PEAB slot 1 which was reserved for this is available with limits.

For configuration measures for interrupt scanning please refer to the Chapter 3, Configuration.

The operating function of “real-time program” is not yet available for the already equipped real-time clock for log functions.

A 2-fold processing speed is available depending on the degree of memory assignment, the possible equipment with the coprocessor and the input/output scope as opposed to the ALU 011 and a processing speed of up to 8 times the speed of ALU 150.

1.1 Physical Characteristics

The hardware of the ALU 061 resp. ALU 071 module consists of 2 printed boards with double Europe format (6 HE), a front panel with a breadth of 8T and various operating, indicating and port elements as well as the basic software. The boards have a multi-layer structure and all the memory modules are arranged obliquely in the printed board to save on equipment height.

The current version of the basic software is accommodated in the EPROM memory are.

Available versions see chapter 3.2.6.

The main components of the module are:

- ❑ 80386 microprocessor for the processor
- ❑ 80387 microprocessor is optional as a numeric data processor
- ❑ Memory slots for several RAM and/or EPROM types as well as alternative supplements see Figure 92
- ❑ Real-time clock with date and calendar functions (the “real-time programming” operating function is not yet available)
- ❑ RAM backup with a rear supply from the system rechargeable battery in the subrack and the BAT 001 lithium battery which can be plugged in on the front to enable the module to be removed without losing any data
- ❑ Front interface for programming panels
- ❑ Rear interfaces for I/O bus (PEAB) and memory bus (PMB)
- ❑ Rechargeable battery charging circuit with test functions
- ❑ DIP switch area for setting the write protection
- ❑ Monitoring functions for the program sequence and rechargeable battery voltage
- ❑ Operating mode selection for the user program

1.2 Mode of Functioning

The central processor fulfills the following tasks:

- ❑ Creating the internal processing clock
- ❑ Organization of the internal data traffic on the I/O bus between all the units
- ❑ Writing the process input signals into the signal memory
- ❑ Processing the user program
- ❑ Saving any intermediate results (markers) in the signal memory
- ❑ Outputting the process output signals from the signal memory
- ❑ Operating the serial interface for program transfers
- ❑ Monitoring the signal and program memories, processor sequence (with self test), program circulation, supply voltage and rechargeable battery voltage
- ❑ Monitoring the ALU ambient temperature

2 Operation / Presentation

The module has the following operating and indicating elements starting at the top of the front panel:

- | | | |
|---|---------|--|
| ❑ green “run” LED | lit up: | User program is running over END block, cycle monitoring time is not exceeded, pilot relay has picked up |
| | dark: | User program has not been started or processor sequence is faulty, cycle monitoring time has been exceeded
marker 60 = 1, pilot relay has dropped out |
| ❑ red “watchdog” LED | lit up: | User program is not running within the max. permitted cycle time |
| | dark: | User program is running |
| ❑ red “>70 °C” LED | lit up: | Access temperature has been reached.
For evaluation, see section 3.9.2 |
| ❑ “set” contact socket
(operating modes) “reset” | | boot loading see start-up characteristics
Break see start-up characteristics |



Warning The possibilities of the “reset” socket may not be used in the standard system operation. The program abortion does not guarantee the system to be stopped according to the commands without the loss of data.

<input type="checkbox"/> "batt" contact socket (acknowledgement pin)	Insertion deletes the rechargeable battery undervoltage indicator (red "batt. test" LED), initiates and immediate rechargeable battery load test and enables a disabled program		
<input type="checkbox"/> red "batt test" LED	lit up:	Undervoltage for the rechargeable battery at the time when the system is switched on	
	dark:	"good" rechargeable battery voltage or it has not been tested.	
<input type="checkbox"/> green "batt" test LED	lit up:	with a successful load test	
	flashes:	if there is undervoltage after the rechargeable battery has been tested	
		For more details, see section 3.3.2	
	dark:	Undervoltage for the rechargeable battery between 2 load tests	
<input type="checkbox"/> B2 contact socket B4	B500 or P150 transparent mode Single bit entry		
<input type="checkbox"/> DIP switches	K1 ...	K3	Baudrate selection depending on the switch combination
	K4		Write enable for segments 21 - 24
	W3		for segments 5+6, 15+16
	W2		for segments 9 - 12
	W1		for segments 13+14, 7+8
	without marking		for segments 17 - 20
<input type="checkbox"/> Port connector	RS 232C interface 9 pole socket block to connect programming panels and supply an external backup voltate		
<input type="checkbox"/> MR terminal	used as a normally open contact of the pilot relay for the deadman's function (watchdog)		

3 Configuration

The following are to be configured for the module:

- ☐ Equipment of the memory areas
- ☐ Baudrate
- ☐ Program operating mode
- ☐ Assignment of the terminals
- ☐ "Access temperature indicator" evaluation
- ☐ Equipment with the numeric data processor

The spatial arrangement for equipment, operation and setting jumpers is to be taken from Figure 87 and Figure 88 and the section numbers of the relevant configuration measures.



Caution The ALU 061 resp. ALU 071 module must be screwed to the subrack to discharge electromagnetic interference which possibly enters the system via the data cable.



Caution Interruptable modules on PEAB
When interruptable modules such as SES 2 or SEA 020 are used, the scan chain must be extended to include also the present 'UKA' slot (address 00) to the left of the ALU. For this the terminals a15 and c15 of the PEAB connector should be connected with the suitable jumper. All other nodes on this PEAB slot generate this connection automatically. Otherwise the ALU cannot process the interrupts and does not call the V lists.

Note for the bootloading of an A500 programmable controller:



Caution In case of the simultaneous use of the functions TI and AKF on Modnet 1/SFB, faulty signals can appear with respect to the V.24 operation. If still the user program is started, this fault does not appear after that.




Note The bitbus is switched off with the following combination of pin and switch:

- ☐ Battery acknowledgement pin is inserted
 - ☐ B1 = OFF or OPEN
 - ☐ Reset with pin or power supply OFF/ON
- No bitbus menu appears with the function EQL, only the PROMPT <ADDR:> appears.

3.1 Setting the Start-Up Characteristics

The start-up characteristics of a programmable controller are determined by the operating modes of the central processor. The ALU 061 resp. ALU 071 has the S8 jumper for this (corresponds to the M5 jumper for UKA ...) and the "set" contact socket:

Automatic Start:  **S8 (Figure 88, M)**

Automatic start of the PLC when the supply voltage is switched on if a program panel is not connected. No automatic start if a programmable panel is connected and switched on.

Manual Start:  **S8 (Figure 88, M)**

The PLC remains as stopped when the supply voltage is switched on and must be started manually via the programming panel.

Boot Loading: **'set' is Plugged in Contact Socket in the Front Panel (Figure 87)**

- ☐ at the start of the program
- ☐ when the mains is switched on
- ☐ when the activated "reset" pin is plugged in

A few standardizing cycles are executed with the boot loading. The Dolog B blocks with initial state characteristics are standardized here. Blocks which are not processed in the cycles are not standardized (e.g., interrupt Vlists). Moreover the system variables will be restored automatically.

Further standardizations which are over and above this scope are to be realized by the user by means of a program.

Hot Restart: **'set' is not Plugged, 'reset' is not Plugged**


The PLC generally continues the program at the interrupted point with the saved signal memory data.

3.2 Memory Functions

3.2.1 Address range


The addressing of MME 002 or MMR 002 will be adapted by inserting the jumpers S1 and S2:


☐ S1  MME 001 containing 1 ... 4 x 128 kbyte for F5 ... F8

☐ S1  MME 002 containing 1 x 512 kbyte for F8

MMR 001 (128 kbyte) can be replaced by MMR 002 (512 kbyte) without limitations. However, in this case the memory capacity used is only 128 kbyte.

When MMR 002 is inserted in slot F1, the following alternatives are available:

☐ S2  1 ... 4 x 128 kbyte are used on slot F1 ... F4

☐ S2  1 x 512 kbyte are used on slot F1.
All other MMR / MME on the slots 2 ... 4 must be removed.
The segments 1+2 and 5 ... 16 are then entirely in F1.
That means, the programs, which were available on EPROM earlier, can be used only after loading in the corresponding RAM.

Further limitations:

The write enable switches W1, W2, W3 are inactive, i.e. write protection is not possible. However, all RAM contents can be battery backed-up.

Possible equipment alternatives are shown in Figure 92.

3.2.2 PMB range

Extension of PMB area from segment 3 - 4 to segment 3 - 6 with MMR 001:

S3  segment 3-4 S3  segment 3-4, 5-6

Extension of the PMB area (S3 inserted) is not possible when the full capacity of the MMR 002 should be used (S2 inserted).

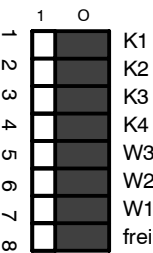


Note S3 is available for ALU 061 from index .04 and for ALU 071 from index .01.

Declarations to 1 MB Address Area

The memory areal of the ALU 061 resp. ALU 071 is designed to receive 8 memory modules (see Figure 88). Variants of equipment see Figure 92. Each memory module MMR 001 / MME 001 occupyes 4 segments and each memory module MMR 002 / MME 002 occupyes 16 segments. They are contacted via a 68 pole powerless connector on the CPU board.

Write Protection:



Out of the 32 segments 1 ... 4 are reserved for the system RAM. They always have write enable. For the memory modules of the slots F2 to F6 DIP switches are assigned for setting the write protection (W = write). These can be operated, after removing the label “Modicon A500” , from the front plate window. (see the table at the end). According to the labeling for the given segments the write enable (WE) is switched off (write inhibit) in position 0 and switched on (write enable) in position 1. The equipment with RAM modules is the precondition for the possible write protection.

Switch	Segments	Address range
-	1 + 2	00000 ... 1FFFF
K4	17 ... 20	80000 ... 9FFFF
W3	5 + 6	20000 ... 2FFFF
	15 + 16	70000 ... 7FFFF
W2	9 ... 12	40000 ... 5FFFF
W1	13 + 14	60000 ... 6FFFF
	7 + 8	30000 ... 3FFFF
(frei)	21 ... 24	A0000 ... BFFFF (or without labeling)

For the DIP switches of K1 ... K4, see section 3.4
If S2 is inserted, DIP switches W1 to W3 have no function

3.2.3 Field 1: Data Area

Field 1 is reserved to save system data in a 128 kbyte signal in-line memory module (MMR) equipped with SRAM elements.

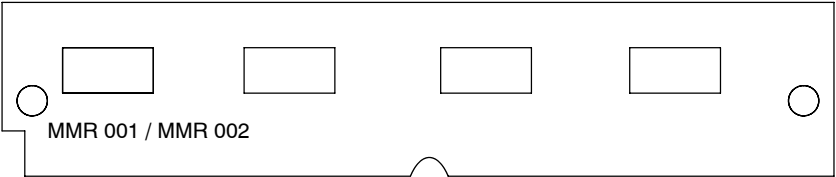


Figure 89 SRAM Module on ALU 061 resp. ALU 071

3.2.4 Fields 2 ... 4: User Program

These fields are to be equipped with 3 MMR or MME memory modules. These modules are not part of the standard technique. The user program can also be saved in different module types.

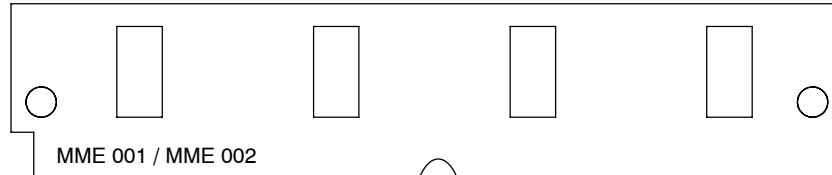


Figure 90 EPROM Module on ALU 061 resp. ALU 071



Caution The spatial arrangement of the segments is changed in comparison to the previous version.
The segments 7 + 8 in field 2 are exchanged with the segments 15 + 16 (SYKON/SYRES) in field 4. Therefore SYKON/SYRES should be equipped in field 2.

3.2.5 Operating the Memory Modules

The dead connectors to receive the memory modules are freely accessible.

A special operation simplification including reverse voltage protection is achieved for the user by a notch in one of the board sides.



Warning The following is valid when inserting or removing a module:

1. A module must be changed with the voltage supply to the ALU 061 resp. ALU 071 switched off.
2. The regulations for operating CMOS components must be observed at all costs (e.g., carrying out work on a earthed working plate).
3. Remove BAT 001 if plugged in.

Inserting a Memory Module

Remove the module from the packaging and turn it so that the printed label, e.g., MMR 001, can be read. The port contacts on the lower edge and the 1 and the coded section are then on the left.

Stage 1 Insert the module obliquely into the corresponding connector.

Stage 2 Carefully press the module downwards with your two thumbs on the two upper ends until it clicks in.
Check whether the lateral locking hooks hold down the memory module.

Removing a Memory Module

Stage 3 Press the lateral locking hooks outwards with your two thumbs until the module leaves its inserted position due to spring force.

Stage 4 Remove the module.

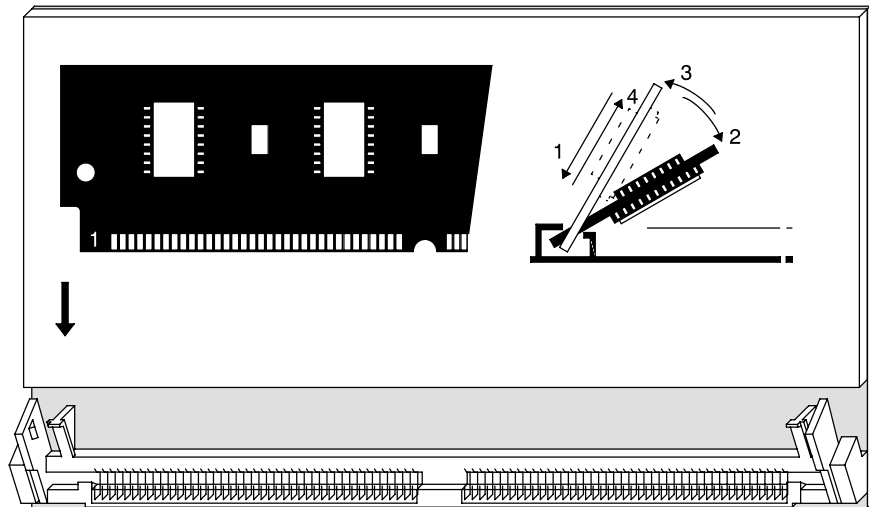


Figure 91 Removing a Memory Module on ALU 061 resp. ALU 071

3.2.6 Fields 5 .. 8, Basic Software

ALU 061

Re-productions contain for slot F8 only the basic software BSW981DE resp. BSW 981EN in 1x MME 002 instead of the basic software BSW381DE resp. BSW381EN in 4x MME 001 for the slots F5...F8.
Delivered modules may be realized in both variants. Additional to BSW9xx the jumper S1 is plugged in.
Repair inputs containing BSW381DE resp. BSW381EN in 4x MME 001 will be sent back in the same version – as far as possible.

ALU 071

Re-productions contain for the slots F7 and F8 only the basic software BSW982DE in 2x MME 002 instead of the basic software BSW382DE in 2x MME 001 (also for the slots F7 and F8).
Delivered modules may be realized in both variants.
The now possible version in English is exclusively loaded in 2x MME 002 named BSW982EN. In all three cases jumper S1 is removed.
Repair inputs containing BSW382DE in 2x MME 001 will be sent back in the same version – as far as possible.

BSW extensions are equipped alternatively as RAM or EPROM on the fields F5 (segment 17 ... 20) and F6 (segments 21 ... 24).
For RAM equipments in segment 17...24 is required: S7 inserted and S12 in position .1. See arrangement in Figure 88.

Repair, Test shop

Untill further notice the specific software is available in both EPROM types (MME 001, MME 002). Their contents are identical, even if the designation differs between MME 001 and MME 002 and the index differs by 1.

Overview Memory Equipment ALU 061 / ALU 071

Figure 92 shows in tabular form four possible equipment alternatives for ALU 061 and two for ALU 071 with their corresponding jumper positions.

The obligatory settings of the jumpers S1 ... S12 are represented there.

ALU 061					ALU 071	
	Variante 1	Variante 2 **)	Variante 3	Variante 4	Variante 1 **)	Variante 2
F1 Kap. Typ Segm.	128 kB RAM *) 1+2	128 kB RAM 1+2	512 kB RAM 1+2, 5...16	512 kB RAM 1+2, 5...16	128 kB RAM 1+2	512 kB RAM 1+2, 5...16
F2 Kap. Typ Segm.	128 kB RAM/EPROM 5+6, 15+16	128 kB RAM/EPROM 5+6, 15+16	---	---	128 kB RAM/EPROM 5+6, 15+16	---
F3 Kap. Typ Segm.	128 kB RAM/EPROM 9...12	128 kB RAM/EPROM 9...12	---	---	128 kB RAM/EPROM 9...12	---
F4 Kap. Typ Segm.	128 kB RAM/EPROM 13+14, 7+8	128 kB RAM/EPROM 13+14, 7+8	---	---	128 kB RAM/EPROM 13+14, 7+8	---
F5 Kap. Typ Segm.	128 kB EPROM *) 17...20	---	128 kB EPROM 17...20	---	128 kB RAM/EPROM 17...20	128 kB RAM/EPROM 17...20
F6 Kap. Typ Segm.	128 kB EPROM 21...24	---	128 kB EPROM 21...24	---	128 kB RAM/EPROM 21...24	128 kB RAM/EPROM 21...24
F7 Kap. Typ Segm.	128 kB EPROM 25...28	---	128 kB EPROM 25...28	---	128 kB EPROM 25...28	128 kB EPROM 25...28
F8 Kap. Typ Segm.	128 kB EPROM 29...32	512 kB EPROM 17...32	128 kB EPROM 29...32	512 kB EPROM 17...32	128 kB EPROM 29...32	128 kB EPROM 29...32
S1						
S2						
S3	2)	2)			2)	
S7						
S12						

*) RAM = MMR 001 or MMR 002; EPROM = MME 001 or MME 002

**) Version as delivered

1) inserted or inserted on .1, if F5 and/ or F6 is equipped with RAM

2) S3 can be inserted or not as required

Figure 92 Memory Equipment and Corresponding Jumpers

3.3 Backup Battery and Monitoring the Backup

3.3.1 Supplying the Backup Voltage

You can choose between two different sources for the supply of the SRAM modules.

- central rechargeable battery in the subrack with standard operation
- external battery via an interface connector to be disconnected/plugged in



Warning If the module is disconnected from the subrack without an external battery being connected, you must expect data losses!

Internal Backup (Figure 88, I):

The backup generally takes place via the rechargeable battery in the controller subrack. The PMB carries out the supply.

If an additional backup voltage is supplied via the 9 pole interface connector (RS-232C), the module can be disconnected without losing any information.

The lithium battery block (BAT 001) with a 9 pole plug-in port is available here. It is fed via contacts 5 and 9 of the interface connector (see also Figure 96):

Pin 9: $+U_{\text{Batt}}$ (max. 5 V)

Pin 5: GND

3.3.2 Monitoring Functions

If the operating voltage of +5 V is valid for the memory elements and if a rechargeable battery test was not carried out, the rechargeable battery is loaded with approx. 100 mA. If the operating voltage does not reach 4.75 V, the supply of the entire memory is switched to the rechargeable battery.

The rechargeable battery test is repeated every 4 hours independently of the user program. It can also be triggered at any time via the "batt" contact socket (acknowledgement pin). The rechargeable battery is loaded with approx. 1 A for 1 sec in both cases.

Result of the Measured Value:

$U_{\text{Batt}} > 3.2 \text{ V}$: The rechargeable battery quality is normal;
the green LED is permanently lit up

$U_{\text{Batt}} < 3.2 \text{ V}$: The rechargeable battery quality is insufficient. Marker 23 or 33 is set and the green "batt" LED flashes with approx. 1 Hz

"batt" socket If the battery voltage does not permanently remain under 3.2 V after the

load test, the message can be acknowledged with the "batt" pin (the marker is reset; the green LED lights up permanently).

3.4 Setting Status Bits

There are 2 code switches on the module

- Switches 1.1 ... 1.8 in the front panel behind the cover

	1	0		110	300	1200	2400	9600	19200	Baud
1			K1	0	1	0	1	0	1	Selection via 3 DIP switches
2			K2	0	0	1	1	0	0	Other switch combinations are not
3			K3	0	0	0	0	1	1	permitted. Example: 9600 Baud
4			K4	Segmente 21 - 24						Write protection for segments 5 - 24 (only if S2 is removed)
5			W3 :	Segmente 5 + 6, 15 + 16						
6			W2	Segmente 9 - 12						
7			W1	Segmente 13 + 14, 7 + 8						
8			frei	Segmente 17 - 20						
bzw. nicht beschriftet										
			= position "0"						= position as delivered	

The DIP switches show the position as delivered

The DIP switches show the position as delivered

Figure 93 Kodierschalter 1.1 ... 1.8 für Baudraten- und Speicherschutz-Festlegung

- Switches 2.1 ... 2.8 on the upper edge of the ALU 061 resp. ALU 071

	1	0		
1			B4	Single bit evaluation; can be defined using the software
2			B3	Single bit evaluation; can be defined using the software
3			B2	B500 or P150 transparent mode
4			B1	set pin evaluation (Chapter 3.1)
5			free	(initiates Boot-loading, restore of system variables)
6			E	single bit entry
7			G	Sensor bit standardization
8			reset	"reset" pin evaluation (Chapter 3.6)

The code switches of 2.3 and 2.1 are switched in parallel to the contact sockets of B2 and B4 in the front panel

Figure 94 Code Switches 2.1 ... 2.8 for Status Bits on ALU 061 resp. ALU 071

3.5 Program Sequence Monitoring

3.5.1 Monitoring the Basic Software Sequence

The activities of the cooperation between the processor and basic software are monitored. Module-internal cycles and those which are assigned to the PEAB and PMB periphery interfaces have monitoring times of different lengths. They are switched over automatically. A "reset" start for the user program is suppressed if the time is exceeded.

For more details, see section 3.1

3.5.2 Monitoring the User Software Sequence

The sequence of the user software is monitored by measuring the cycle time. The cycle monitoring time is adapted automatically to its circulation time for a number (specified in the software) of Vlist circulations after the start of the Vlist. The maximum value of the digital word multiplied by the factor 2 is then entered in the counting register of the timer (digital word 2).

If a Vlist is to be started and its running time is shorter than the previous one, the digital word 2 is to be standardized at the start by inserting the "set" pin (boot loading) so that a re-adaptation can take place. However, if the Vlist is longer than the previous one, the adaptation is carried out automatically.



Warning If long program parts which considerably extend the program circulation time, e.g., bus networking, are enabled after the start (or during the sequence) of the user program, the dead man's function can detect an excess of the monitoring time and cause the pilot contact to drop out.

This involuntary interruption can be suppressed if the cycle monitoring time saved in the digital word 2 is significantly enlarged using a program block (e.g., with an ADD) or a programming panel (PADT).

However, you are warned before extending the time since the value can then impair the monitoring function.

3.6 Program Abortion

Program Abortion Disabled

Code switch 2.8 to 0 ☒ ☐

Inserting the "reset" pin has no effect

Program Abortion Permitted

Code switch 2.8 to 1 ☐ ☒

A program break is initiated if the "reset" pin is plugged in, whereby it is not guaranteed that the user program will stop in accordance with the commands and without any data losses. This possibility may therefore not be used in the standard system operation (thus locked via 2.8).

3.7 Ports and Interfaces

3.7.1 Screw/Plug-In Port

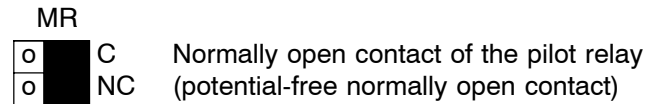


Figure 95 Terminals of the Pilot Contact

3.7.2 RS 232 C Plug-In Connection (Programming Panel and BAT 001)

Figure 96 shows the pin assignment of the RS 232C socket on the ALU 061 resp. ALU 071 .

“PG” signal column This is valid for the signal assignment if a programming panel is connected

”BAT 001” column This is valid for the connector assignment of the BAT 001 battery block which permits the backup of the CMOS elements via this interface even if the module is disconnected.

See also section 3.3.1.

The metallic chassis of the socket is connected to the front panel.

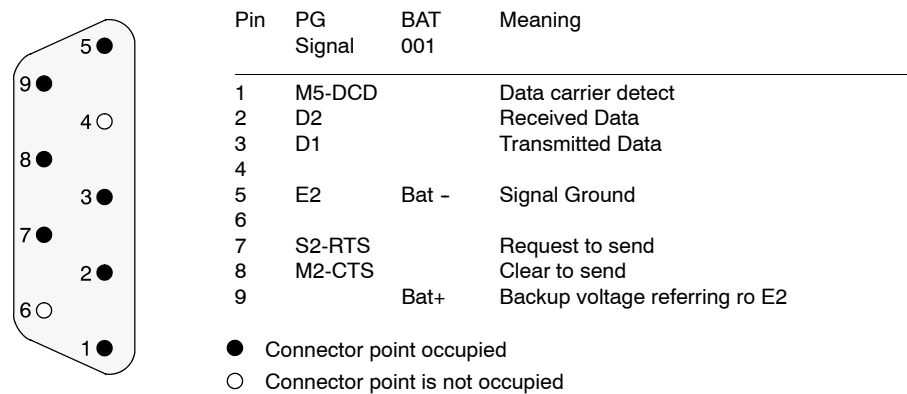
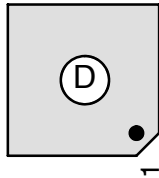


Figure 96 Pin Assignment for the RS 232 C Connector Looking at the Cable Solder Port of the Pin Connector (ALU 061 resp. ALU 071)

3.7.3 YDL 052 Programming Cable

The ALU 061 resp. ALU 071 is connected to the P500 (-AT) programming panel via the RS 232C serial interface with the YDL 052 cable. Figure 96 shows the port assignment of the connector and the names of the present signals.

3.8 Numeric Data Processor 80387



Der numeric data processor can be plugged in as an option. A corresponding socket (Figure 88, D) is already present. However, no plug-in jumpers whatsoever are needed since the central processor detects the existence of the 80387 with its software.

When inserting the numeric data processor ensure that the cut-off corner of the chassis designated with a dot covers the socket corner designated with “1”. The component is to be pressed in evenly.



Warning Remove the Component with a Suitable Tool only!

Table 45 Recommended Tool for Removing the Numeric Coprocessors

Typ	Manufacturer/Supplier
TX 8136-11x11	Fa. Augat 8000 München, Tel. (089) - 6 12 90 90
TW 2011	Fa. State Electronics 5409 Holzappel, Tel. (06439) - 70 24

3.9 Software Notes

3.9.1 Real-Time Clock

The real-time clock manages the parameters

Time of day: Second, minute and hour

Calendar: Week day, today's date, month and year, leap-years are corrected automatically.

The clock is set by the software. There are no hardware settings to be made. The time information is saved in the digital words 60 ... 64. Therefore it is also available to other routines.

The clock depends on the backup battery of the subrack; it therefore continues to run even when the supply voltage switched off. It is supplied via the BAT 001 lithium battery which can be plugged in if the module is disconnected.

3.9.2 Assignment of Markers to Error Indicators or Messages

Table 46 Reserved Markers set on ALU 061 resp. ALU 071

Type	Marker	Indicator if there is an Error	Comments
Plug-in check	20/30 *	- - -	no longer present
Access temperature	22/32 *	>70°C LED	Access temperature is reached. The evaluation of this message (e.g., reaction in the user program) is to be carried out by the user
Monitoring the battery backup	23/33 *	'batt' LED	The ALU checks whether there is a battery undercoltage after the PLC start; if yes, <23, 33> = 1 after the program start. This corresponds to a loss of data if there was a battery undervoltage at the time when the power supply was switched on. (see section 3.3.2, "batt" acknowledgement pin)
Battery status test	28/38 *	'batt' LED	The ALU checks with the program running (e.g., every 4 hours) whether an undervoltage has occurred during the battery test; if yes: <28, 38> =1.
Program sequence check	60	'run' LED: On Off	<60> = 0: no group error has occurred <60> = 1: group error has occurred, normally open contact of the pilot relay opens The marker is to be set by the user program. If this does not occur, ensure that <60> = 0 at the start of the program!

*) since boot loading/cold start restart



Caution Marker 60 is to be defined by the user.

3.10 Dokumentation

DIN A3 form sheets are available for the (Ruplan) processing for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- ☐ included in the form block for conventional processing (see ordering data)
- ☐ included in the A500 data bank for Ruplan processing (technical sales office version) (in preparation)

3.11 Standard Settings for B500-3 (from Index .06)

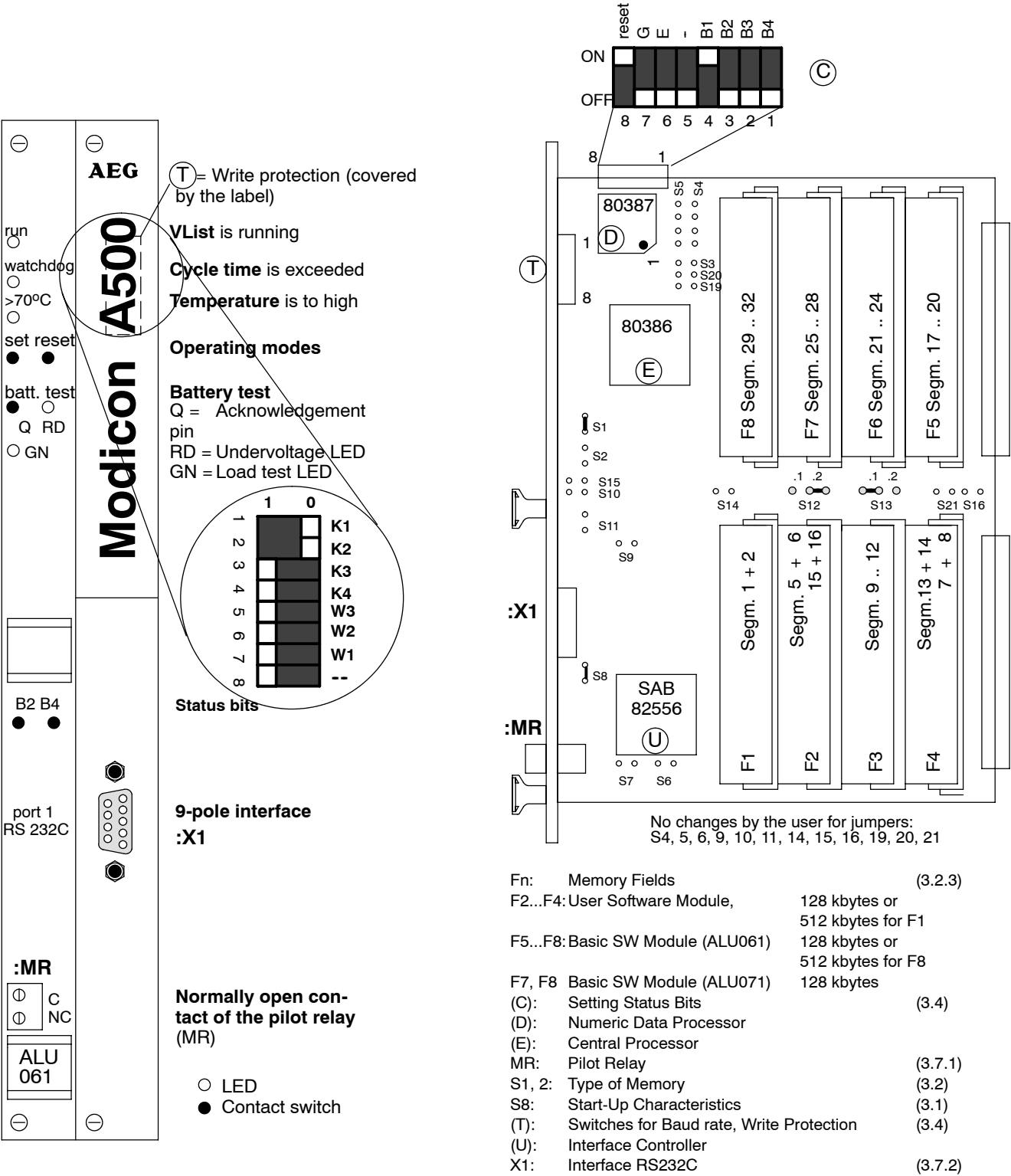


Figure 97 Standard Settings on ALU 061 for B500-3 (from index .06)

4 Specifications

4.1 Assignment		
Product Family	Modicon	
Device	A500	
Structure	reserved slot in the controller subracks (DTA 024, DTA 27.1, DTA 028, DTA 107)	
4.2 Supply Interface		
Internal (System Bus)	+5 V, typically 4.4 A, max. 6.3 A +12 V, typically 0.1 A, max. 0.15 A	
4.3 Data Interface		
PEAB	Parallel I/O bus	
RS 232 C (V.24)	serial interface according to DIN 66 020, non-isolated	
Transmission Rate	110 ... 19 200 baud	
4.4 Signalling Relay MR		
Type	Normally open contact	
Working voltage	≤ 60 VDC	
Load current	≤ 0.1 A	
Switching capacity	≤ 5 VA	
4.5 Processor Type		
Intel 80386	Microprozessor (32 bits) for processor	
Intel 80387	Numeric coprocessor	
Clock Frequency	16 MHz	
4.6 Memory Modules		
Construction	Special format with memory elements soldered on	
EPROM Type	MME 001	MME 002
capacity each module	128 kbytes	512 kbytes
basic SW type V5.xx	BSW381DE/EN	BSW981DE/EN
basic SW type V6.xx	BSW382DE/EN	BSW982DE/EN
RAM Type	MMR 001	MMR 002
Capacity each module	128 kbytes	512 kbytes
Access Time	70 ns	
4.7 Backup Battery		
NiCd Rechargable Battery	in the primary subrack	
Lithium Primary Cell	to disconnect the subrack without loosing any data (BAT 001)	
4.8 Physical Characteristics		
Module Format	Size: 6HE / 8T Double Europe format according to DIN 41 494	
Structural Form	extensively surface-mounted (SM technique)	
Weight	900 g	
4.9 Port Type		
PEAB, PMB	2 C64M connectors according to DIN 41 612	
RS 232 C (V.24) or BAT 001	9 pole socket block	
Memory Modules	Edge connector with powerless contacting	

4.10 Environmental Conditions

Regulations	VDE 0160, UL 508
System Data	see A500 user manual
Power Dissipation	typically < 22 W

4.11 Ordering Data

with German Basic Software:

ALU 061 Module	424 272 532
ALU 071 Module	424 277 561

with English Basic Software:

ALU 061EN Module	424 272 533
ALU 071EN Module	424 277 562

Programming Cable YDL 052	424 244 878
BAT 001 Lithium Battery	424 241 541

Numeric Coprocessor	424 075 242
---------------------	-------------

MMR 001 ²⁰⁾	424 240 058
MMR 002 ²¹⁾	424 277 575
MME 001 ²⁰⁾	424 240 060
MME 002 ²²⁾	424 277 574

Shorting plug	
(yellow 22 mm)	424 150 126
(red 12.5 mm)	424 210 072

Terminal strip two-pole	424 247 035
-------------------------	-------------

EPS 386	424 271 033
ADP 386 Adapter	424 272 063

A3 Form Block	A91M.12 - 234 720
---------------	-------------------

Technical rights reserved!

20) as long as deliverable
21) substitute for MMR 001
22) substitute for MME 001

ALU 150

Central Processing Unit

Module Description

The ALU 150 is the processor and must be inserted in the A350 and A500 primary subracks.

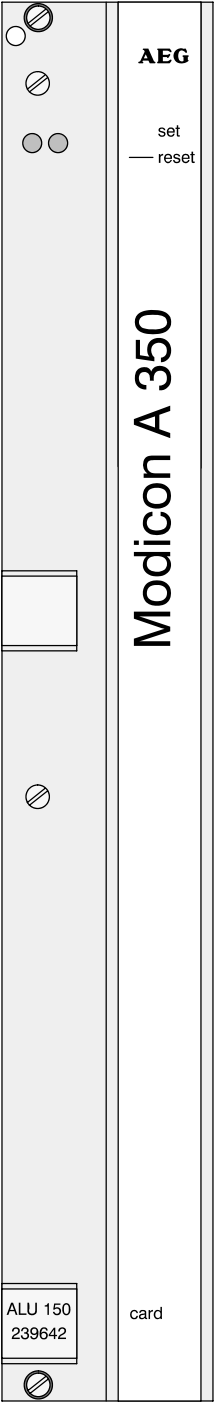
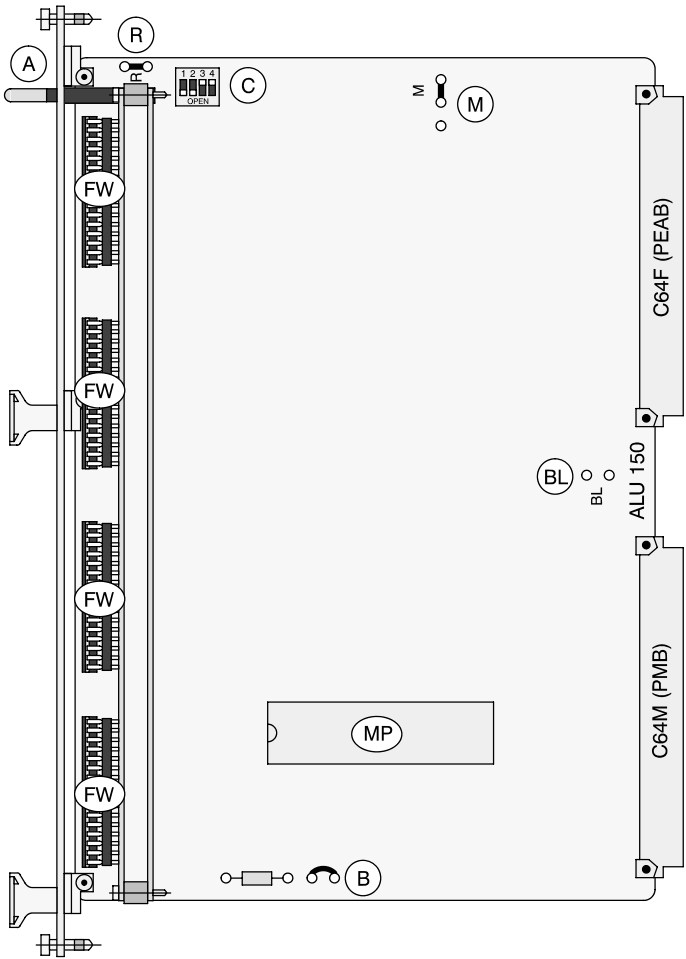
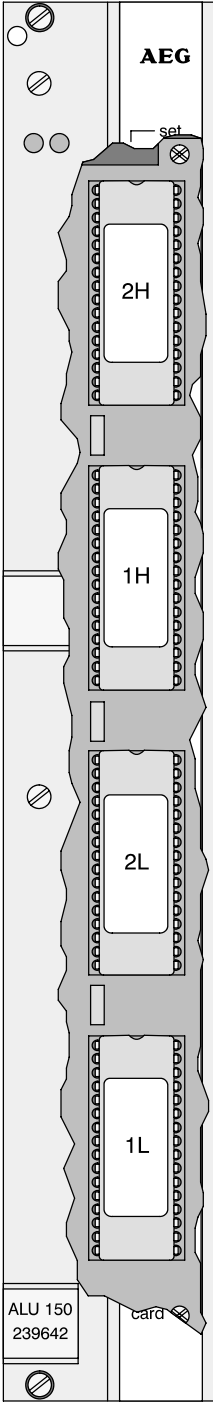


Figure 98 Front view of ALU 150



- A: Contact Sockets set/reset (see 2)
- B: Wire Jumper separated when MAT 827 is inserted
- BL: Battery Charging Connection, (see 3.3)
- C: DIP Switch for Baudrate (see 3.2)
- FW: EPROMs with Basic Software (see 3.1)
- M: Jumper for Determining the Starting Behavior (Automatic Start ↔ Manual Start)
- MP: Microprocessor
- R: Reset jumper for program break (see 2)

The jumpers shown are as delivered. All further jumpers, soldering points and contact combs not shown are necessary for inspection adjustments in the factory; therefore no change may be made to these.

Figure 99 Survey of Configuration Elements ALU 150

1 General

The ALU 150 is the processor and must be inserted in the A350 and A500 primary sub-racks. Its plug location is fixed and details are given in the description of the respective module carrier.

1.1 Physical Characteristics

The module has double European format with 8T width and PMB and PEAB contact. Its essential component parts are:

- ❑ Microprocessor 8086, expansion capability for the arithmetic processor MAT 827
- ❑ 512 Kbyte memory (EPROM) for basic software, inserted in a DIP socket
- ❑ 32 Kbyte memory (CMOS-RAM) for signal and program memory
- ❑ Jumpers, contact sockets and DIP switches for start behavior, baudrate etc. ...

In addition it contains the adaptive control for the parallel I/O bus (PEAB), the memory bus control as well as a RS 232C-interface whose signals are brought out via the SCU.

1.2 Mode of Function

The processor fulfills the following tasks:

- ❑ Production of the internal processing pulse
- ❑ Organization of the internal data transfer on the PEAB between all units
- ❑ Organization of the internal data transfer on the PMB between the memory modules
- ❑ Reading the process input signals into the signal memory
- ❑ Executing the user program
- ❑ Storing the occurring intermediate results (markers) in the signal memory
- ❑ Output of the process output signals from the memory
- ❑ Operating the serial interface for program transmissions
- ❑ Storing and evaluating the monitoring signals for temperature, supply, control loop, program circulation and memory contents (parity error).

2 Operation and Display

The module contains 2 contact sockets for the following functions:

- ❑ Socket "set" Bit 0 of the status word, serves to define the starting behavior after a voltage failure, providing the M jumper of an automatic start is enabled. The status word is queried with a read command.

Inserted: Initial start, i.e. start at the program beginning
Not inserted: Restart, i.e. continuation of the program at the interrupt point
- ❑ Socket "reset" Reset socket for program break (if the contact pin is inserted and the internal jumper R is closed).



Warning The program break attainable using the reset socket (by plugging in) does not guarantee that the program will stop as commanded with data being saved as in the program interrupt after an undervoltage warning. This facility may not be used in regular system operation (therefore the jumper R should be open in normal operation).

3 Configuration

The following are to be configured for the module:

- ❑ Battery charging connection
- ❑ Baudrate (status word)
- ❑ Type of program start
- ❑ Operation without/with additional processor MAT 827
- ❑ Relaying for desired functions (A3 formula)
- ❑ Reset permitted/not permitted

3.1 Basic Software

The basic software of the A350/A500 is distributed on four EPROMs in the ALU 150 (see item FW in Figure 99), which are accessible from the front after unscrewing the front plate (4 screws to be loosened, 2 of which are covered by the handles). The name plate with the version number of the basic software used is fixed to the lower handle of the module.



Caution When taken over completed A500 programs care must be taken that the distribution of the memory address space for the ALU 150 does not deviate from that valid for the ALU 821 diagram. Detailed data on this can be found in the user manual in the chapter "Adressing the Memory" resp. "Memory Allocation".

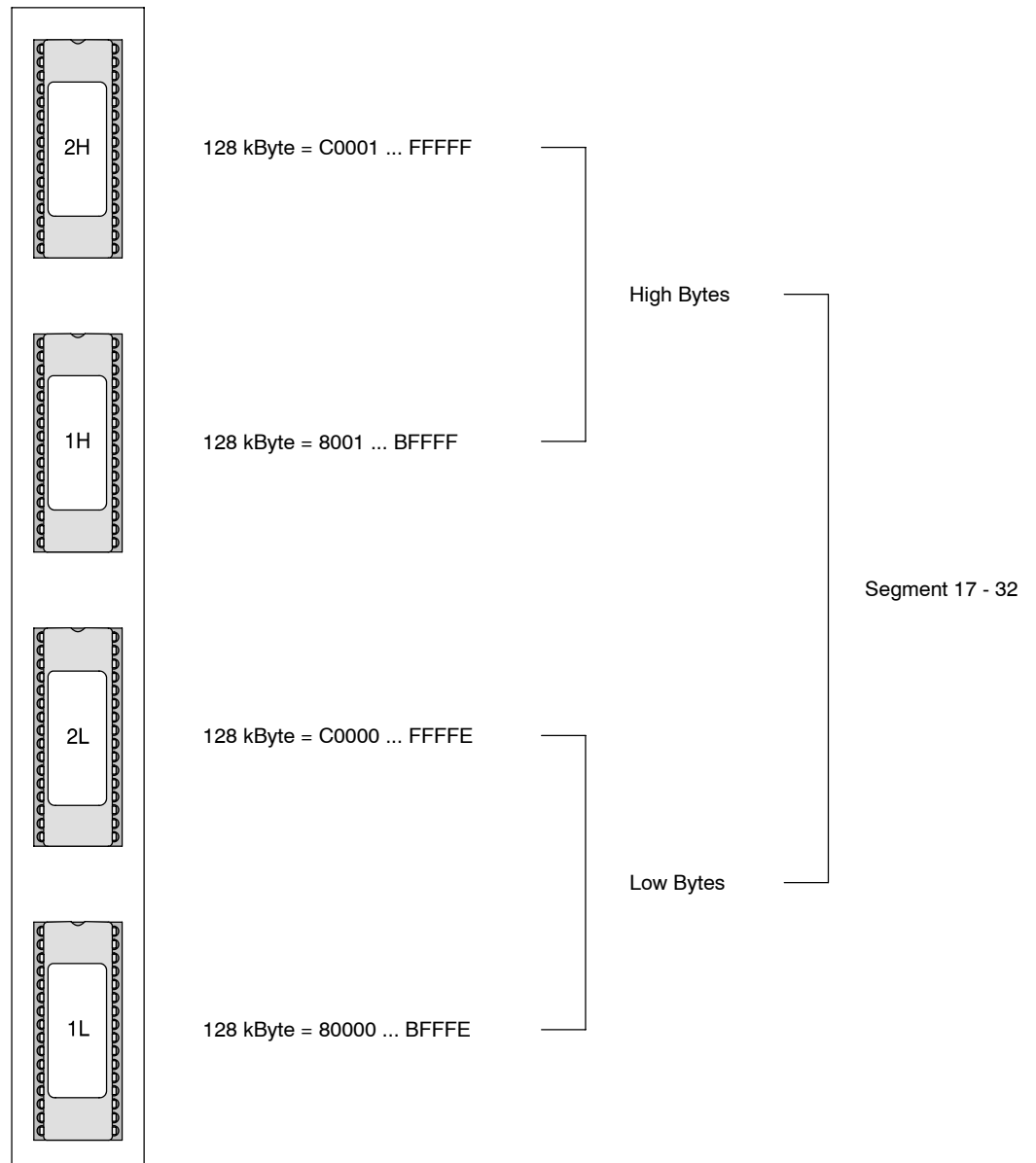


Figure 100 Arrangement of the EPROMs on the ALU 150 (Front View after Removing the Front Panel)

3.2 Baudrate

With the DIP switches 1-3 (pos. C in Figure 99) the baudrate is given, however, it is only then evaluated when the SCU 150 or UKA 024 is defective or if no baudrate is set. The switch coding is drawn from the following table.

Table 47 DIP-Switch Coding

Baudrate	DIP Switch			
	1	2	3	4
110	0	0	0	x
300	1	0	0	x
1 200	0	1	0	x
2 400	1	1	0	x
9 600	0	0	1	x
19 200	1	0	1	x

"0" = Switch Position OFF

"1" = Switch Position ON

"x" = Switch Position OFF,
Switch Position ON,

No other codings are permitted.



Warning When using front connection modules the switch position of the DIP switch 4 (x) must accord with the position of the DIP switch B1 on the SCU 150 or the jumper B1 on the UKA 024. Otherwise the function of the jumper B1 is not guaranteed.

3.3 Battery Charging Connection and Monitoring

The jumper BL is only necessary, when the ALU 150 is used in the A500. It enables a charging current which is designed for one 3-cell NiCd battery 1.8 Ah.

- When using the A350, the jumper "BL" has always to be open
- When using the A500, the jumper "BL" is necessary, if a NiCd battery integrated in the primary subrack is to be charged.

BL ○ ○ The battery charging current is interrupted.
 ○ ● The battery charging current is enabled. The battery integrated in the primary subrack of the A500 is charged.

A battery low voltage warning (when operating in the A350 battery low voltage warning) is distributed with valency 1 in the marker 23 and/or 33.

3.4 Starting Behavior of the Controller

With the aid of the jumper M, contact pin "set" and in combination with the UKA 024 or SCU 150 the starting behavior of the controller may be defined after a voltage failure. For more information on configuration see chapter "Startup Characteristics" in the user manual.

3.5 Documentation

An A3 form sheet with explanations is available for the system documentation, showing which type and E-No. is set for the software used as well as the operating conditions of jumpers and switches. These form sheets are:

- part of the form pad intended for conventional processing (see ordering details)
- part of the Ruplan processing database (under development) and intended for Ruplan processing (technical sales office version)

4 Specifications

4.1 Allocation	
Devices	A350, A500
Structure	Designated slot in the primary subrack (see module description of the subrack)
4.2 Supply Interface	
Internal	
UB 5	+5 V/1.4 A typical (2.5 A max)
UB 12	+12 V/0.1 A typical (0.15 A max)
UB -12	-12 V/10 mA typical (15 mA max)
Reference Potential	0 V
4.3 Data Interface	
PEAB	Parallel in-/output bus
PMB	Parallel microprocessor bus, driver design for max. 12 PMB subscribers
RS 232C / V.28	Serial interface according to DIN 66 020, non-isolated connection via SCU 150 on A350 or UKA 024 on A500
4.4 Processor Type	
8086	Microprocessor (16 bit) for logic and arithmetic
8087	Expansion of the module by adaptation of the additional board MAT 827 for processing numerical-mathematical problems

4.5 Memory Capacity

RAM	Signal RAM and system RAM, 32 Kbyte (16 x 16K / 1 bit, type 6167), of which 2 Kbytes can be addressed bit by bit,
EPROM	4 x 128K x 8 bit (INTEL 27C1000) = 512 Kbytes, occupied by system basic software (console functions, I/O routines, operating functions, Dolog B blocks etc.) can be fitted in parts in 2 x 128 Kbyte

4.6 Physical Characteristics

Module	Double European format
Format	6/8T
Mass (weight)	520 g

4.7 Type of Connection

PEAB, PMB	2 x plug-in connectors C64M according to DIN 41 612
-----------	---

4.8 Environmental Conditions

System Data	see chapter 4 in user manual A350 resp. A500
Stray Power Dissipation	≤8 Watt typical

4.9 Ordering Details

Module ALU 150	424 239 642 (with German basic software)
Module ALU 150 EN	424 239 667 (with English basic software)
Module MAT 827	424 203 633
A3 form pad A350	A91M.12-234 785
A3 form pad A500	A91M.12-234 720

Specifications subject to change without notice.

BATT

3.6 - 1.8 Ah Rechargeable Battery Module Description

Battery block which can be charged up to back up write/read memories (RAM) without any interruptions.

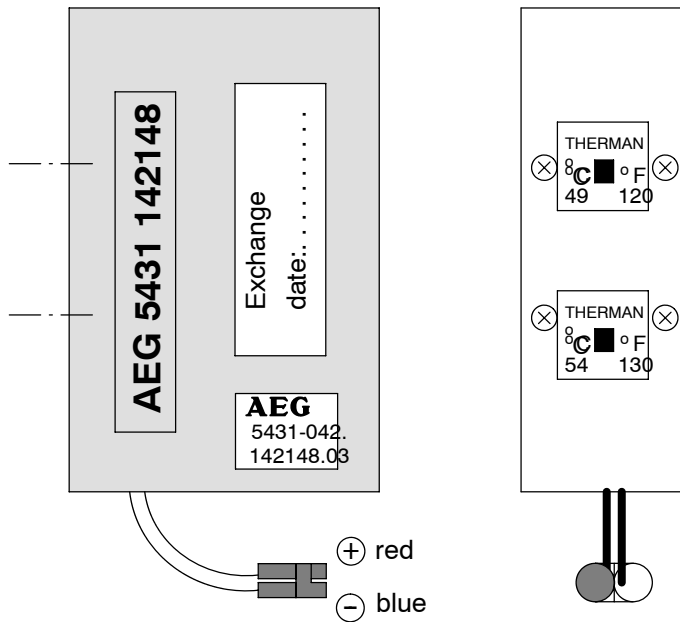


Figure 101 Front and Side Views of the NiCd Rechargeable Battery (BATT) with its Port

1 General

The module consists of a rechargeable battery which can be combined with the front panel of the 3HE/6T size to be fixed by insertion or on a mounting sheet for the rear of the subrack.

1.1 Physical Characteristics

The mounting of the front panel or mounting sheet is equipped with screw recessed heads for the possible battery change. The 2 pole port is protected against confusion.

1.2 Graphical Symbols

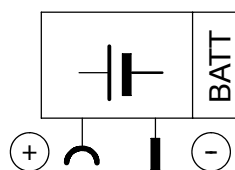


Figure 102 Graphical Symbols of the NiCd Rechargeable Battery (BATT)

2 Operation and Display

The module does not have any operating or indicating elements.

3 Configuration

Not necessary.

4 Specifications

4.1 Assignment

Product Family	Modicon
Devices	A500, CP550

4.2 Properties

Type	NiCd rechargeable battery
Capacity	3.6 V / 1.8 Ah

4.3 Operating Conditions

Duration of	at 20 °C	min. 5 years	(typically > 10 years)
Operation	at 50 °C	min. 2 years	(typically > 5 years)
Storage	(empty)		
	at -40°C ... +50°C	min. 5 years	(typically > 10 years)
Backup Duration with max. Capacity			
	at 0°C	min. 16 days	(typically 7.5 months)
	at 20°C	min. 13 days	(typically 2.8 months)
	at 40°C	min. 10 days	(typically 1.2 months)
Charging Duration for max. Capacity		6 days	
		after a Partial Discharge 1/4 ... 1/30 of the subsequent backup time	
Factory Delivery		empty	

4.4 Physical Characteristics

Format of the Rechargeable Battery Block	L x W x H = 81 x 53 x 28 mm
Front Panel	Size: 3 HE/6T
Port Type	2 pole, with C24-18 contact spring

4.5 Environmental Conditions

Operating Temperature	0 ... +50 °C, with information storage of the RAM
Storage Temperature	-40 ... +50 °C, without information storage of the RAM
Humidity	F category (according to DIN 40 040)
Weight	300 g

4.6 Ordering Data

BATT Rechargeable Battery Block

- | | |
|--------------------------------------|-------------|
| □ without the Front Panel | 424 142 148 |
| □ with the Front Panel
(DNQ 022*) | 424 142 152 |

Technical rights reserved!

*) previous designation

BIK 151

Modnet 1/SFB Interface for Central Processing Units

Module Description

The BIK 151 is the Modnet 1/SFB interface of the programmable controller for the remote input/output units.

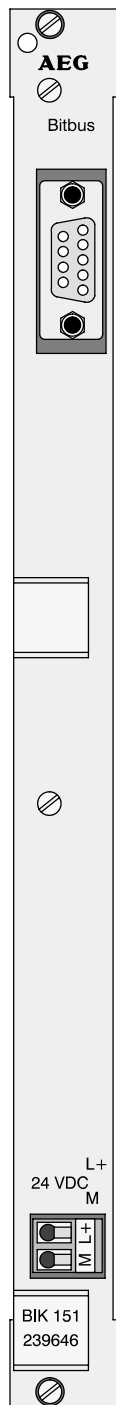
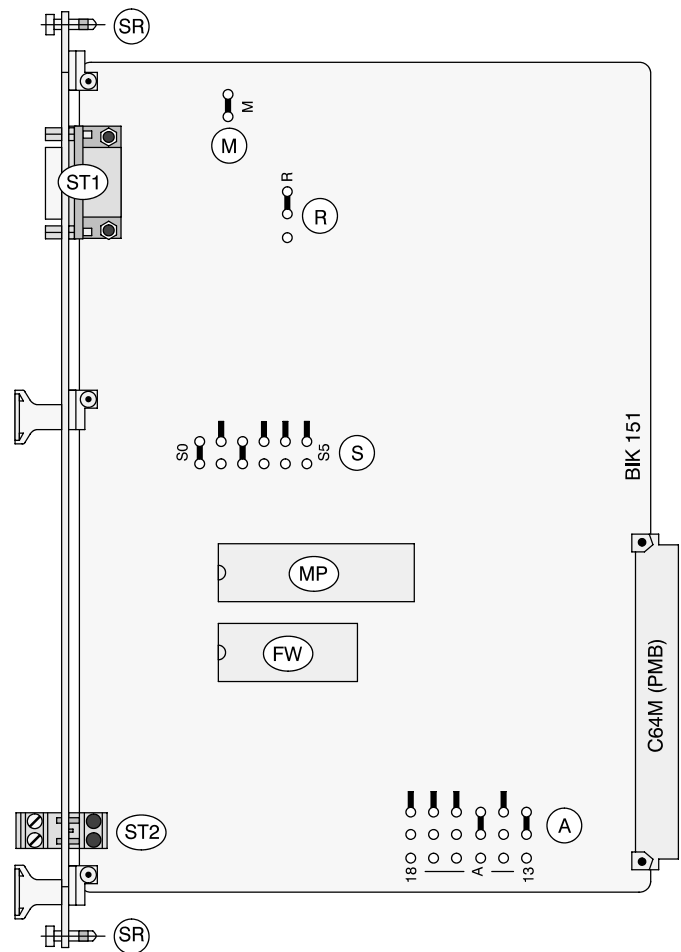


Figure 103 Front View of BIK 151



- (ST1) Modnet 1/SFB interface, Connection 9-pole
- (ST2) Front Connection for Supply Voltage, 24 VDC;
(always to be connected)
- (A) Address Setting (see 3.3)
- (FW) EPROM for Firmware
- (M) Jumper, Connection Cable Shield → Subrack, see 3.4
- (MP) Microprocessor
- (R) Switching Jumper Selfclocked/Synchron Mode
- (S) Baudrate Setting, Master/Slave S0-S2, see 3.1
(S3-S5 not for the user)
- (SR) Screw (always screw to the subrack)

Figure 104 Survey of Configuration Elements BIK 151

Note The jumpers shown correspond to the condition in which the system is supplied. All further not shown plug connectors are only for the test field settings in the factory, no adjustments may be made to these.

1 General

The BIK 151 is the Modnet 1/SFB interface of the programmable controller for the remote input/output units. In the sense of definition all I/O units which can be reached via the Modnet 1/SFB, are remote even if they are located in the common subrack or the same swing frame or control cabinet.

The module is an intelligent PMB node and is inserted in a PMB slot in the primary subrack of the A350 (DTA 150, DTA 151) or A500 (DTA 024, DTA 027.1, DTA 028, DTA 101, DTA 107) controllers.

A bus line with up to 28 networking nodes can be connected to the RS 485 interface, that is accessible from the front. Up to 16 of these nodes can be remote input/output units (DEA ...), regardless whether these are components of the compact or chassis mount layout. A suitable connecting cable between the BIK and DEA must be supplied by the user. For this RS 485 connector BBS 1 and bus cable JE-LiYCY (by the meter) are available separately.

1.1 Physical Characteristics

The module has double European format (front panel 4T) with reverse PMB contacting, front RS 485 connector and front auxiliary supply connection (see Figure 103 and Figure 104). The essential component parts are:

- Bitbus processor INTEL 8344 (RUP1)
- 16K networking RAM (dual port)
- EPROM with 16K firmware
- RS 485 interface for DEA and/or 1N procedures
- Plug jumpers for addressing, baudrate, screen connection, mode adjustment

1.2 Mode of Functioning

The module is used for transmitting and receiving data telegrams via the Modnet 1/SFB. It produces the data transfer between the central processing unit and the remote I/O units. It is fitted with its own microprocessor for this. With the inserted firmware the microprocessor and interface unit independently carry out the bitbus procedure. Input signals are filed in the networking RAM, the output signals are drawn from the networking RAM and transmitted to the remote I/O units.

The maximum transmission rate depends on the length of the bitbus cable and is

62.5	kbaud with a max.	1200 m	
375	kbaud with a max.	300 m	and
2	Mbaud with a max.	30 m	of lead.

In order to guarantee correct data transmission the cable length must not exceed 1200 m.

The bus signals on the front plug must be galvanically separated from the remaining logic via the optocoupler. A potential connection is possible via the jumpers.

2 Operation and Display

There are no display and operation elements available, however, some configuration elements must be taken into account for system startup (see chapter 3 "configuration").

3 Configuration

For the module the following are to be designed:

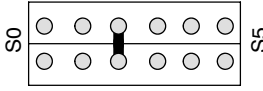
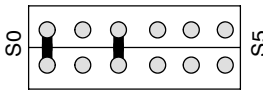
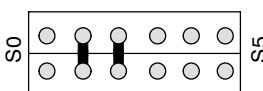
- ❑ Transmission rate, master/slave, transmission mode (c.f. 3.1)
- ❑ Address setting (c.f. 3.3)
- ❑ Interference suppression (c.f. 3.4)

3.1 Transmission Rate (S0, S1), Master/Slave (S2), Transmission Mode (R)

3.1.1 Transmission Rate, Transmission Mode

The transmission rate is set via the jumpers S0 and S1. Plugging in both jumpers at the same time is not permitted.



Table 48 Jumper Setting for Transmission Rate of BIK 151

Transmission Rate	Jumper Setting
62.5 kBit/s (kBd)	
375 kBit/s (kBd)	
2 MBit/ (MBd)	





Caution The jumpers S3, S4, S5 are not be used by the user.

The Modnet 1/SFB knows the two operating modes "selfclocked mode" and "synchronous mode". The operating mode depends on the choice of transmission rate and is set via the jumper R.

-  R synchronous mode, jumper setting with 2 Mbit/s (MBd)
-  R selfclocked mode, jumper setting with 62.5 and 375 kbit/s (kBd)

3.1.2 Master / Slave

The jumper S2 determines the function of the firmware on the serial interface:

- S2  Master; DEA and 1N logs are operated in DMP. In master status the jumper M must be plugged in (see 3.5).
- S2  Slave; in this case only the 1N log is processed. The jumper M may not be plugged in.

3.2 Entry in the EQU-List / COM-Table

BIK and KOS in the A350 and A500 are operated on the PMB slots in the primary sub-rack. Here the following maximum assignment is to be noted:

Table 49 Maximum assignment for PMB slots

A350	Number	A500	Number
BIK 151 for DEA logs	≤ 3	BIK 151 / BIK 821 for DEA logs	≤ 3
BIK 151 for 1N logs	≤ 3	BIK 151 for 1N logs	≤ 3
KOS 152	≤ 2	KOS 152 / KOS 882	≤ 7

The module transmits data telegrams both for I/O units (DEA logs) as well as for networking nodes (1N logs). In the Modnet 1N mode the BIK is entered in the communication table with the numbers shown below. It is then treated like a KOS. With mixed components (KOS and BIK) the first number should always be the first KOS. The following table contains the setting of BIK and KOS numbers with their corresponding PMB allocation (and entry in the equipment list or communication table).

Table 50 Determination of BIK and KOS Numbers for Respective PMB Allocation

Segment	ALU xxx	ALU 821	8k-Block	BIK 151 Entry in	:No.	Use
3	29	1			:BIK 0	
3	29	2		Com-Table ²³⁾	:KOS 2	Only 1N logs
3	29	3		EQU-List ²⁴⁾	:BIK 1	DEA and/or
3	29	4		Com-Table ²³⁾	:KOS 4	1N logs
4	30	1		EQU-List ²⁴⁾	:BIK 2	DEA and/or
4	30	2		Com-Table ²³⁾	:KOS 6	1N logs
4	30	3		EQU-List ²⁴⁾	:BIK 3	Only DEA logs
4	30	4				

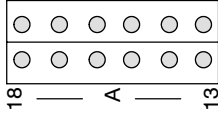


Note For the purpose of remote control/downloading a programming panel can only be connected to the busses of the BIK 1 and BIK 2 as remote device. Secondary sub-racks connected to the BIK 3 should be located as close as possible to the controller, because here remote control/downloading is not possible via a programming panel (connection on BIK 3).

²³⁾ Communication Table

²⁴⁾ Equipment List

3.3 Addressing



The module requires a memory space of 16 KB, which has to be reserved during configuration by means of jump settings on the RAM of the programmable controller (addressing). Here the segment is stated with the jumpers A14 ... A18 in which this memory space should be located whilst the jumper A13 defines whether in that segment the upper or lower half is reserved.

3.3.1 General Addressing

The following two tables give the general addressing of the module. Here an "1" signifies: jumper plugged in. Jumper settings for installation of the module in connection with ALU 0x1, ALU 150, ALU 286, and ALU 821 can be derived from these tables, but it is, however, treated separately again in section 3.3.2.

Table 51 Setting the Segment Address on BIK 151

Segment	32k block Address (hex)	A18	A17	A16	A15	A14
1	00000 - 07FFF	0	0	0	0	0
2	08000 - 0FFFF	0	0	0	0	1
3	10000 - 17FFF	0	0	0	1	0 ←
4	18000 - 1FFFF	0	0	0	1	1
5	20000 - 27FFF	0	0	1	0	0
6	28000 - 2FFFF	0	0	1	0	1
7	30000 - 37FFF	0	0	1	1	0
8	38000 - 3FFFF	0	0	1	1	1
9	40000 - 47FFF	0	1	0	0	0
10	48000 - 4FFFF	0	1	0	0	1
11	50000 - 57FFF	0	1	0	1	0
12	58000 - 5FFFF	0	1	0	1	1
13	60000 - 6FFFF	0	1	1	0	0
14	68000 - 6FFFF	0	1	1	0	1
15	70000 - 77FFF	0	1	1	1	0
16	78000 - 7FFFF	0	1	1	1	1
17	80000 - 87FFF	1	0	0	0	0
18	88000 - 8FFFF	1	0	0	0	1
19	90000 - 97FFF	1	0	0	1	0
20	98000 - 9FFFF	1	0	0	1	1
21	A0000 - A7FFF	1	0	1	0	0
22	A8000 - AFFFF	1	0	1	0	1
23	B0000 - B7FFF	1	0	1	1	0
24	B8000 - BFFFF	1	0	1	1	1
25	C0000 - C7FFF	1	1	0	0	0
26	C8000 - CFFFF	1	1	0	0	1
27	D0000 - D7FFF	1	1	0	1	0
28	D8000 - DFFFF	1	1	0	1	1
29	E0000 - E7FFF	1	1	1	0	0
30	E8000 - EFFFF	1	1	1	0	1
31	F0000 - F7FFF	1	1	1	1	0
32	F8000 - FFFFF	1	1	1	1	1

Table 52 Setting the Module address on BIK 151

16K block	Address (HEX)	A13
1	00000 - 03FFF	0
2	04000 - 07FFF	1 ←

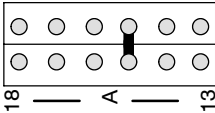
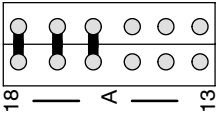
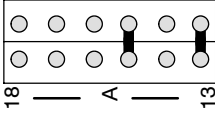
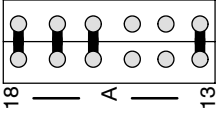
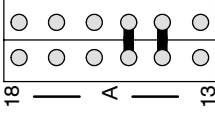
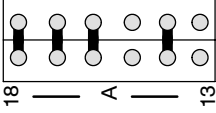
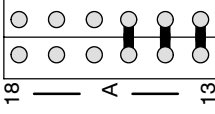
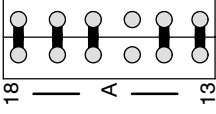
Addressing example:

For the BIK the second 16K block in segment 3 (address 14000 - 17FFF) should be reserved. A jumper between A15 and A13 is necessary (see arrows in Table 51 and in Table 52).

3.3.2 Addressing for Installation of BIK 151 in A350 / A500

When using the ALU 821 the BIK and KOS are addressed in the segments 29 and 30 of the memory area, in other cases only in the segments 3 and 4. The following table gives the coding of the address jumpers A18 - A13.

Table 53 Coding of the Address Jumpers A13 ... A18 for Installation of the BIK 151 in A350/A500

BIK No.	16 k block	Address for ALU 0x1, ALU 150 Segment Jumper setting	Address for ALU 821 Segment Jumper setting
0	1	3 	29 
1	2	3 	29 
2	1	4 	30 
3	2	4 	30 

3.4 Interference Measures (EMC), Jumper M

In order to avoid interference currents via the cable screen, RS 485 connectors and module handles are to be screwed firmly with the subrack. With "M" a galvanic connection between the plug casing and the front panel is produced. The position of the jumper M is determined by the jumper position of S2 (see 3.1.2).

3.5 Documentation

An A3 form sheet with explanations is available for the system documentation, showing which type and E-No. of the module's firmware is set used as well as the operating conditions of jumpers and switches. These form sheets are:

- ❑ part of the form pad and intended for conventional processing (see ordering details)
- ❑ part of the Ruplan processing database (under development) and intended for Ruplan processing (technical sales office version)

4 Specifications

4.1 Allocation

System	A350, A500
Structure	PMB area in the primary subrack, (see subrack description)

4.2 Supply Interface

Internal (PMB)	+5 V +4 %, -3 % 650 mA typical, max. 900 mA
External	+24 VDC peripheral voltage via the front plug 70 mA typical, max. 150 mA

4.3 Data Interface

PMB (internal)	Parallel microprocessor bus, see user instruction
Modnet 1/SFB Interface	Potential separation with optocoupler
Modnet 1/SFB	According to RS 485 (symmetric serial)
Assignment	see RS 485 connector description
Baudrate/Cable Length	62.5 kbaud at max. 1200 m 375 kbaud at max. 300 m 2 Mbaud at max. 30 m

4.4 Processor

Type	INTEL 8344 for bitbus
------	-----------------------

4.5 Memory

Program Memory (Firmware)	DSW 452/00 on EPROM type 27128 (16K)
---------------------------	--------------------------------------

4.6 Mechanical Structure

Module	Double European format
Format	Gr. 6/4T
Weight	290 g

4.7 Connection Mode

PMB	C64M
Modnet 1/SFB	9-pole socket for BBS 1

4.8 Environmental Conditions

System data	see user manual for A350, chapter 4
Power Dissipation	5 W typical

4.9 Ordering Details

Module BIK 151	424 239 646
RS 485 Connector BBS 1	424 233 854
Bus Cable JE-LiYCY (by the meter)	424 234 035
Modnet 1/SFB Standard	424 234 184
Cable YDL 40	
A3 Form Pad	A91M.12-234 785

Specifications subject to change without notice.

COP 82

Coprocessor

Module Description

The COP 82 module is operated as a coprocessor for ALU 150 and for ALU 821 in all primary subracks of the A500 and also as a passive PMB node on the active PMB with its own passive PMB. A multi processor system which considerably increases the processing capability of the ALU or of the entire system can thus be set up.

The module also has a directly accessible serial B.24 interface and a 32 kbyte or 64 kbyte memory (EPROM) for the basic software and a 32 kbyte memory (RAM) for the signal and program memory at its disposal.

Expanding the module with the insertable arithmetic option (MAT 827) is possible.

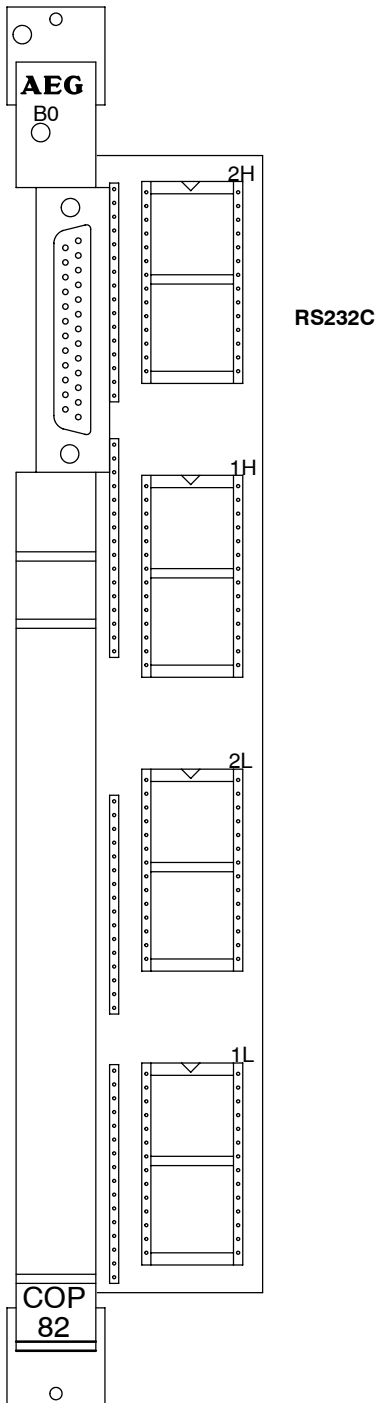
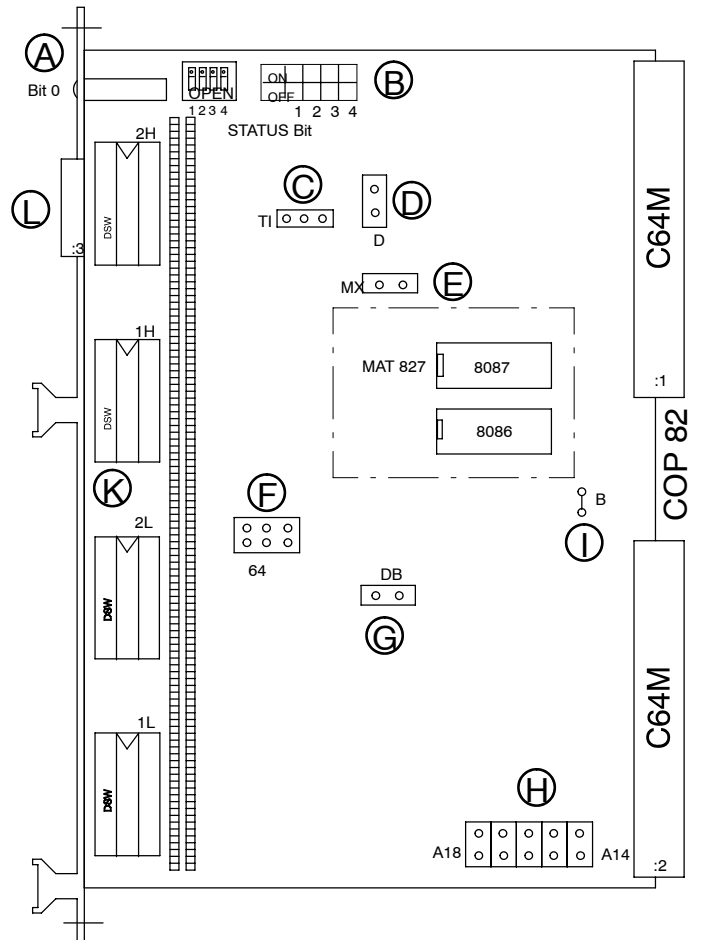


Figure 105 Front View of COP 82



- (A) B0 Contact Socket
- (B) Status Word of DIP Switch
- (C, D) V.24 Criteria
- (L) V.24 Interface
- (E) MAT 827 Use
- (F) EPROM Type
- (K) EPROM Slot
- (I) CMOS Supply Backup
- (G) Using the Bit Area
- (H) Address Area of the Dual Port Memory

Figure 106 Survey of the Configuration Elements for COP 82

1 General

1.1 Physical Characteristics

The module has the Europe double format with a construction width of 8T. The physical and electrical characteristics generally correspond to the ALU 150 or the ALU 821, expanded by the serial interface to connect periphery and a second (passive) memory bus directly. The PMB is divided physically into two parts for this purpose. These parts communicate with each other by means of a flexible printed circuit board via the dual port memory.

The front panel only has a width of 4T so that the equipment of the basic software can be detected and exchanged at the front. The label included with the relevant EPROM sentence is stuck onto the front panel and informed the operator of the type of the equipped software.

1.2 Mode of Functioning

The module is equipped with the 8086 processor type and is operated as a passive PMB node. The separate, passive PMB part communicates with the active PMB part via the dual port memory of the module. The mode of functioning is made clearer by Fig. Figure 107:

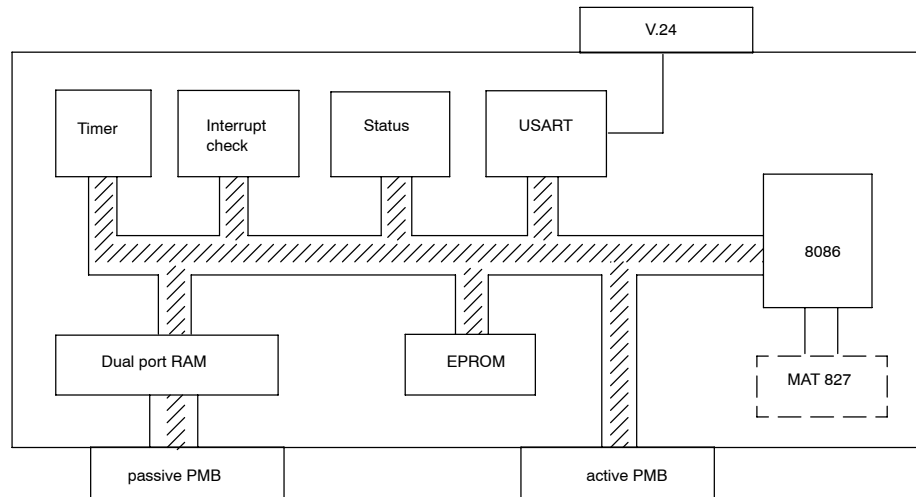


Figure 107 Block Diagram of COP 82

1.2.1 Memory Organization (RAM, Word Area):

The 32 kbyte RAM area is designed as a dual port memory (DPM), one side of which is connected to the PMB: COP 82 is therefore a passive PMB node, similar to a conventional 32 k RAM component. The two processors, (COP, ALU) communicate with each other via the DPM without affecting each other as far as the time is concerned (no wait states).

The other side of the dual port memory is connected to the internal microprocessor bus. This is guided to connector 1 as an “active PBM” via corresponding uncoupling and connected to the physically separate backplane via a flexible ribbon cable with a C64 connector. All types of PMB nodes such as, e.g., SC 8128, KOS 882, SF 8512, etc., can be connected here.

1.2.2 Memory-Organization (RAM, Bit Area):

2 kbyte of the RAM area can be addressed internally bit by bit. Each bit from this area can be addressed valently and anti-valently. 32 k addresses are thus assigned for the bit area.

2 Operating and Indicating Elements

B0 contact socket: Entering bit 0 of the status word; pin is plugged in = “1”.
The effect of status bits B0 ... B4 is to be defined in the application software.

25 pole connector: V.24 interface on the Cannon pin connector

EPROMs: These contain the basic software.

3 Configuration













The following is to be configured for the module:

- ☐ Type of basic software to be equipped, EPROM-type
- ☐ Transmission rate (status word)
- ☐ MAT 827 optional processor
- ☐ Using RAM bit area
- ☐ Data backup (CMOS-supply)
- ☐ PMB isolation point

3.1 Memory Capacity

The program memory is made up of 4 EPROM elements with a selective 2764/27128 type use through selective jumper “64”..

The EPROM area covers 4 x 8 kbytes or 4 x 16 kbytes. Disconnecting the “64” plug-in jumper switches off the internal EPROM area which can then be replaced by an external memory module.

- | | | | |
|--|--|--|--------------------|
| a)   | b)   | c)   | a) 2764 type |
|   |   |   | b) 27128 type |
| 64 | 64 | 64 | c) external memory |

3.2 Data Back-Up

The “B” layout jumper (I in Figure 106) connects the CMOS supply lines of MSBT (passive PMB) and CBT (active PMB of the COP 82). The “passive PMB” and the uncoupled “active PMB” are connected to a common backup battery for CMOS RAM with jumper “B”. If the “B” layout jumper is disconnected, a second backup battery can be connected to terminals a04 (+) and a01 (-) of the 64 pole PMB-connector for the “active PMB”. A regular replacement is to be ensured if a suitable dry battery is used. If a second rechargeable battery is used, a charging circuit is to be provided (ALU charges the 1st rechargeable battery only).

3.3 Address Area Setting


The address of the dual port memory are on the passive PMB is set with plug-in jumpers A18 ... A14 in accordance with the controller module.

Table 54 Setting the Address Area on the COP 82

A18	A17	A16	A15	A14	Segm.	Address area
○ ○	○ ○	○ ○	○ ○	○ ○	1	00 000 - 07 FFF
○ ○	○ ○	○ ○	○ ○	● ●	2	08 000 - 0F FFF
○ ○	○ ○	○ ○	● ●	○ ○	3	10 000 - 17 FFF
○ ○	○ ○	○ ○	● ●	● ●	4	18 000 - 1F FFF
○ ○	○ ○	● ●	○ ○	○ ○	5	20 000 - 27 FFF
○ ○	○ ○	● ●	○ ○	● ●	6	28 000 - 2F FFF
○ ○	○ ○	● ●	● ●	○ ○	7	30 000 - 37 FFF
○ ○	○ ○	● ●	● ●	● ●	8	38 000 - 3F FFF
○ ○	● ●	○ ○	○ ○	○ ○	9	40 000 - 47 FFF
○ ○	● ●	○ ○	○ ○	● ●	10	48 000 - 4F FFF
○ ○	● ●	○ ○	● ●	○ ○	11	50 000 - 57 FFF
○ ○	● ●	○ ○	● ●	● ●	12	58 000 - 5F FFF
○ ○	● ●	● ●	○ ○	○ ○	13	60 000 - 67 FFF
○ ○	● ●	● ●	○ ○	● ●	14	68 000 - 6F FFF
○ ○	● ●	● ●	● ●	○ ○	15	70 000 - 77 FFF
○ ○	● ●	● ●	● ●	● ●	16	78 000 - 7F FFF
● ●	○ ○	○ ○	○ ○	○ ○	17	80 000 - 87 FFF
● ●	○ ○	○ ○	○ ○	● ●	18	88 000 - 8F FFF
● ●	○ ○	○ ○	● ●	○ ○	19	90 000 - 97 FFF
● ●	○ ○	○ ○	● ●	● ●	20	98 000 - 9F FFF
● ●	○ ○	● ●	○ ○	○ ○	21	A0 000 - A7 FFF
● ●	○ ○	● ●	○ ○	● ●	22	A8 000 - AF FFF
● ●	○ ○	● ●	● ●	○ ○	23	B0 000 - B7 FFF
● ●	○ ○	● ●	● ●	● ●	24	B8 000 - BF FFF
● ●	● ●	○ ○	○ ○	○ ○	25	C0 000 - C7 FFF
● ●	● ●	○ ○	○ ○	● ●	26	C8 000 - CF FFF
● ●	● ●	○ ○	● ●	○ ○	27	D0 000 - D7 FFF
● ●	● ●	○ ○	● ●	● ●	28	D8 000 - DF FFF
● ●	● ●	● ●	○ ○	○ ○	29	E0 000 - E7 FFF
● ●	● ●	● ●	○ ○	● ●	30	E8 000 - EF FFF
● ●	● ●	● ●	● ●	○ ○	31	F0 000 - F7 FFF
● ●	● ●	● ●	● ●	● ●	32	F8 000 - FF FFF

3.4 Switching Off the Bit Area

One of the bit areas to be occupied and with an address capacity of k can be switched off by plugging in jumper OB (G), whereby this address capacity then becomes free.

OB  Bit area is switched off

3.5 Status Bits

The statuses are set via 5 switches which can be requested via reading commands. Switch 1 is a contact socket located in the front panel (bit 0). The remaining 4 (bits 1 ... 4) are designed as mini DIP switches. The function of the switches is determined by the relevant software.

3.6 Serial Interface

The interface is realized with the 8251 block and non-isolated with the corresponding interface. The maximum transmission rate amounts to 19 200 baud.


The T1, T4 clock signals can be used as well as the D1, D2, S2, M5 signals. These permit the interface to be clocked externally.

- The clock is switched over between internally and externally via the “TI” plug-in jumper.

TI  V.24 clock is clocked internally

TI  V.24 clock is clocked externally

- Plugging in the “D” jumper is permitted to control the D2 input with +12 V / 0 V instead of with +12 V / -12 V.

D  +12 V / -12 V

D  +12 V / 0V

3.7 Using an “Active PMB”

The “active PMB” outgoing via connector 1 is laid with a flexible printed circuit board in the level of the “passive PMB” of the ALU 150 or the ALU 821. The C64F connector of the flexible board is guided to connector 1 of the COP 82 and the C64M of the flexible board mounted on the right next to connector 2 of the COP 82 (pick-a-back by means of distance pins).

COP 82 now has 2 C64M plug connectors in the PMB-area, one of which belongs to the passive PMB and one of which belongs to the active PMB. The PMB must therefore be disconnected between the relevant socket connectors of the wiring circuit board in accordance with the 6054M-211194 modification instruction which cannot, however, be carried out by the user.



Caution The required slot of the COP 82, the isolating point in the backplane and therefore the number of slots for the “active PMB” is to be specified when ordering the subrack.

3.8 Documentation

DOIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of the circuit elements are already entered. These form sheets are

- ☐ included in the form block for conventional processing (see ordering data)
- ☐ included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

4 Specifications

4.1 Assignment

Product Family
Device
Structure

Modicon
A500
occupied PMB-slot (PMB operated by ALU 150 / 821), whereby the space in the area of connector 1 must be physically free for the "active PMB" (see section 3.7)

4.2 Data Interface

Passive PMB:

Connector 2 (C64M)
Inputs: MSA0 ... MSA18, MSBLEN, MSBHEN, MSMWN, MSMRN MSUSN, MSUSWN, MSRSTN, MSBT
Outputs: MPARN
bi-directional: MSD0 ... MSD15

Active PMB:

Connector 1 (C64M)
Inputs: CRDY, CPFN, CARN
Outputs: CA0 ... CA18, CBLN, CBHEN, CMWN, CMRN, CUSN, CUSWN, CRSTN, CBT, CLOWN, CIORN, CT2J, CAPN
bi-directional: CD0 . . . CD15

V.24

non-isolated, serial interface
Inputs: MPD2, MPM5, MPT4, MPE2
Outputs: MPD1, MPS2, MPT1
max. 19 200 bit/sec

Transmission Rate

4.3 Memory Capacity

RAM

32 kbytes, 2 kbytes = 16 kbits of which can be addressed valently / anti-valently (bit area)

EPROM (Front Panel)

depending on selective jumper "64" (see section 3.1)
32 kbytes, 2764 type or 64 kbytes, 27128 type

4.4 Processor type

8086
8087

Microprocessor (16 bits) for processor
MAT 827 optional board to process numerical and mathematical problems

4.5 Physical Characteristics		
Format		Double Europe format, size 6/8T
Weith		500 g
4.6 Type of Port		
PMB		2 x C64M connectors in the PMB area
V.24		25 pole Cannon front connector
4.7 Supply Interface		
U _B 5		typically + 5 V / 1.7 A (max. 2.5 A)
U _B 12		typically + 12 V / 0.1 A (max. 0.15 A)
Reference Potential		0 V
4.8 Environmental Conditions		
System Data		see A550 user manual
Power Dissipation		typically 8.8 watt
4.9 Ordering data		
COP 82 Module		424 200 650
Flexible Board		424 211 194
MAT 827		424 203 633
A3 Form Block		A91M.12-234 720

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DKV 023 PEAB Network Module Description

The DKV 023 is the driver side of the I/O bus extension of the controller via DKV 023 → MDL 67 → DKV 022 to the inputs/outputs. It permits the expansion to 1024 I/O points for each DKV 022 together with the DKV 022 (in secondary subracks), whereby up to 4 DKV 022 can be driven by the DKV 023. The prerequisite for the mentioned number of inputs/outputs is that I/O modules for 32 bits are used with a 4T slot width.

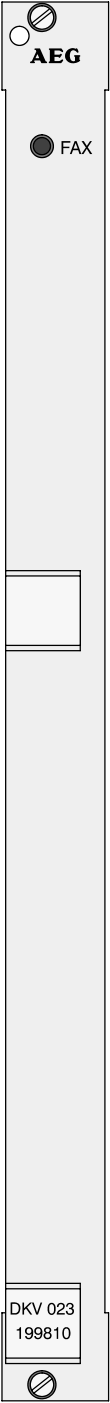


Figure 108 Front View of the DKV 023

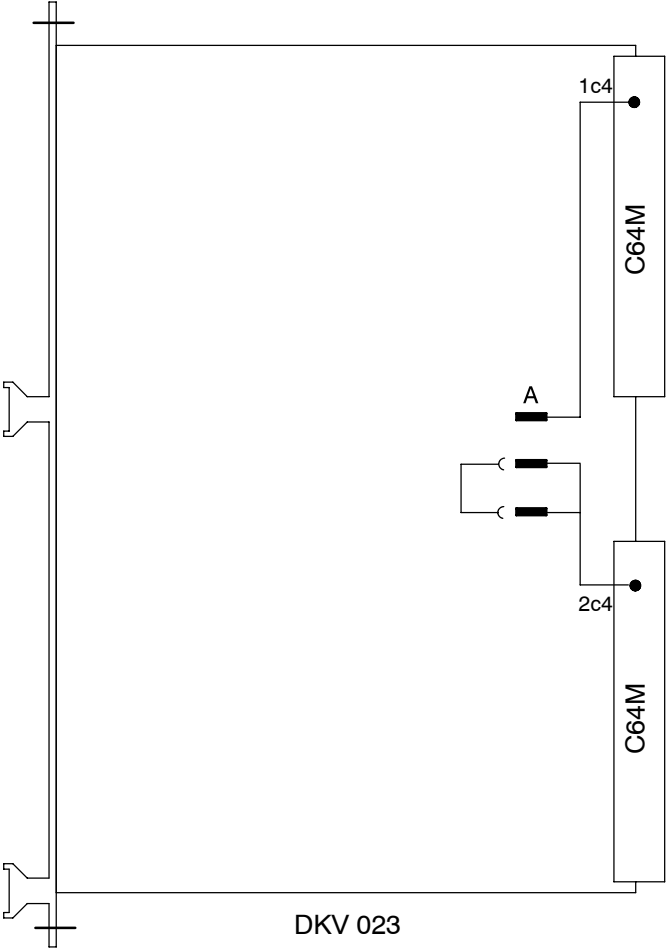


Figure 109 Survey of the Configuration Elements for DKV 023

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 4T. It is equipped with a contact socket (FAX) for the interrupt evaluation and a plug-in jumper to interrupt the WWSRN signal.

1.2 Mode of Functioning

The control signals are looped from subrack to subrack via a cable with a length of max. 20 m.

The slot reference occupied by the DKV 023 can still be used in a secondary subrack connected in parallel.

The undervoltage / access temperature signal (WWSRN) formed in the supply units must be guided by plugging in jumper A suitably so that

- the WWSRN signal is guided to all I/O modules but so that
- the WWSRN signals of different supply units do not operate in one and the same line either.

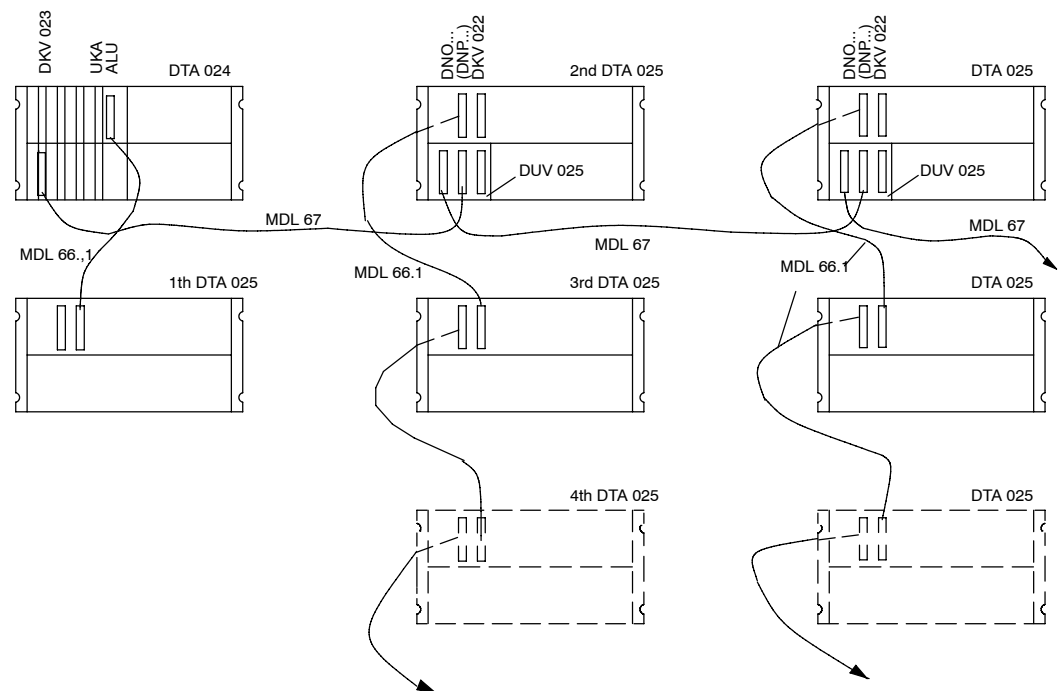


Figure 110 Using the DKV 023 with PEAB Extensions

2 Operation / Presentation

The module includes:

- ❑ The FAX contact socket on the front panel: Interrupt evaluation for test and start-up purposes.

Moreover, the module does not have any indicating and operating elements.

3 Configuration

The following is to be configured for the module:

- ❑ DKV 023 specification
- ❑ Structure
- ❑ I/O bus in DTA 025 (A3 forms)
- ❑ Physical coding of the slot, mounting measures

The following is to be configured for the central processing unit:

- ❑ Slot reference (EQL list entry)

3.1 Test and Start-Up

- ❑ **FAX:** Contact socket for interrupt evaluation
The interrupt memory of the entry modules (capable of interrupt) which are addressed via the DKV 023 are set with the contact pin plugged in and the interrupt cycle runs.
- ❑ **MDL 67:** The sum of all the part lengths may not exceed 20 m.

3.2 WWSRN Signal Guide

The WWSRN signal must be guided to all modules which are supplied by the same power supply. If secondary subracks have a separate supply, their WWSRN signal guide is to be separated from the controller. The following is useful here:

- ❑ Jumper A on the DKV 023 or
- ❑ the WWSRN jumpers on the rear of a DTA 025 even if the I/O extension has more than 1 power supply.

However, it should generally be separated so that no unnecessary cable lengths of the MDL 67 cause a “signal load” for the DKV 023.

Case 1:

The system has a common supply for the controller and inputs/outputs. The WWSRN signal flows to the I/O modules via jumper A and jumper 0713.

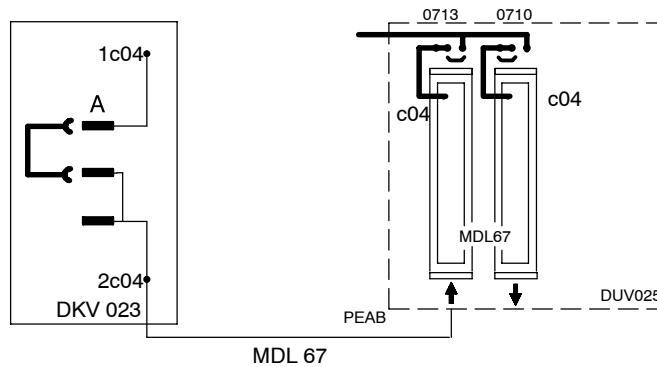


Figure 111 WWSRN Signal Guide

Case 2:

The inputs/outputs are equipped in the 2nd DTA 025 (see Figure 110). It possesses a separate power supply so that the WWSRN signal on the DKV 023 must be separate. Jumper 0713 must also be open and jumper 0710 closed. (The 1st DTA 025 addressed directly by the ALU via an MDL 66.1 without its own supply is not affected by this.)

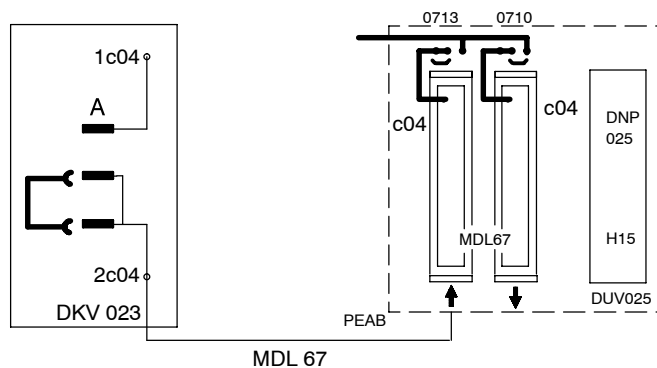


Figure 112 WWSRN Signal Guide

3.3 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of the circuit elements are already entered. These form sheets are

- ☐ included in the form block for conventional processing (see ordering data)
- ☐ included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	I/O bus in the DTA 024, DTA 025 (together with DTA 27.1), DTA 028 primary subracks

4.2 Supply Interface

U_{B12}/I_{B12} (PEAB)	+ 12 V / 50 mA
Reference Potential	0 V (2a32, 2c32)

4.3 Physical Characteristics

Block Format	Size: 6HE / 4 T
Type of Port	2 C64M connectors
Weight	260 g

4.4 Environmental Conditions

System data	see A500 user manual
Power dissipation	approx. 0.6 W

4.5 Ordering Data

DKV 023 Module	424 192 997
PEAB Cables	
MDL 67 (0.85 m)	424 200 969
(3.50 m)	424 207 133
(4.50 m)	424 207 134
A3 Form Block	A91M.12-234 720

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DNO 028

24 VDC Power Supply

Module Description

The DNO 028 is a DC power supply without isolation between the inputs and outputs. It generates the internal +5 V and ± 12 V supply voltages and the signals for the synchronization of several power supplies and for the undervoltage evaluation. It can only be used on slots of controller subracks reserved for it with H11M supply connectors.

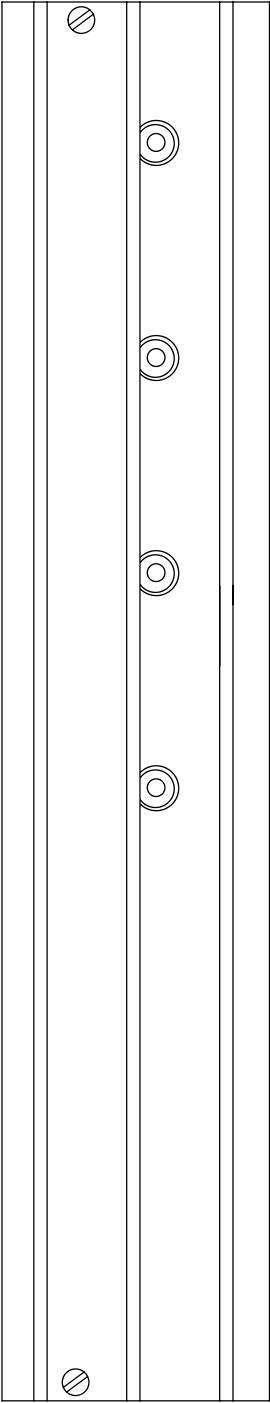
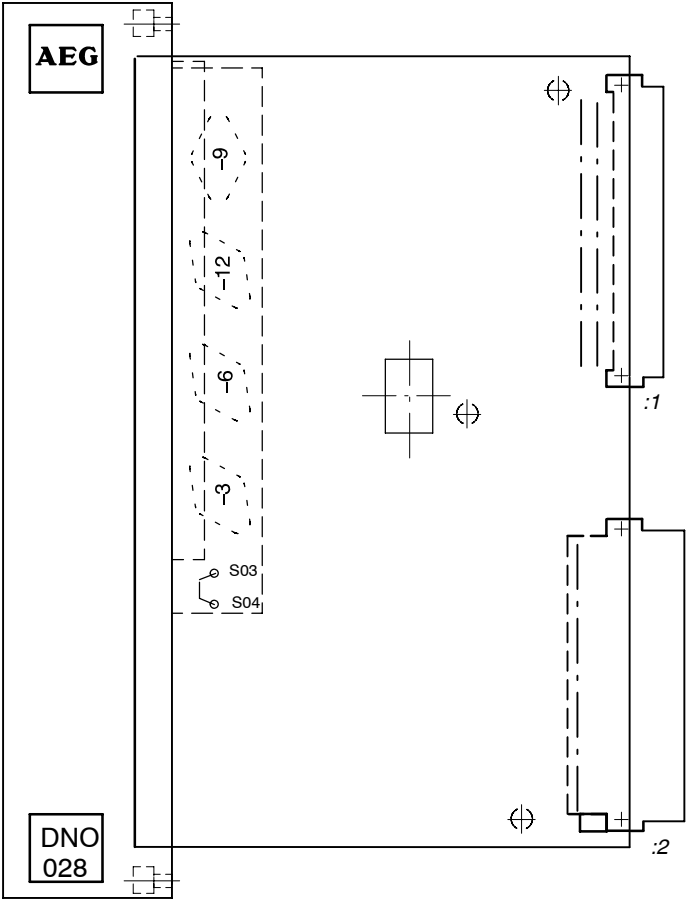


Figure 113 Front View of the DNO 028



S03, S04: Installation Position for Isolating Diode
Covered by the Shielding Sheet Metal

Figure 114 Survey of the Configuration Elements for DNO 028

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 8T, rear contacting of the inputs and outputs and a front heat zinc without operating elements.

1.2 Mode of Functioning

The generating secondary voltages are clocked and controlled and monitored electronically for voltage deviations and overload. Monitoring and enabling signals dependent on this permit the synchronous switching on and off of several power supplies of one system.

The DNO 028 operates without isolation between inputs and outputs; port M (M2) and secondary reference potential GND (0V) are separated by suppressor chokes and may therefore not be connected to each other.

Dependent Operation:

The wiring of several power supplies of one system is to be taken from Figure 117.

Synchronization

All the power supplies of one system are switched off for roughly 2 sec after a malfunction. They are then enabled again for approx. 100 ms. If the nominal values of all the output voltages are not obtained within this time, the power supplies are switched off again.

Parallel Connection

The parallel connection for the outputs of several power supplies is permitted.

FRGR: FRGM: FRGA:

Potential-free changeover contact to enable other power supplies. The relay picks up for approx. 100 ms when switched on (internally or externally) and closes the FRFM-FRGA contact. If not all the voltage nominal values are reached after this time or if a malfunction occurs after this time, the relay drops out again.

UEP: UEN:

Input separated via an optical coupler for monitoring other power supplies. This input must be connected to GND (preferably via FRGM-FRGA) so that the DNO 028 operates correctly. If GND is switched away, the warning cycle runs; i.e., the MPUSWN signal immediately becomes low while MPUSN and WWSRN become low after approx. 1 ms and the power supply is switched off.

2 Operating and Indicating Elements

The heat zinc serving as the front panel does not include any indicating or operating elements. See section Kap. 3 "Configuration", for physical alterations to extend the backup time.

3 Configuration

The following is to be configured:

- Wiring in the subrack (see 3.2)
- Optional capacitor for backup time extension, isolation by means of diode (see 3.3)
- Connecting several power supplies in one system

3.1 Graphical Symbols

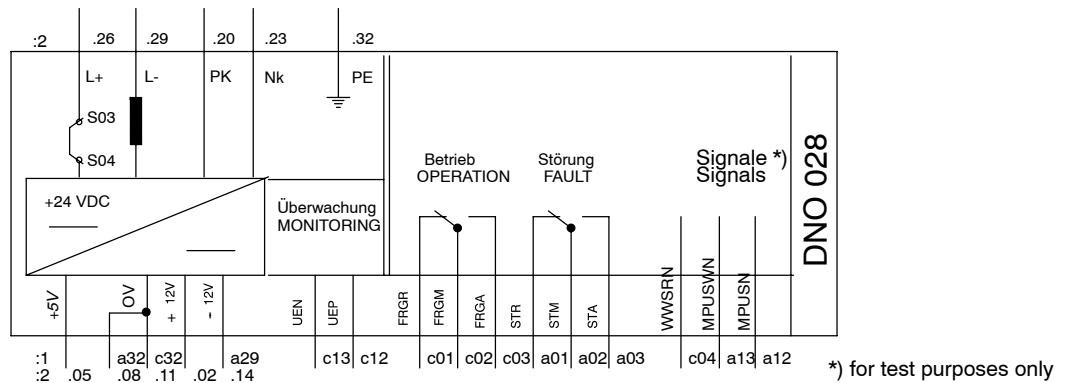


Figure 115 Graphical Symbols for DNO 028

3.2 Wiring in the Subrack

Single Power Supply:

The DTA 028 subrack already includes the following standard wiring for a single DNO 028 (Figure 116):

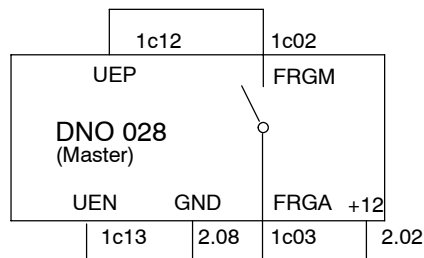


Figure 116 Standard Wiring of the DNO 028

Combination of Several Power Supplies:

The enabling wiring is to be altered or supplemented according to Figure 117 for systems with several power supplies.

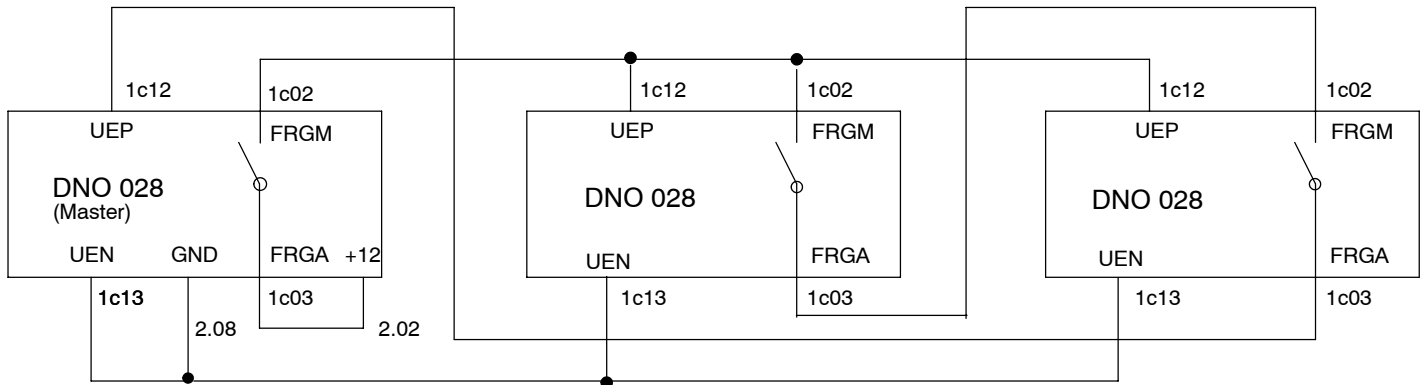


Figure 117 Expanded Wiring of DNO 028

3.3 Backup Time Extension

The standard backup time depends on the load and amounts to at least 150 μ s.

The slot in the DTA 028 subrack is wired with 2 x 4.7 mF for the use in A500 systems, so that the WWSRM signal results in a time of $t > 1$ ms (≥ 19 V with UB) for the data rescue with an undervoltage warning. The following is also valid for the backup time with external electrolytic capacitors for PK and NK:

$$U_e \geq 19V: C_{ext.} = 2.2 \text{ mF} / \text{ms} \text{ (Dielectric strength: 63 VDC)}$$

Disconnection:

If other actuators are also dependent on the source of the voltage supply and the backup capacitor could be discharged via these actuators, the S03 \leftrightarrow S04 jumper shown in Fig. 107 (it can be reached after removing the shield plate) is to be replaced by a diode which is to be adapted to the charging current of the power supply which is expected when the device is switched on the board of the DNO 028 module.

3.4 Connector Pin Assignment

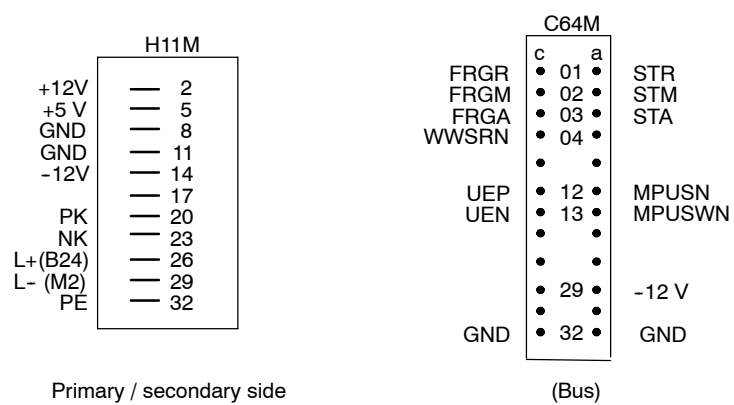


Figure 118 Connector Pin Assignment for DNO 028

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	Supply structure in the DTA 028

4.2 Supply Interface

Supply

U_e	+ 16.5 ... 24 ... 41 VDC
I_e max	< 4.5 ... 3 ... 1.8 A
L+ (U_{B24})	uncontrolled input
L- (M2)	Reference potential
PE	Protective earth

Outputs

U_{B5}	+ 5.05 V \pm 3% max 6 A
U_{B12}	+ 12 V \pm 3% max 2 A
U_{B-12}	- 12 V \pm 3% max 0.15 A
Reference Potential (GND)	0 V
Protection	
Against Overload	electronic current limit, switch-off
Against Overvoltage	Suppressor diodes for each output voltage
Fuses	non
Backup Time	> 150 μ s for powerfail and nominal load
Extension	external backup capacitor; see functions for values

4.3 Enable / Monitoring

Enable	
FRGR / FRGM / FRGA	Normally closed contact / root / normally open contact
Fault	
STR / STM / STA	Normally closed contact / root / normally open contact
Relay Loadability	\leq 60 V / 0.5 A / 10 W, 15 VA
UEP	Monitoring input (optical coupler)
	+5 ... 12V (8 ... 26 mA) for "good" area
UEN	Reference potential for UEP

4.4 Physical Characteristics

Format	Size: 6/8 T
Type of Port	
Bus	C64M connector
Mains, Backup Capacitor	H11M: PK (+, terminal 20), NK (-, terminal 23)
Weight	1.5 kg

4.5 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	< 65 W, typically 20 W

4.6 Ordering Data

DNO 028 Module	424 199 850
A3 Form Block	A91V.12-234 721

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DNP 023

220 VAC Power Supply

Module Description

The DNP 023 is an AC power supply with isolation between the inputs and outputs. It generates the internal +5 V and ± 12 V supply voltages and the signals for the synchronization of several power supplies and for the undervoltage evaluation. It can only be used on slots of controller subracks reserved for it with H15M supply connectors.

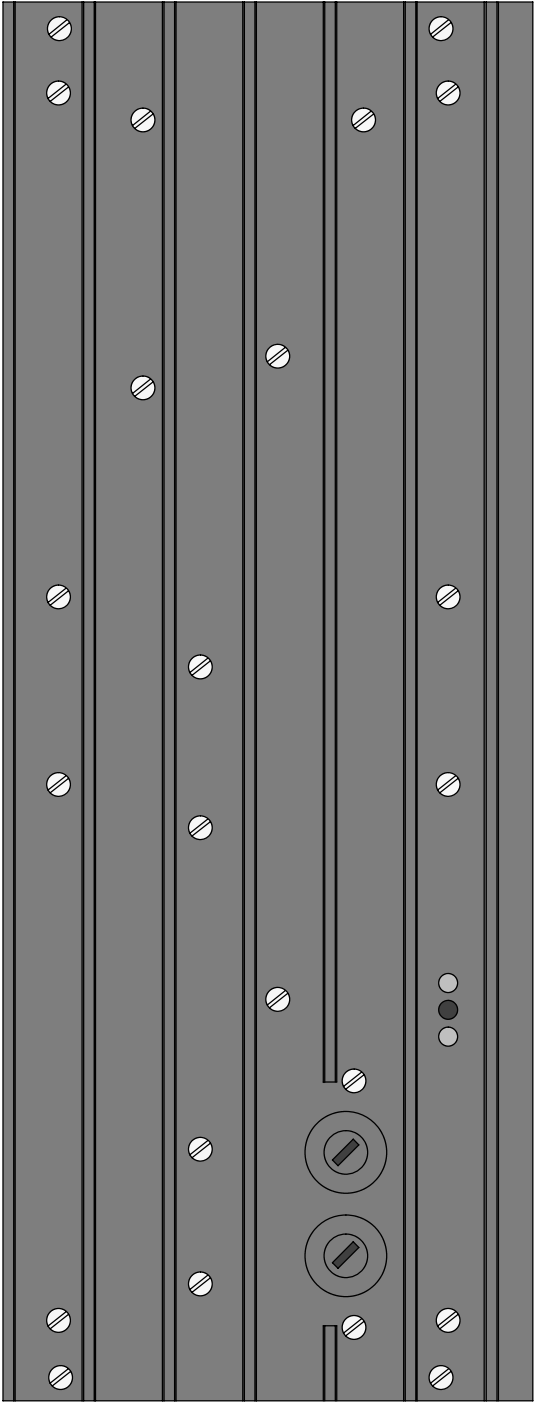


Figure 119 Front View of the DNP 023

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 20T, rear contacting of the inputs and outputs and a front heat zinc with fuses and operation indicator.

1.2 Mode of Functioning

The generated secondary voltages are clocked and controlled and monitored electronically for voltage deviations and overload. Monitoring and enabling signals dependent on this permit the synchronous switching in and off of several power supplies of one system.

SYNCHN:

SYNCHN is a non-isolated input to monitor other power supplies. This input must be connected to GND (0 V) (preferably via FRGM-FRGA) so that the generating secondary voltages are enabled (see Figure 120). If the input is open or if the signal is 1, the warning cycle runs, i.e., MPUSWN immediately becomes LOW while MPUSN and WWSRN become LOW after approx. 1 msec and the power supply is switched off.

FRGM (PSEC), FRGA (PSENO):

The potential-free normally open contact serves to enable other power supplies. When the primary voltage is switched on, the relay picks up for approx. 100 msec and closes the FRGM - FRGA contact. If not all the voltage nominal values are reached after this time or if a fault occurs after this time, the relay immediately drops out again.

Synchronization

All the power supplies of one system are switched off for roughly 2 sec after a fault (red LED). They are then enabled again for approx. 100 msec. If the output voltages of all the power supplies do not reach their nominal values within this time, the power supplies are switched off again.

2 Operating and Indicating Elements

The heat zinc serving as a front panel includes the two primary fuses and 3 light emitting diodes for the operating state indicator.

- LED 1 ready for service, green (top)
- 2 fault, red
- 3 mains voltage is present, green

3 Configuration

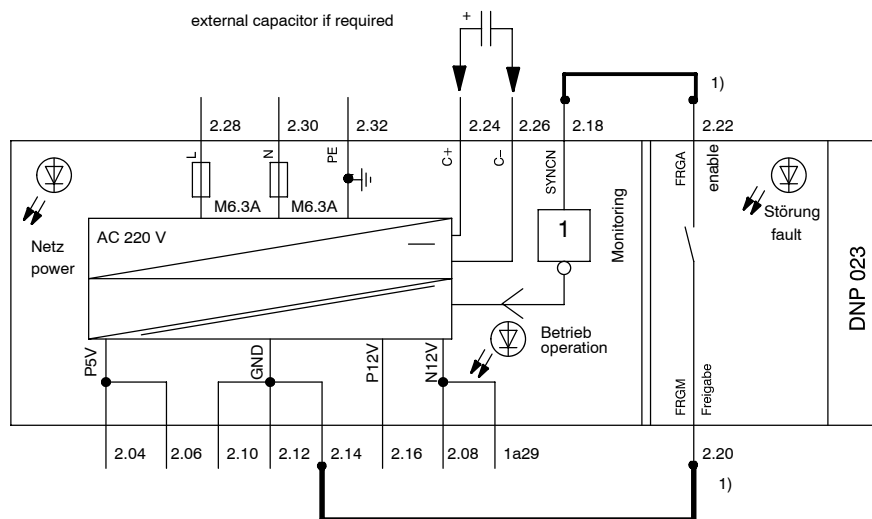
The following is to be configured:

- ❑ Wiring in the subrack
- ❑ Coding the slot
- ❑ Backup time extension (if required)

3.1 Settings/Protective Circuits/Indicators

There are no modifications possible on the module whatsoever.

3.2 Graphical Symbols



Wiring the enable for controllers with a single power supply

Figure 120 Graphical Symbols for DNP 023

3.3 Wiring in the Subrack

The DTA 024 and DTA 027 subracks are supplied with or without enable wiring for a single 220 VAC power supply depending on the revision index (DTA 27.1 and DTA 107 are always supplied without enable wiring for a single 220 VAC power supply). The function of any inserted power supply is blocked in order to avoid startups with unsuitable wiring without this wiring of the enable loops! See Figure 120 and Figure 121 for the necessary wiring for systems with one or more power supplies.



Caution Note the existing wiring or enable wiring which is still present in the subrack for use in the DTA 024 or DTA 027.

Enable Wiring

for the dependent operation of several power supplies for one system

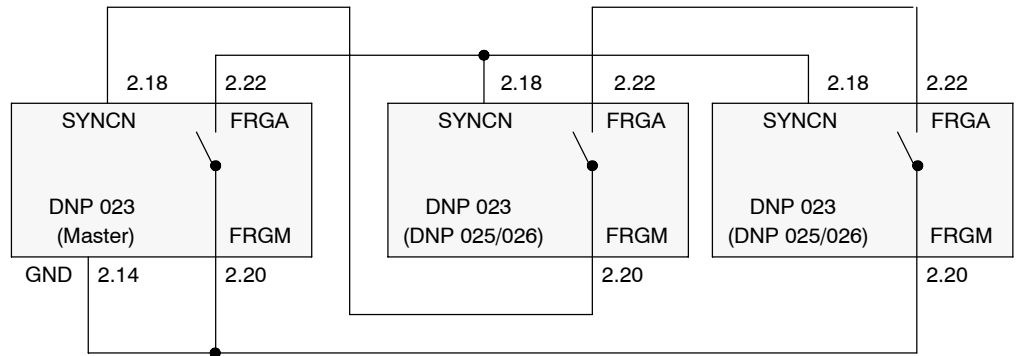


Figure 121 Enable wiring for DNP 023

Doubling the Enable Contact

for an event

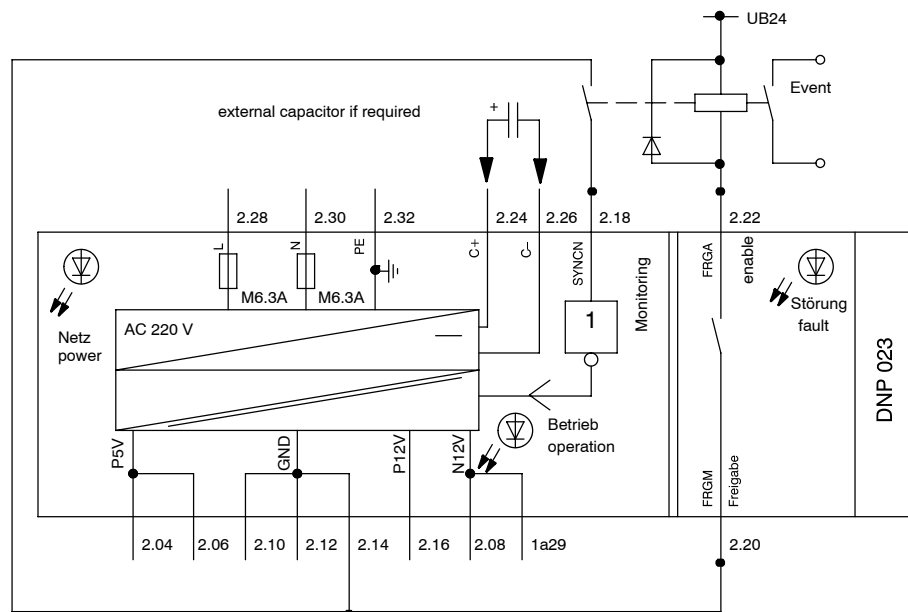


Figure 122 Doubling the Enable Contact for the DNP 023

3.4 Slot Coding

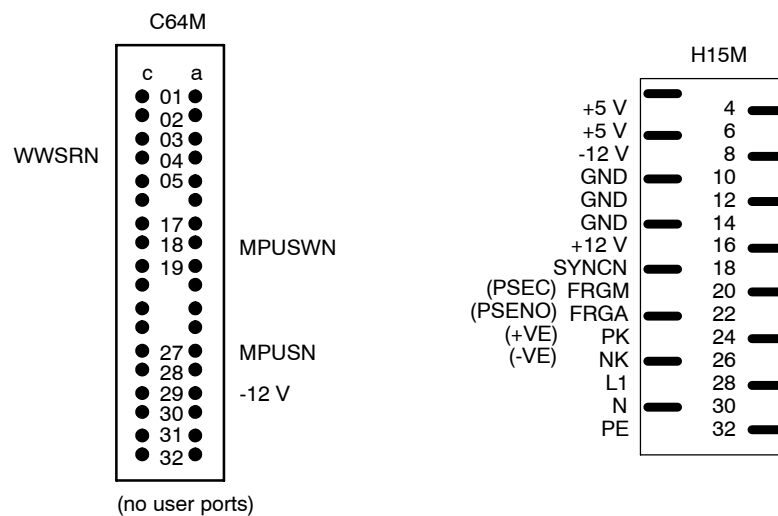
The slot in the subrack provided by the configuration is to be coded as the slot of a 220 VDC component by inserting two coding screws (x, see Figure 119).

3.5 Backup Time Extension

If the standard backup time (see Specifications) is to be extended, an optional capacitor of 0.37 mF / 10 ms is to be connected to terminal 24 (+) and terminal 26 (-).

Maximum values: 3.3 mF (450 VDC) without series resistor R
15 mF (450 VDC) with R = 0.47 ohms / 12 W

3.6 Connector Pin Assignment



(...) Signal names for devices labelled in English

Figure 123 Assignment of the Connectors (Looking at the Rear of the Subrack)

3.7 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- ☐ included in the form block for conventional processing (see ordering data)
- ☐ included in the A500 Ruplan data bank für Ruplan processing (Technical Sales office version, in preparation).

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	Supply structure in the DTA 024, DTA 027, DTA 27.1 subracks

4.2 Supply Interface

Input

U_e	220 VAC + 10%, - 15%, 48 ... 62 Hz
I_e	max. 2 A
L	Mains input. phase (terminal 2.28)
N	Mains input, MP (terminal 2.30)
Fuse	2 x M 6.3 E
Reference Potential	MP
Protective Earth	PE

Outputs

$U_{B\ 5}$	+5.05 V $\pm 3\%$ max. 20 A (terminals 2.04, 2.08)
$U_{B\ 12}$	+12 V $\pm 3\%$ max. 8 A (terminals 2.16)
$U_{B\ -12}$	-12 V $\pm 5\%$ max. 0.5 A (terminals 2.08, 1a29)
Reference Potential (GND)	0 V (terminals 2.10, 2.12, 2.14)
Load Protection	
□ against Overload	Switch-off
□ against Overvoltage	Suppressor diode
Memory Time with Powerfail and Nominal Load	18 msec (>1 half-wave)
external Capacitor	PK (+VE) (terminal 2.24), NK(-VE) ≤ 15 mF (terminal 2.26)

4.3 Enable/Monitoring

PSEC/PSENO (FRGM/FRGA)	Enable, potential-free normally open contact (terminals 2.20 - 2.22)
SYNCR	Monitoring input, (terminal 2.18) non-isolated, negated

4.4 Physical Characteristics

Format	Double Europe format, size: 6/20T
Port	H15M + C64M connectors
Weight	4.1 kg

4.5 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	< 50 W with nominal load

4.6 Ordering Data

DNP 023 Module	424 199 810
A3 Form Block	A91M.12-234 721

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DNP 023-1, DNP 023-2 Power Supply Module Description

The DNP 023-1 and the DNP 023-2 are power supplies for a 24 VDC or 48 VDC primary voltage and offer 3 isolated secondary voltages of +5 V, +12 V and -12 V.

They are suited to be used in the DTA 024, DTA 027 and DTA 27.1 controller subracks with the H15M supply connector.

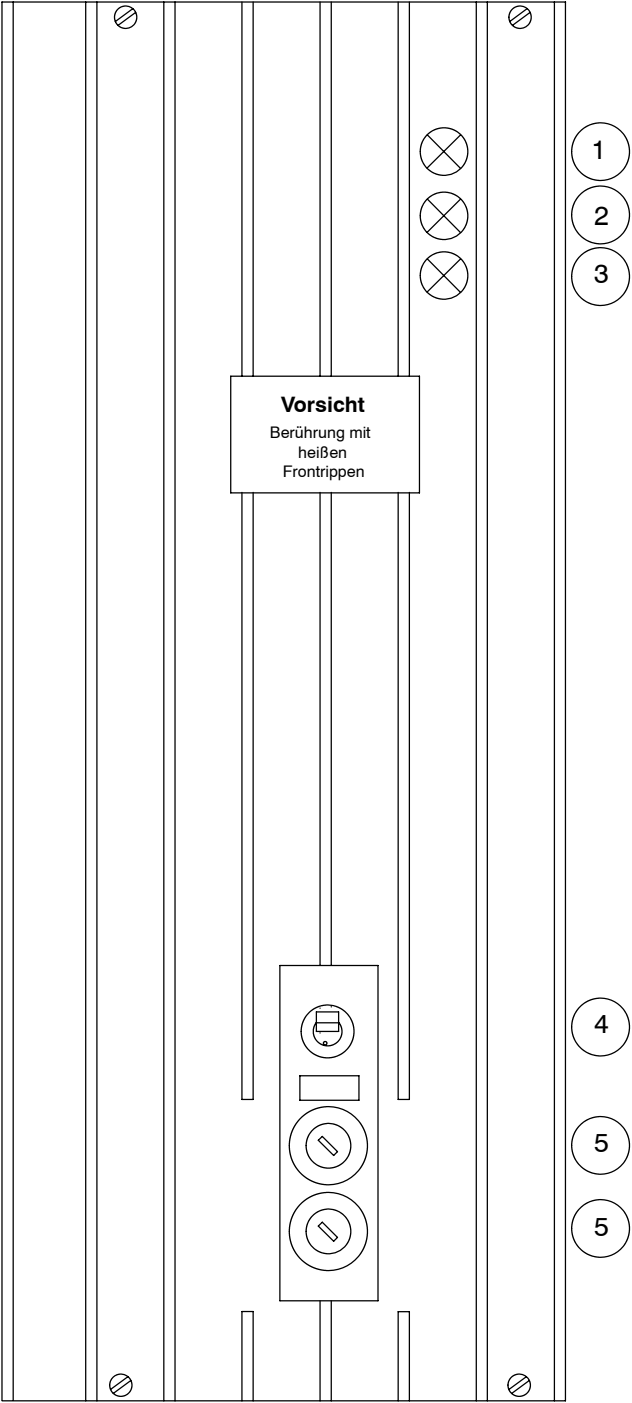
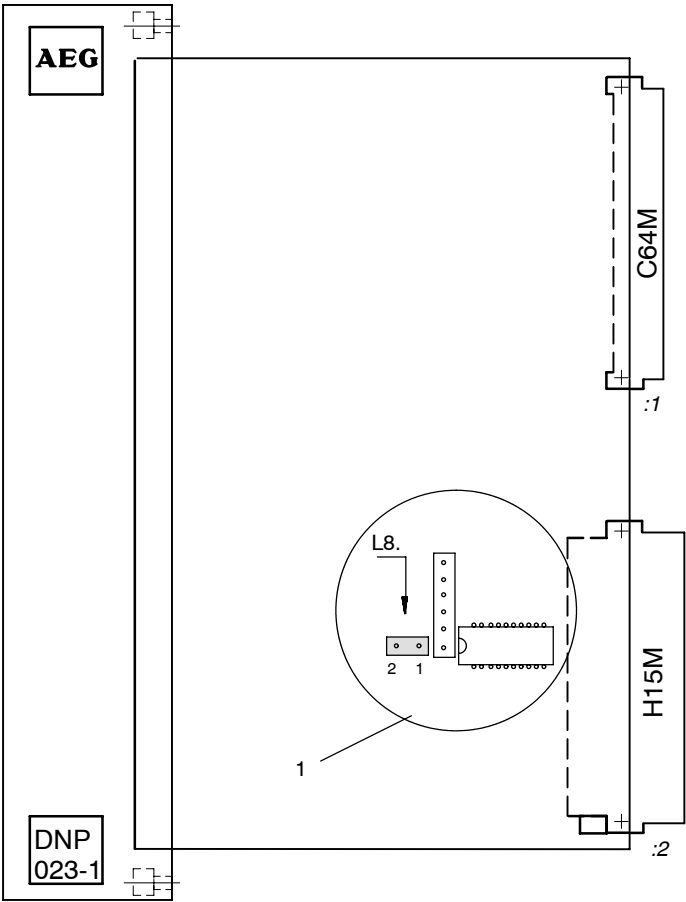


Figure 124 Front View of the DNP 023-1, -2



1) This figure detail represents a section of the upper printed board the equipment of which projects into the inside of the device (accessible after loosening this printed board). The interpolation points of the backup time are jumper are located here (L8.1 - L8.2) (see backup time extension).

Figure 125 Survey of the Configuration Elements for DNP 023-1

1 General

1.1 Application

The DNP 023-1 ($U_e = 24$ VDC) and DNP 023-2 ($U_e = 48$ VDC) modules are DC power supplies with isolation between inputs and outputs. They generate the +5 V and ± 12 V internal supply voltages and signals for the synchronization of several power supplies and for the undervoltage evaluation. They can only be used on slots of primary sub-racks reserved for them with a H15M supply connector.

1.2 Physical Characteristics

The module has a double Europe format with a construction width of 20T, rear contacting of the inputs and outputs and a front heat zinc with a power switch, fuses and operating indicators.

1.3 Mode of Functioning

The device types can only be distinguished in the supply voltage. The generated secondary voltages are clocked and controlled and monitored electronically for voltage deviations and overload. Monitoring and enable signals depending on this permit several power supplies of one system to be switched on and off in synchronization. Power interruptions of up to 0.3 sec can be bridged by the additional capacity.

SYNCHN:

SYNCHN is a non-isolated input to monitor other power supplies which connect this input to GND (0V) (preferably via FRGM-FRGA) if the device is functioning perfectly; the input is to be wired with GND for solo operation so that the power supply operates correctly (see standard protective circuit). If the input is open or the signal is 1, the warning cycle runs, i.e., MPUSWN immediately becomes LOW while MPUSN and WWSRN become LOW after approx. 1 msec and the power supply is switched off.

FRGM (PSEC), FRGA (PSENO):

The potential-free normally open contact serves to enable other power supplies. The relay picks up for approx. 100 msec when the primary voltage is switched on and closes the FRGM-FRGA contact. If not all the voltage nominal values are reached after this time or if a fault occurs after this time, the relay immediately drops out again. The wiring of the warning signal can be designed with the connector of the add. pack. for systems with 1 power supply only.

Synchronisation

All the power supplies of a system are switched off for roughly 2 sec after a fault. They are then enabled again for 100 msec. If the output voltages of all the power supplies do not reach their nominal values during this time, the power supplies are switched off again.

2 Operating and Indicating Elements

The hot zinc designed as the front panel includes the power switch, the two primary fuses and 3 light-emitting diodes for the operating state indicator:

- (1) LED 1 (top) Operation, green
- (2) LED 2 Fault, red
- (3) LED 3 Supply is present, green
- (4) Power switch
- (5) Fuse

3 Configuration

The following is to be configured:

- ☐ Wiring in the subrack
- ☐ Optional capacitor if required as a backup time extension
- ☐ Voltage control for +5 V
- ☐ Time range switch-over

3.1 Settings/Protective Circuits/Indicators

There are no interventions necessary for the module whatsoever except for switching over the backup time (see section 3.4 and Figure 128).

3.2 Graphical Symbols

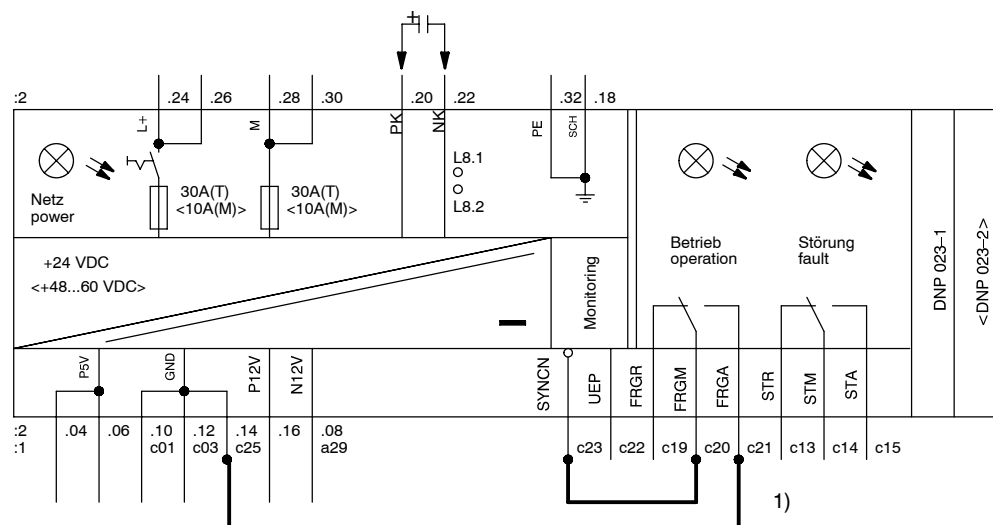


Figure 126 Graphical Symbols for DNP 023-1, -2

Re Figure 126 :

Graphical symbol entries in < > are valid for DNP 023-2.

The enable wiring is to be extended in accordance with Figure 127 for systems with several power supplies.

3.3 Wiring in the Subracks



Warning A wiring which is not adapted to the selected power supply can cause the module to be destroyed.

The DTA 024 and DTA 027 subracks are supplied with or without the standard wiring for a single 230 VAC power supply depending on the revision index (enable loop). The function of any inserted power supply is blocked without the wiring of the enable loop! See Figure 126 and Figure 127 for the necessary wiring for systems with one or more power supplies.

Table 55 Wiring Differences with DC and AC Power Supplies

Supply or Signals	DTA 024, DTA 027 with DNP 023, 230 VAC, Column 1			DTA 024, DTA 027 with DNP 023-1 ... -4, 24 / 48 VDC, Column 2		
Power	L	2.28		L+	2.24,	2.26
Power	N	2.30		L-	2.28,	2.30
PK (+VE)		2.24			2.20	
NK (-VE)		2.26			2.22	
FRGM (PSEC)		2.20				1c20
FRGA (PSENO)		2.22				1c21
SYNCH		2.18				1c23
GND		2.14				1c25
GND		2.12		2.14		
GND		2.10		2.12		
				2.10		

1) Standard wiring for DNP 023: Removes this at all costs when using DNP 023-1 ... -4

2) Connectors and labels for the rear of DTA 024/027 can be ordered separately as an add.pack.

() Signal names in () are valid for modules labelled in English



Warning The wiring according to Table 55, column 2, required for a single DNP 023-x is to be compared with the standard wiring of the used subrack and to be altered, if necessary, for the use in the DTA 024 or DTA 027.

Enable wiring

for the dependent operation of several power supplies for one system

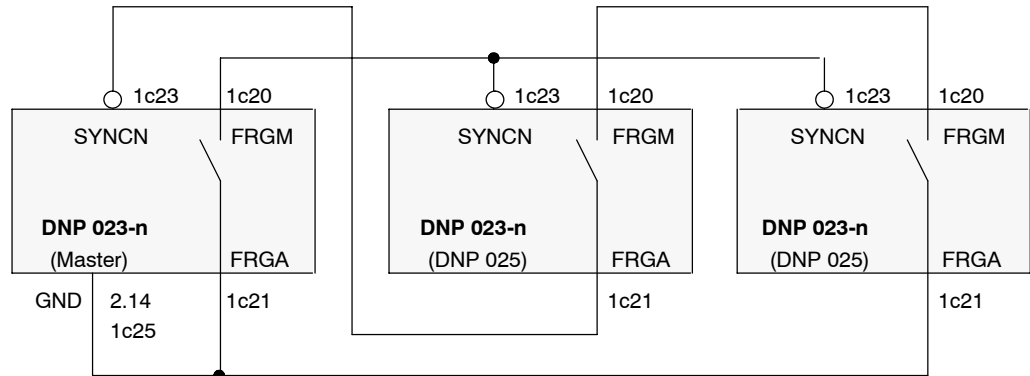


Figure 127 Enable Wiring for the DNP 023-1, -2

3.4 Parallel Power Supply Outputs

Parallelling is only permitted for +5 V and +12 V and under the following prerequisites:

- ❑ Nominal output load for each power supply is limited to **< 130 W**
- ❑ with standard memory time:
wired with optional capacitor of **$C_{\text{ext}} = 220 \mu\text{F} / 160 \text{ V}$**
- ❑ with memory time extension:
wired with **125 %** of the calculated C_{ext} for the desired time extension

3.5 Voltage Control for +5 V

If interference voltage drop-outs occur for the connectors of the supply wiring in the subrack due to a high current load or a load change, a settling of the fluctuations can be carried out to 5.05 V if necessary with a voltage feedback from the critical 5 V supply point to the input of +5H (1a14) of the power supply.

+5H is not wired: $U_{B5} = 5.15 \text{ V}$

This feedback is already taken into account in standard subracks.

3.6 Backup Time Extension

If the standard backup time (2 msec) is to be extended, an optional capacitor is to be connected to terminal 20 (+) and terminal 22 (-) of the supply connector:

You can select between 2 time ranges with the L8.1 - 2 jumper (this can only be reached after opening the shield chassis). The time range begins at 2 msec with the device in the delivery state. The position of the range jumper of L8.1 - 2 can be seen from Figure 125.

The time ranges and the calculation formula for the size of the backup capacitor are to be taken from Figure 128.

Optional Capacitor C_{ext}

Memory time (SPZ)	Capacity (C _{ext})	Jumper L8.1 - 2
2 ... 138 msec	0 ... 50 mF	o—o *)
83 ... 300 msec	14 ... 50 mF	-o o-

*) As delivered from the factory

The following is valid for the calculation of the capacitor

$$C_{ext} \text{ (mF)} = \frac{SPZ \text{ [ms]} - 2}{2.6 \text{ *)}}$$

SPZ [ms] - 2

SPZ = Memory time in msec

*) 5.6 with the jumper open

Port

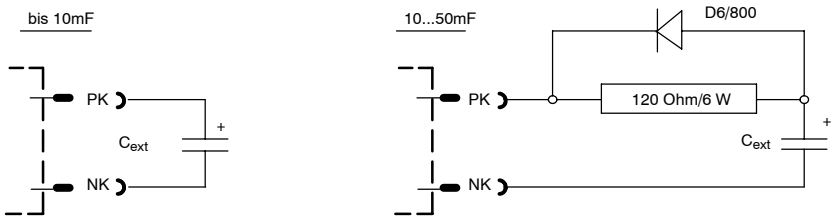


Figure 128 Port C_{ext} (on DNP 023-1, -2)

The optional capacity is to be mounted at a short distance in the same swing frame and connected with a twisted shield line of 2 x 1.5 mm².

3.7 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

3.8 Connector Pin Assignment

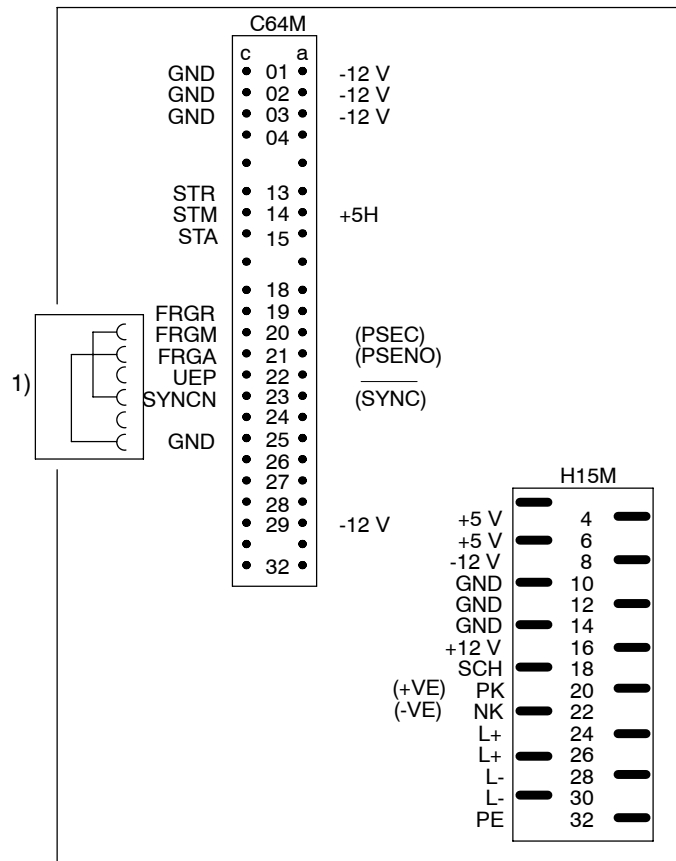


Figure 129 Assignment of the Connectors for the DNP 023-1, -2 (Looking at the Rear)

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	DTA 024, DTA 027, DTA 27.1 subracks

4.2 Supply Interface

Input DNP 023-1

L+ (U_e)	+16.8 ... 24 ... 33.6 VDC (LED 3)
I_e max (Operation)	< 17 ... 11.5 ... 8.3 A
(Switch on)	approx. 30 A for $t = 50$ msec
Fuses	2 x 3AG-30A (T)

Input DNP 023-2

L+ (U_e)	+33.6 ... 48 ... 75.0 V (LED 3)
I_e max (Operation)	< 7.7 ... 5.4 ... 3.5 A
(Switch on)	approx. 20 A for $t = 40$ msec
Fuses	2 x 3AB-10A (M)
L-	Reference potential
PE	Protective earth
SCH	Shield
Supply Cross-Section for L+ and L-	2 x 2.5 mm ²

Outputs

U_{B5}	+5.05 V / max. 20 A
I_{B5} min	> 1 A (for data observation)
U_{B12}	+12 V / max. 6 A
I_{B12} min	> 0.2 A (for data observation)
U_{B-12}	-12 V / max. 0.5 A
Reference Potential (GND)	0V
permitted Output Performance	≤ 180 W, thermal, peak < 200 W
Load Protection, Fuses	see input
Current Limit	against overload
Suppressor Diodes	against overvoltage
Switch-on Time	approx. 150 msec for 97% of U_{nom}
Memory Time	typically 2 msec with powerfail and nominal load
Memory Time Extension	see function
max. Capacitor	≤ 50 mF with $U_c \geq 160$ VDC

4.3 Enable/Monitoring

FRGR / FRGM / FRGA	
Enable	Normally closed contact/root/normally open contact
STR / STM /	
STA Fault	Normally closed contact/root/normally open contact
Loadability of the Relay	≤ 60V / 0.5 A / 10 W, 15 VA
UEP	Monitoring input (optical coupler)
	Low : 0 ... 2.9 V
	High: +3.2 ... 80 V, "good" area
SYNCH	Synchronizing input

4.4 Physical Characteristics

Format	Double Europe format, size: 6/20T
--------	-----------------------------------

Port	H15M + C64M connector
Weight	5.0 kg

4.5 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	< 100 W, referring to the nominal load

4.6 Ordering Data

DNP 023-1 Module	424 204 790
DNP 023-2 Module	424 204 799
Add. Pack. for DTA 024 / DTA 27.1	424 199 814
A3 Form Block	A91M.12-234 721

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DNP 023-3, DNP 023-4

Power Supply

Module Description

The DNP 023-3 ($U_e = 24 \text{ VDC}$) and the DNP 023-4 ($U_e = 48 \text{ VDC}$) are DC power supplies with isolation between inputs and outputs. They generate the internal supply voltages of $+5 \text{ V}$, $\pm 12 \text{ V}$, $\pm 15 \text{ V}$ and $24/48 \text{ VDC}$ as well as signals for the synchronization of several power supplies and for the undervoltage evaluation.

The modules can only be used on the slots of the controller subracks reserved for them with a H15M supply connector.

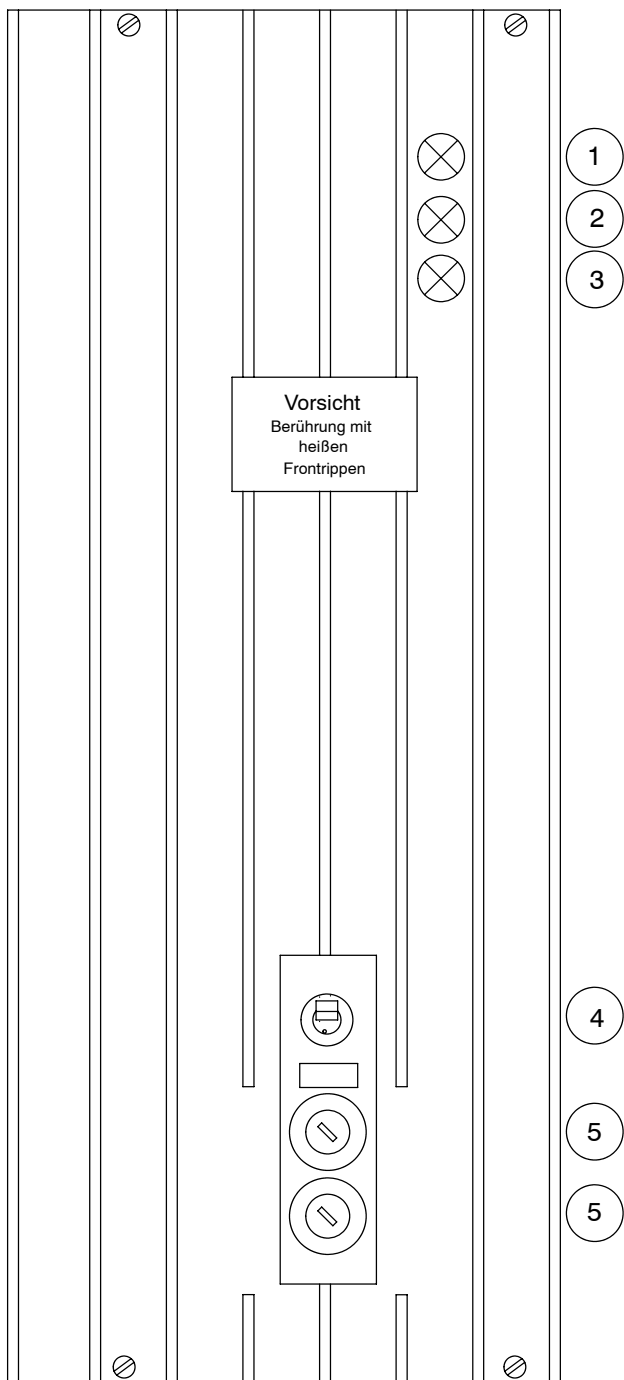
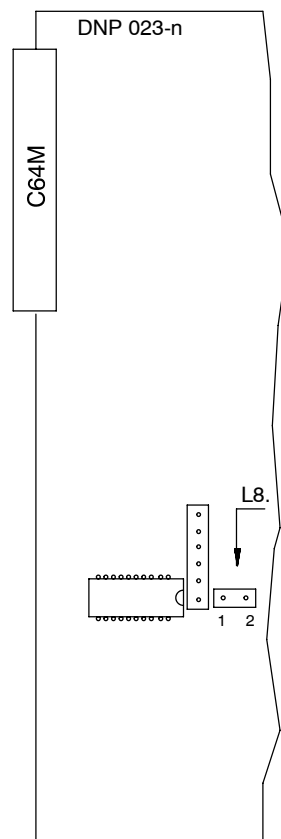


Figure 130 Font View of the DNP 023-3, -4



lefthand printed board with a 64 pole connector, looking at the equipment side (inside)

Figure 131 Survey of the Configuration Elements for DNP 023-3, -4

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 20T, rear contacting of the inputs and outputs and a front heat sink with a power switch, fused and operating indicators.

1.2 Mode of Functioning

The device types can only be distinguished in the supply voltage. The generated secondary voltages are clocked and controlled and monitored electronically for voltage deviations and overload. Monitoring and enable signals dependent on this permit several power supplies of one system to be switched on and off in synchronization. Power interruptions of up to 0.3 sec can be bridged by the additional capacity.

SYNCHN:

SYNCHN is a non-isolated input to monitor other power supplies which connect this input to GND (0 V) (preferably via FRGM-FRGA) if the device is functioning perfectly; the input is to be wired with GND for solo operation so that the power supply switches through the secondary voltages (see enable protective circuit). If the input is open or the signal is 1, the warning cycle runs, i.e., MPUSWN immediately becomes LOW while MPUSN and WWSRN become LOW after approx. 1 msec and the power supply is switched off.

FRGM (PSEC), FRGA (PSENO):

The potential-free normally open contact serves to enable other power supplies. The relay picks up for approx. 100 msec when the primary voltage is switched on and closes the FRGM-FRGA contact. If not all the voltage nominal values are reached after this time or if a fault occurs after this time, the relay immediately drops out again. The wiring of the warning signal can be designed with the connector of the add. pack for systems with 1 power supply only.

Synchronization

All the power supplies of a system are switched off for roughly 2 sec after a fault (red LED). They are then enabled again for approx. 100 msec. If the output voltages of all the power supplies do not reach their nominal values during this time, the power supplies are switched off again.

2 Operating and Indicating Elements

The heat zinc serving as the front panel includes the power switch, the two primary fuses as well as 3 light-emitting diodes for the operating state indicator:

- (1) LED Operation, green
- (2) LED Fault, red
- (3) LED Supply is present, green
- (4) Power switch
- (5) Fuse

3 Configuration

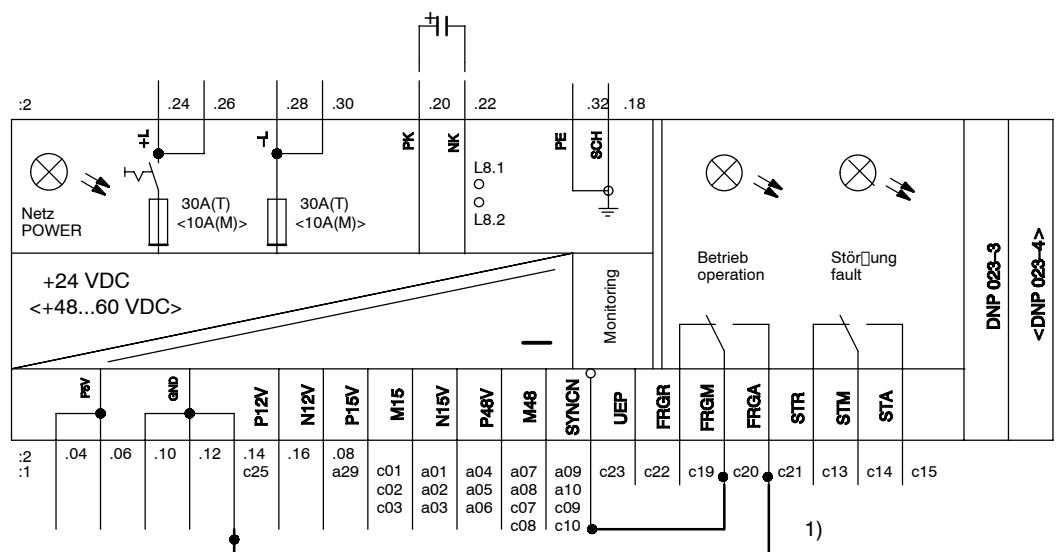
The following is to be configured:

- ☐ Wiring in the subrack
- ☐ Optional capacitor if required as a backup time extension
- ☐ Voltage control for +5 V

3.1 Settings / Protective Circuits / Indicators

There are no interventions required for the module whatsoever except for the backup time switch-over (see section 3.4 and Figure 134).

3.2 Graphical Symbols



1) Wiring of the enable for controllers with a single power supply when using the add. pack.

Figure 132 Graphical Symbols for DNP 023-3, -4

Re Figure 132:

Graphical symbol entries in < > are valid for DNP 023-4.

The enable wiring is to be extended according to Figure 127 for systems with several power supplies.

3.3 Wiring in the Subrack



Warning A wiring which is not laid out for the selected power supply can lead to the DNP 023-x power supply being destroyed.

The DTA 024 and DTA 027 subracks are supplied with or without the standard wiring for a single 230 VAC power supply depending on the revision index (enable loop). The function of any inserted power supply is blocked without the wiring of the enable loop! See Figure 127 and Fig. 120 for the necessary wiring for systems with one or more power supplies.

Table 56 Wiring Differences for DC and AC Power Supplies

Supply or Signals	DTA 024, DTA 027 with DNP 023, 230 VAC Column 1			DTA 024, DTA 027 with DNP 023-1 ... -4, 24 / 48 VDC Column 2		
Power	L	2.28		L+	2.24,	2.26
Power	N	2.30		L-	2.28,	2.30
PK (+VE)		2.24			2.20	
NK (-VE)		2.26			2.22	
FRGM (PSEC)		2.20	1)			1c20
FRGA (PSENO)		2.22				1c21
SYNCH		2.18				1c23
GND		2.14				1c25
GND		2.12		2.14		
GND		2.10		2.12		
				2.10		

- 1) Standard wiring for DNP 023: Remove this at all costs when using DNP 023-1 ... -4
 2) Connectors and labels for the rear of DTA 024/027 can be ordered separately as an add. pack.
 () Signal names in() are valid for modules labelled in English



Warning The wiring according to Table 56, column 2, required for a single DNP 023-x is to be compared with the standard wiring of the used subrack and to be altered, if necessary, for the use in the DTA 024 or DTA 027.

3.3.1 Enable Wiring

for the dependent operation of several power supplies for one system

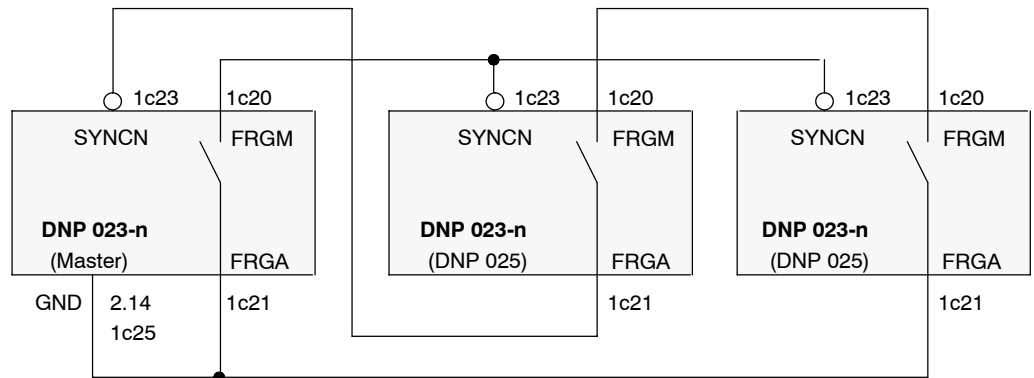


Figure 133 Enable wiring for the DNP 023-3, -4

3.4 Voltage Control for +5 VDC

If interfering voltage drop-outs occur for the connectors of the magazine supply wiring in the subrack due to a high current load or a load change, a settling of the fluctuations can be carried out to 5.05 V if necessary with a voltage feedback from the critical 5 V supply point to the input of +5H (1a14) of the power supply.

+5H is not wired: $U_{B5} = 5.15 \text{ V}$.

This feedback is already taken into account in standard sub racks.

3.5 Secondary Voltage of +48 VDC

The isolated secondary voltage of +48 VDC can be switched selectively to +24 VDC and can then be loaded with 2 A (previously 1.5 A only). 3 jumpers are therefore to be soldered in on a printed board. This conversion is carried out by the factory and is to be given with the order.

3.6 Backup Time Extension

If the standard backup time (2 msec) is to be extended, an optional capacitor can be connected to terminal 20 (+) and terminal 22 (-).

2 time ranges can be selected with the L8.1-2 jumper (only accessible after opening the shield chassis).

The time ranges and the calculation formula for the size of the backup capacitor are to be taken from Figure 134.

3.6.1 C_{ext} Optional Capacitor

Memory time (SPZ)	Capacity (C _{ext})	Jumper L8.1-2
2 ... 138 msec	0 ... 50 mF	o—o *)
83 ... 300 msec	14 ... 50 mF	-o o-

*) As delivered from the factory

The following is valid for the calculation of the capacitor:

$$C_{\text{ext}} \text{ (mF)} = \frac{\text{SPZ [ms]} - 2}{2.6 \text{ *)}}$$

SPZ = Memory time in msec
*) 5.6 with the jumper open

Port

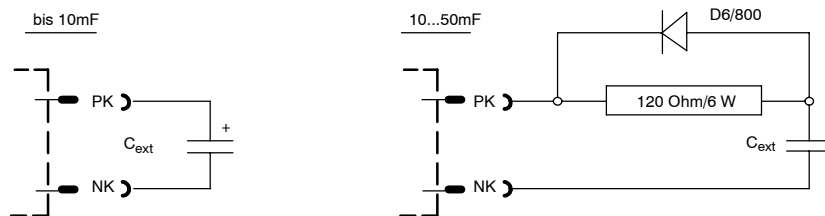


Figure 134 Port C_{ext}

The optional capacity is to be mounted at a short distance in the same swing frame and connected with a twisted shield line of 2 x 1.5 mm².

3.7 Parallelling Power Supply Outputs

Parallelling is permitted for +5 V and +12 V only and under the following prerequisites:

- ☐ Nominal output loads for each power supply is limited to < **130 W**
- ☐ with standard memory time:
wired with optional capacitor of **C_{ext} = 220 µF / 160 V**
- ☐ with memory time extension:
wired with **125 %** of the calculated C_{ext} for the desired time extension

3.8 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These forms are

- ☐ included in the form block for conventional processing
(see ordering data)
- ☐ included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version)
(in preparation).

3.9 Connector Pin Assignment

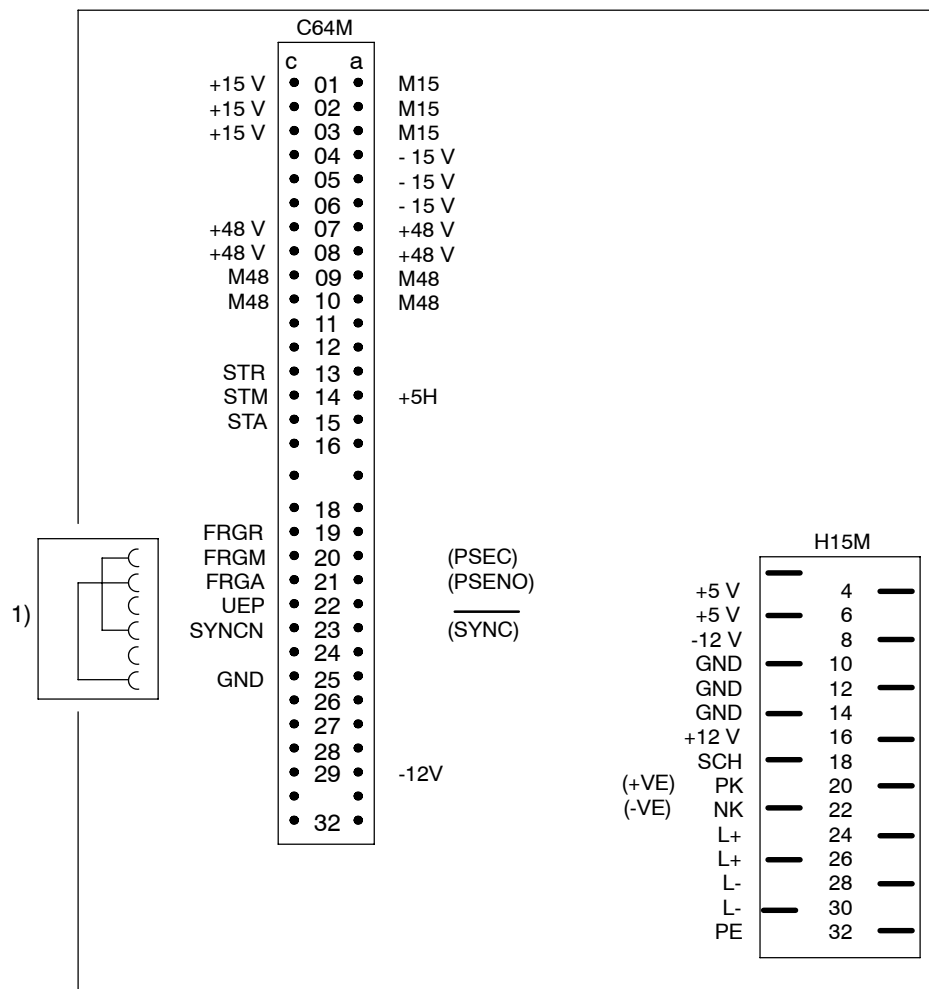


Figure 135 Assignment to the Connectors for the DNP 023-3, -4 (Locking at the Rear)

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	DTA 024, DTA 027 subracks

4.2 Supply Interface

Input DNP 023-3

L+ (U_e)	+ 16.8 ... 24 ... 33.6 V (LED 3)
I_e max (Operation)	< 17 ... 11.5 ... 8.3 A
(Switch on)	approx. 30 A for $t = 50$ msec
Fuses	2 x 3AG-30A (T)

Input DNP 023-4

L+ (U_e)	+ 33.6 ... 48 ... 75.0 V (LED 3)
I_e max (Operation)	< 7.7 ... 5.4 ... 3.5 A
(Switch on)	approx. 20 A for $t = 40$ ms
Fuses	2 x 3AB-10A (M)
L-	Reference potential
PE	Protective earth
SCH	Shield
Supply Cross-Section	2 x 2.5 mm ² for L+ und L-

Outputs

U_{B5}	+5.05 V / max. 20 A
I_{B5} min	> 1 A (for data operation)
U_{B12}	+12 V / max. 6 A
I_{B12} min	> 0.2 A (for data operation)
U_{B-12}	-12 V $\pm 3\%$ max. 2 A
Reference Potential (GND)	0 V
U_{B15}	+15 V $\pm 4\%$, max. 0.5 A
U_{B-15}	-15 V $\pm 4\%$, max. 0.5 A
Reference Potential	M15
U_{B48}	+48 V $\pm 7\%$, 1.5 A, can be switched to +24 V/2 A
Reference Potential	M48
permitted Output Performance	≤ 180 W thermal, peak < 200 W
Load protection	
Current Limit	against overload
Suppressor Diodes	against overvoltage
Switch-On Time	approx. 150 msec for 97% of U_{nom}
Memory Time	2 msec with powerfail and nominal load
Memory Time Extension	$C \leq 50$ mF with $U_c \geq 160$ VDC (times, see function)

4.3 Enable/Monitoring

Relay Port	Enable	Fault
Normally Closed Contact	FRGR	STR
Root	FRGM	STM
Normally Open Contact	FRGA	STA
Relay Loadability	≤ 60 V / 0.5 A / 10 W, 15 VAC	
UEP	Monitoring input (optical coupler)	
	Low: 0 ... 2.9 V; High: + 3.2 ... 80 V, "good" area	
SYNCH	Synchronizing input	

4.4 Physical Characteristics

Format	Double Europe format, size: 6/20T
Port	H15M + C64M connector
Weight	5.0 kg

4.5 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	< 100 W, referring to the nominal load

4.6 Ordering Data

DNP 023-3 Module	424 204 794
DNP 023-4 Module	424 204 795
Add. Pack. for DTA 024 / DTA 27.1	424 199 814
A3 Form Block	A91V.12-234 721

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DNP 028

220 VAC Power Supply

Module Description

The DNP 028 is an AC power supply with isolation between inputs and outputs. It generates the internal supply voltages of + 5 V, + 12 V, - 12 V.

The power supply also generates signals for the synchronization of several power supplies and for the undervoltage evaluation.

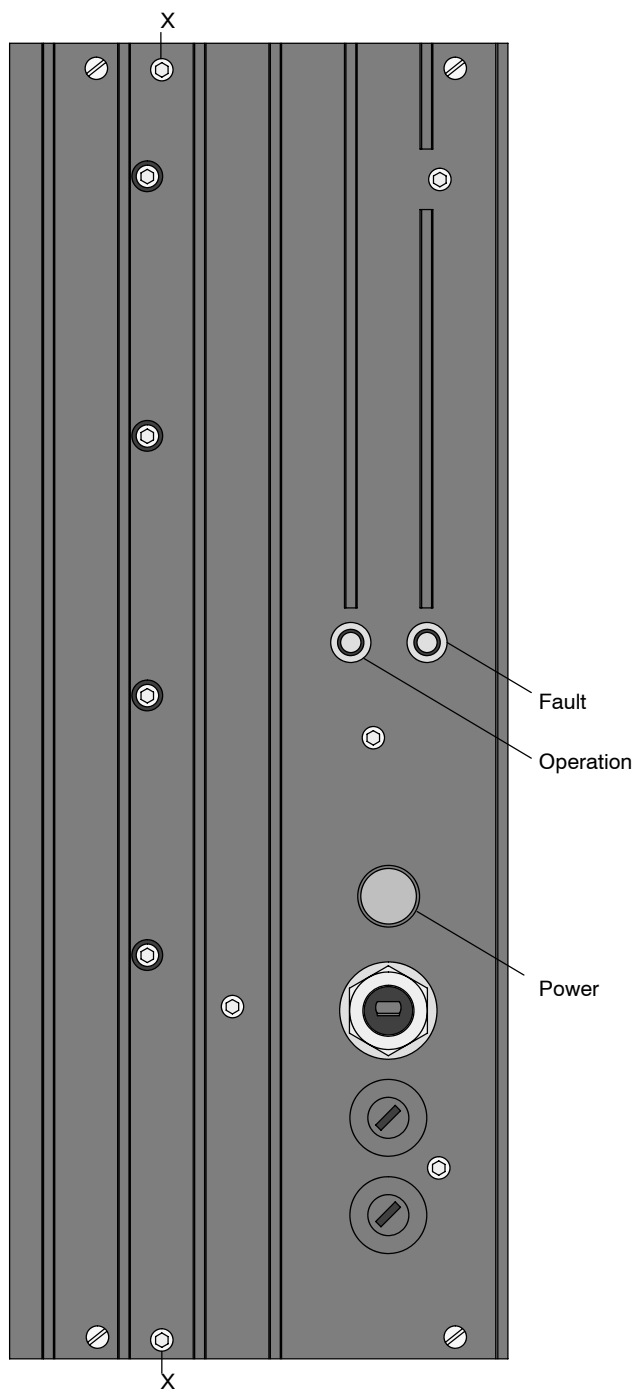
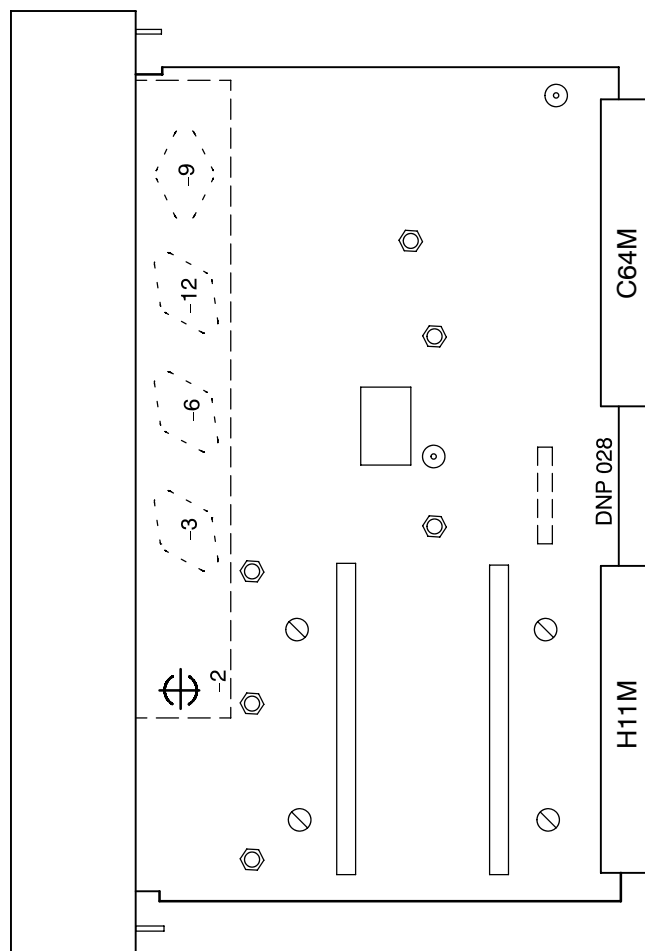


Figure 136 Front View of the DNP 028



Do not make any settings on the module. See section 2 for the indicating elements.

Figure 137 Survey of the Configuration Elements for DNP 028

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 20T, rear contacting of the inputs and outputs and a front heat zinc with fuses and operation indicator.

1.2 Mode of Functioning

The generated secondary voltages are clocked, controlled and monitored electronically for voltage deviations and overload. Monitoring and enable signals dependent on this permit several power supplies of one system to be switched on and off in synchronization.

Synchronization

All the power supplies of one system are switched off for roughly 2 sec after a fault. They are then enabled again for approx. 100 msec. If not all the output voltages reach their nominal value within this time, the power supplies are switched off again.

Parallelling

Parallelling several power supplies for the outputs is **not** permitted.

FRGR: FRGM: FRGA:

Potential-free changeover contact to enable other power supplies. The relay picks up for approx. 100 msec when the device is switched on (internally or externally) and closes the FRGM-FRGA contact. If not all the voltage nominal values are reached after this time or if a fault occurs after this time, the voltage drops out again.

STR: STM: STA

Potential-free changeover contact for the fault output

Faultless state: STR-STM closes approx. 200 msec after the device is switched on

UEP, UEN

Input separated via an optical coupler to monitor other power supplies. This input must be connected to GND (preferably via FRGM-FRGA) so that the power supply operates properly. If GND is switched away, the warning cycle runs, i.e., MPUSWN immediately becomes LOW while MPUSN and WWSRN become LOW after approx. 1 msec and the power supply is switched off.

2 Operating and indicating elements

Toggle switch		Power ON / OFF
Negative-glow lamp	ON:	Power ON indicator
(green) LED	ON:	Operation; participating power supplies are operating perfectly
	OFF:	red LED indicates type of fault
(red) LED	OFF:	participating power supplies are operating perfectly
	ON:	Fault; observed power supply (or the controlling device) has a fault
	flashes:	another power supply has a fault
Fuse	primary	2 x T 0.63 A

3 Configuration

The following is to be configured:

- ☐ Wiring in the subrack
- ☐ Coding the slot

3.1 Slot Coding

The slot in the subrack provided by the configuration is to be coded by inserting two coding screws (x, see Figure 136) as the slot of a 220 VAC component.

3.2 Connector Pin Assignment

H11M		
+ 12 V	=	2
+ 5 V	=	5
GND	=	8
GND	=	11
- 12 V	=	14
	=	17
	=	20
	=	23
L1	=	26
N	=	29
PE	=	32

Figure 138 Connector Pin Assignment for the DNP 028

3.3 Graphical Symbols

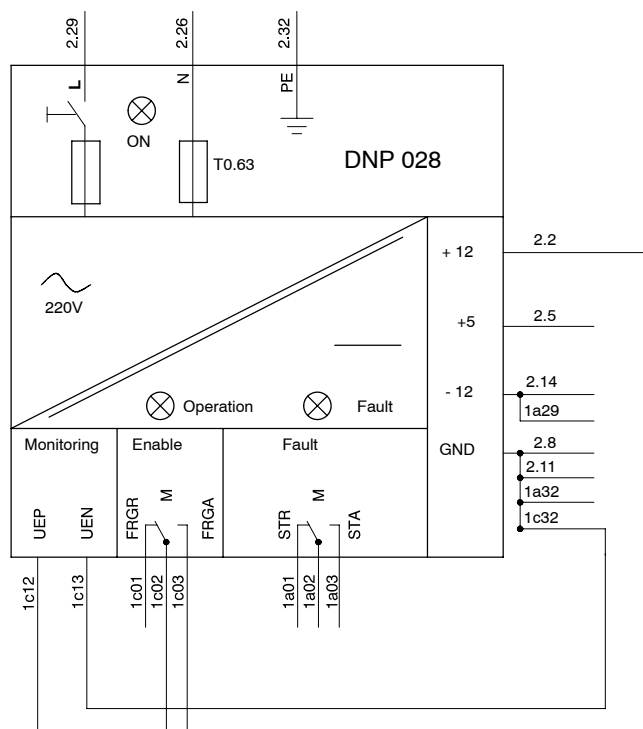


Figure 139 Standard Protective Circuit for 1 Power Supply per System

3.4 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 data bank for Ruplan processing (Technical Sales office version in preparation)

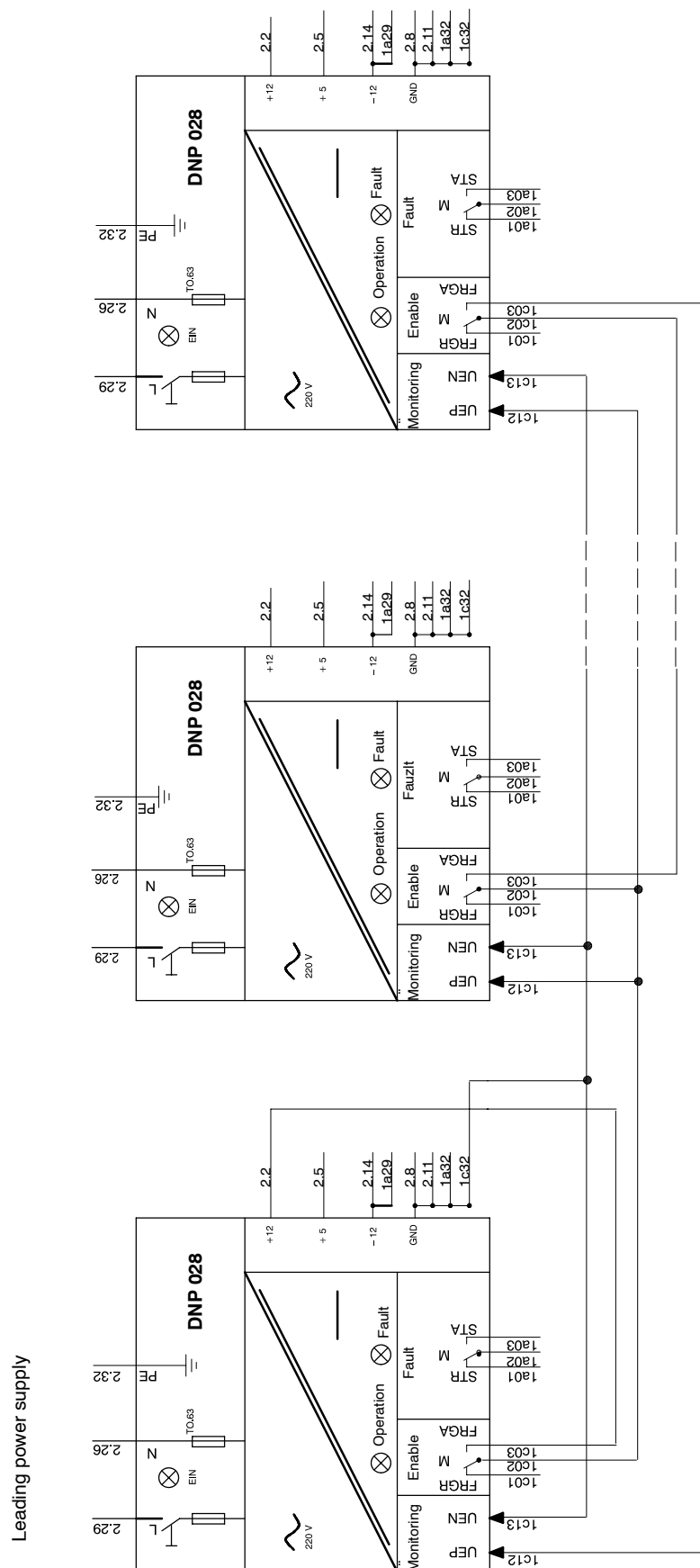


Figure 140 Standard Protective Circuit for the Dependent Operation of Several Power Supplies for one System

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	Supply structure in the DTA 028

4.2 Supply Interface

Input	with isolation, with toggle switch for 2 pole power disconnection
U _e	220 VAC +10%, -15%
	48 ... 62 Hz
I _{e max}	≤ 0.55 A
L	Mains voltage input, Ph (terminal 2.29)
N	Mains voltage input, MP (terminal 2.26)
P _E	Protective earth (terminal 2/32)
Outputs	
UB5	+ 5.05 V ± 3% max. 6 A (terminal 2.05)
UB12	+ 12 V ± 3% max. 2 A (terminal 2.02)
UB-12	- 12 V ± 5% max. 0.15 A (terminals 2.14, 1a29)
Reference Potential (GND)	0 V (terminals 2.08, 2/11, 1a32, 1c32)
Overload Protection	Fuses: 2 x T 0.63
Memory Time with Powerfail and Nominal Load	>15 msec (>1 half-wave)

4.3 Event / Networking Signals

Enable	FRGR)	Normally closed contact	(1c01)
	FRGM)	Root	(1c02)
	FRGA)	Normally open contact	(1c03)
Fault	STR)	Normally close contact	(1a01)
	STM)	Root	(1a02)
	STA)	Normally open contact	(1a03)
Relay Loadability		≤ 60 V/0.5 A/10W, 15 VA	
UEP		Monitoring input (optical coupler)	
		+ 5 ... 12 V (8 ... 26 mA): "good" area	(1c12)
UEN		Reference potential for UEP	(1c13)

4.4 Physical Characteristics

Format	Double Europe format,
Size	6 HE / 20 T
Type of Port	H11M + C64M connector
Weight	4 kg

4.5 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	< 32 W

4.6 Ordering Data

DNP 028 Module	424 199 860
A3 Form Block	A91V.12-234 721

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DTA 024

Subrack

Module Description

Standard subrack with rear connection, construction size: 19"/6HE. The main features are:

- ▣ Use for A500 controllers with one of the following central processing units:
 - ▣ ALU 821 / ALU 150 and UKA 024
 - ▣ ALU 011
 - ▣ ALU 061
- ▣ 7 PMB slots
- ▣ 5 PEAB slots
- ▣ Supply slot with a H15 connector
- ▣ Ports for direct PEAB expansion and PEAB extension via DKV 023
- ▣ Integrated CMOS backup rechargeable battery

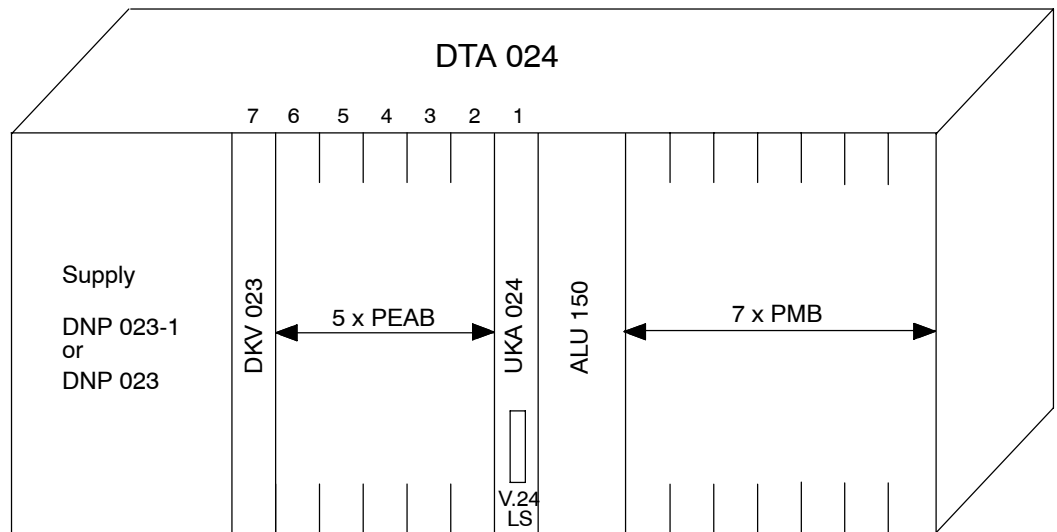


Figure 141 Front View of the DTA 024

1 General

1.1 Application

The DTA 024 is a primary subrack with 7 slots on the PMB (memory bus), 5 memory slots on the PEAB (process input/output bus) and reserved slots for the central processing unit, monitoring, PEAB networking and supply. It is used in standard configurations as well as in systems made to measure.

1.2 Physical Characteristics

The subrack has a width of 19" (48 T) and is provided as a component with rear connection to be installed in racks and swing frames. The wiring printed board designed in the press-in technique carries the connector for the PEAB and PMB ports of the insertion modules with their printed wiring and the RAK plug-in jumpers on the inside as well as the ports for the operating supply, working voltage, PEAB expansion, non-isolation and EMC measures on the rear. The battery block for the backup supply of the CMOS memory modules is also to be found there. The standard equipment is to be taken from Figure 141.

2 Operating and Indicating Elements

The subrack does not have any of its own operating or indicating elements.

3.4 Battery Block for CMOS Memory Modules

The battery port is designed in double to be able to change the battery without an interruption even if the supply is switched off. The plug-in ports are separated when delivered in order to avoid an uncontrolled exhaustion during storage.
The discharge degree of the battery block is not defined.

The replacement date is to be entered on the battery block by the user / commissioner.

3.5 Equipping the PMB Area

There are 7 slots available in the PMB area (Figure 141) (memory bus, DUM 024 wiring printed board).

Slot no. 57 ... 81	7 x 4T, memory bus node (C64F)
	SC 832, SF 8128, MPV 003, KOS 882

Slots which are not used can be occupied by expansion modules which are not PMB nodes if the adapter connector lies in the upper area of the F modules (e.g., UVL 841).
3 slots (expandable9 of the memory area are equipped with guide parts for such expansions for the direct connection of MDL 48 cables.

3.6 Equipping the PEAB Area

The PEAB area (Figure 141) (I/O bus, DUA 024 wiring board) includes 7 slots with the following reservation:

Slot no.	21	PEAB networking DKV 023 or I/O component	(C64F)
	25 ... 41	5 x 4T, I/O bus node	(C64F)
		Slot 6 (7) ... 2, 32 bits	
	45	4T, UKA 024	(Monitorings, LS/V.24)
		Slot reference 1,	(C64F + E48F)

Slot no. 33 = slot reference 4 is to be used in preference to operate the DBK 021 operating console which is 12T wide (EQL list entry), whereby the neighbouring slots of 3 and 2 are physically blocked. The DBK 021 occupies all 4 subaddresses (this must be taken into consideration for the secondary subrack).

3.7 PEAB Expansion / Extension

A DTA 025 subrack (slot references 17 ... 32 only) is controlled by the non-amplified ALU bus via an MDL 66.1 bus cable for the PEAB expansion (see (3) in Figure 142 and Figure 143). The DKV 023 bus driver is not required here. The DTA 025 is coupled via a DKV 023 to be equipped and the MDL 67 bus cable for the PEAB networking (max. 20 m and slot references 33 ... 160) (see (4) in Figure 142).

3.8 RAK Chain

The RAK chain (RAK: Request acknowledge =) determines the priority order of interrupt nodes. A continuous RAK chain is to be ensured.

If an active interrupt node is used, the jumper labelled as "RAK" on the DUA 024 (a15 - c15) of the corresponding equipment slot must be removed so that the RAK signal runs via the interrupt node.

3.9 Ventilation

If the subrack of the complete system has equipment gaps, non-occupied slots on the front of the subrack are to be closed with dummy plates to enable the correct ventilation.

3.10 EMC Measures

The 4 Z screws to be seen in the A3 form connect the internal 0 V potential with the PE cabinet earth ground.

If an operation with an isolated processing core becomes necessary due to faults, these Z screws are to be removed (factory delivery: screwed in).

A capacitive link to PE is also possible in this case if - as described in part 40, configuration, page 40-31-03 - the voltage bus designated as "0 V" (slot 0612) is connected with "PE" via 1 mohm / 4.7 μ F-400 V.

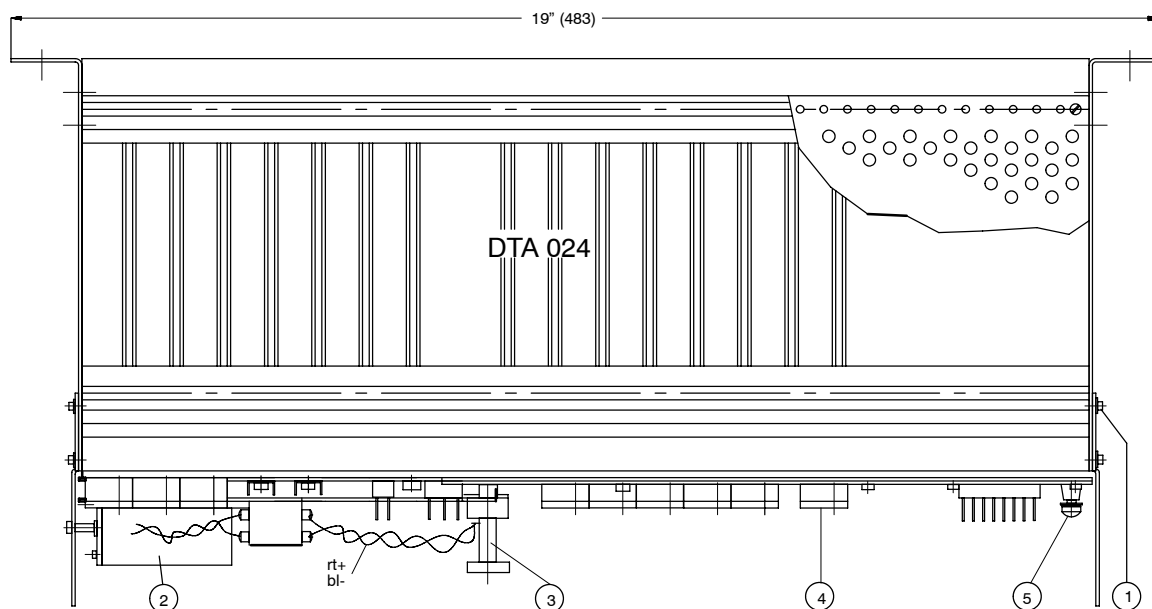
The M1, M4 reference potential is to be earthed capacitively for isolated inputs/outputs especially for semiconductor outputs: 0.1 μ F / 400 V is sufficient.

3.11 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 data bank for Ruplan processing (Technical Sales Office version) (in preparation)

3.12 Dimensions



- (1) Protective conductor terminal
- (2) CMOS backup battery
- (3) MDL 66.1 port
- (4) MDL 67 port
- (5) Central reference potential

Figure 142 Looking at the Equipment Side of DTA 024

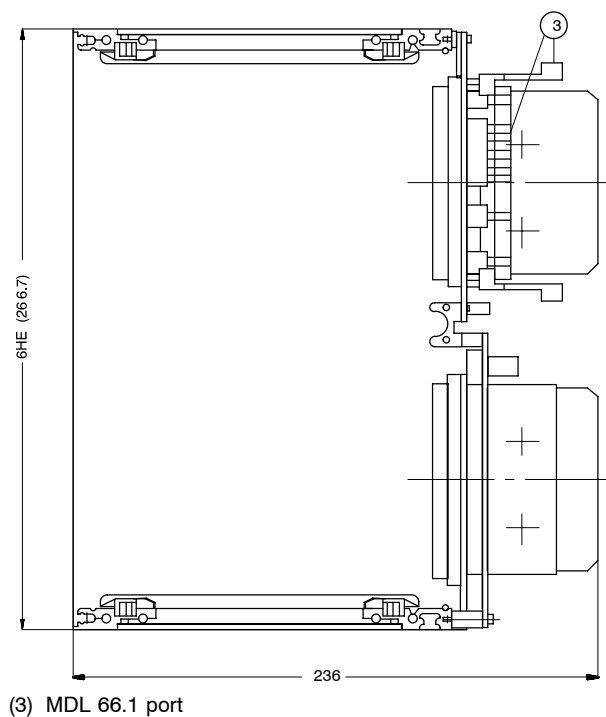


Figure 143 View of the DTA 024 without the Lateral Part

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500

4.2 Supply

Selective	
AC power Supplies	DNP 023 (230 V)
Port	3 x 1.5 mm ²
DC Power Supplies	DNP 023-1 ... 2 (24/48 V)
Secondary Voltages	+5 V, ±12 V
DC Power Supplies	DNP 023-3 ... 4 (24/48 V)
Secondary Voltages	+5 V, ±12 V, ±15 V, 24/48 V
Reference Potential	0 V, M4
Port	2 x 2 x 2.5 mm ²
PE	Earth ground potential (potential earth on the side sheet metal)
Connector Pin Assignment	see the relevant power supply

4.3 Physical Characteristics

Construction	INTERMAS 19", size: 6HE / 84T
DUA 024	Connecting printed board for PEAB nodes: suitable for UKA 023/024 starting from part no. 203 619.02
DUM 024	Connected printed board for PMB nodes, supply
Backup Capacitor	Standard equipment: without
Battery Block	NiCd pack 3.6 V/1.8 Ah, +B, -B; port; port is separate when the device is delivered
Connectors	
Power Supplies	H15M with flat-pin terminal port of 6.3 x 0.8 mm
Modules	C64F and E48F
Bus Networking	C64F, pick-a-pack for MDL 66.1
Push-on Plug Distributor	6.3 x 0.8 mm flat-pin terminal
Guide	5 for MDL 48/48L (4T)
	1 for MDL 66.1 (3T), PEAB extension for direct expansion (pick-a-pack)
	1 for MDL 67 (3T), for PEAB extension via the DKV 023 PEAB networking
EMC-Measures	4 Z screws and central earthing screws on slots 0202, 0302, 0502 connect 0 V with PE

4.4 Environmental Conditions

System Data	see A500 user manual
Safety Type	IP 00
Regulations	VDE 0100, 0110, 0160, part 1
Connection Means	Insulation category C
I/O Equipment	Only 24/60 V components are permitted!
Weight	approx. 4 kg

4.5 Ordering Data

DTA 024 Module
A3 Form Block

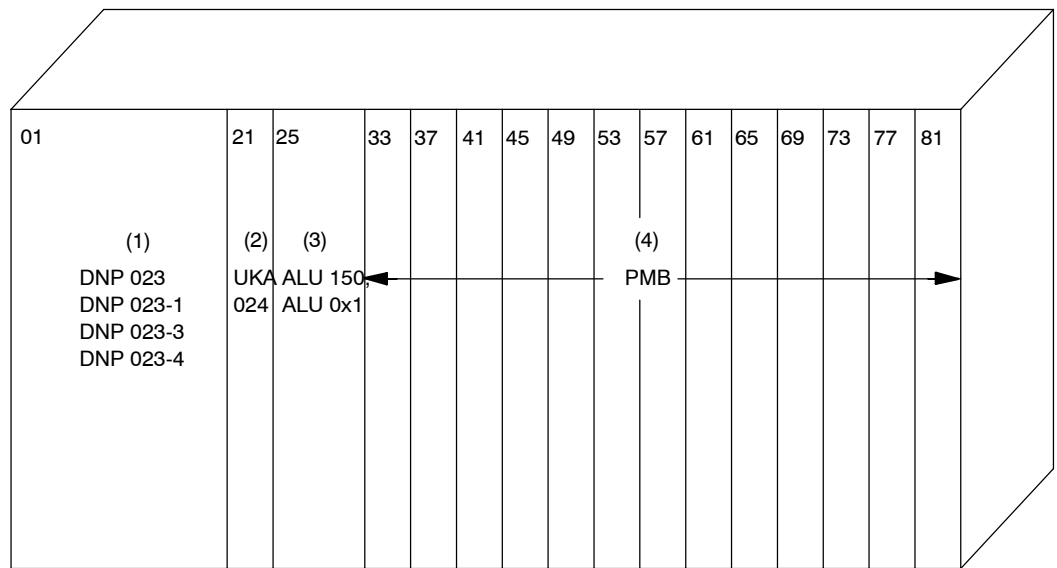
424 192 353
A91M.12 - 234 721

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DTA 27.1 Subrack Module Description

The DTA 27.1 subrack with rear connection permits A500 controllers to be set up with max. 13 memory and interface modules. Process inputs/outputs can be coupled via PEAB and Modnet 1/SFB. However, DKV 023 cannot be inserted to amplify the OEAB.

Various DC and AC power supplies are suitable as the supply. This subrack can also be used in B500-2 systems (with 10 MHz-technique) when modified physically.



- (1) Power supply
- (2) Monitoring (for ALU 150 only)
- (3) Central processing unit
- (4) Memory and interface modules

Figure 144 Front View of the DTA 27.1

1 General

1.1 Physical Characteristics

The subrack has a width of 19" with an equipment width of 84T and is only suited to being installed in 19" holders (racks, swing frames). The wiring printed board designed in the press-in technique carries the connectors for the power supply, the controller components and the memory bus nodes (Figure 144). The upper connector area is free in the area of the PMB so that the VPU-MEA bus (DUM 851) can be mounted here for the B500-2 application. 3 slots are already equipped in this area with guides for standard transfer cables for the signal transfer from KOS 882 to UVL 841 (V.24 → current loop conversion) for the A500 application. Further guides can be retrofitted if required.

A backup battery is mounted on the rear of the subrack for CMOS memory modules (separate port).

Mains and additional supplies, signals for superior fault messages (MR, MM, MA), power supply synchronization for more complicated systems (SYNCR, FRGM, FRGA), ports for a backup capacitor and the signals required for application variations which are connected to flat-pin terminal blocks for the wiring are accessible in the area of the power supply. The standard equipment is to be taken from Figure 144; specifications can be found under point 4, "Specifications".

The components for firmware and user programs, serial networking, system field bus coupling and monitoring functions known for "A500" can be used as controller modules.



Warning DC and AC power supplies do not have uniform port wiring; prohibited wiring alterations can lead to the destruction of the relevant power supply if the types are changed.

2 Operating and Indicating Elements

See “3 Configuration” for the settings

Service Intervention:

The NiCd rechargeable battery required to back up the CMOS memory modules is mounted on the rear of the subrack on the shielding sheet metal of the PMB. The port via one of the two 2 pole connectors is to be made available during the start-up: The port is separated when the device is delivered, the discharge degree undefined.

The sticker on the front of the subrack informs you about the date when the battery should be changed. The entry is to be made during the start-up.

The two connectors for the rechargeable battery port wired in parallel permit

- ☐ **with the system disconnected from the mains**
a continuous backup when changing the old (still functioning) rechargeable battery for a **charged** new rechargeable battery (see entry of the guarantee date).
- ☐ **for the supplied system**
the old rechargeable battery to be replaced by a new rechargeable battery, the discharge degree of which is undefined. The replacement does not affect the backup if there is still efficient capacitive charging time until the next supply interruption.

3 Configuration

The following is to be configured for the subrack:

- ☐ Documentation on the A3 form for supply, backup and equipment
- ☐ Signal wiring dependet on the power supply
- ☐ PEAB coupling via MDL 66.1
- ☐ System field bus coupling via BIK 151 / BIK 812
- ☐ Modifications for B500-2 applications

3.1 Assignment of the Subracks

The standard equipment shown in Figure 144 is to be varied according to the task and documented with the A3 form. The entries necessary for equipment, ordering, spatial requirements, slot no., operating means designation for components and system parts, etc., are made here.

Table 57 Assignment of the Subrack

Equipment on slot no.	Width (T)	Module	Connector in the subrack
-01	20	Power supply	(C64F + H15)
-21	4	UKA 024 (for ALU 150 only)	(E48F + C64F)
-25	8	Central processing unit ALU 0x1, ALU 150	(2 x C64F)
-33 ... -81	13 x 4	PMB node (cf. Figure 144) or UVL 841	(13 x C64F)

Slots which are not occupied are to be closed with dummy plates (ventilation).

3.2 Supply Ports

All the signal names are included in the layout of the wiring printed board. The labels on the outside of the rear wall are valid for the DTA 27.1 with 2 exceptions. Differences in the assignment or parallel supply points **occur if** corresponding DC or AC power supplies are inserted. The signal names in () are valid for AC power supplies.

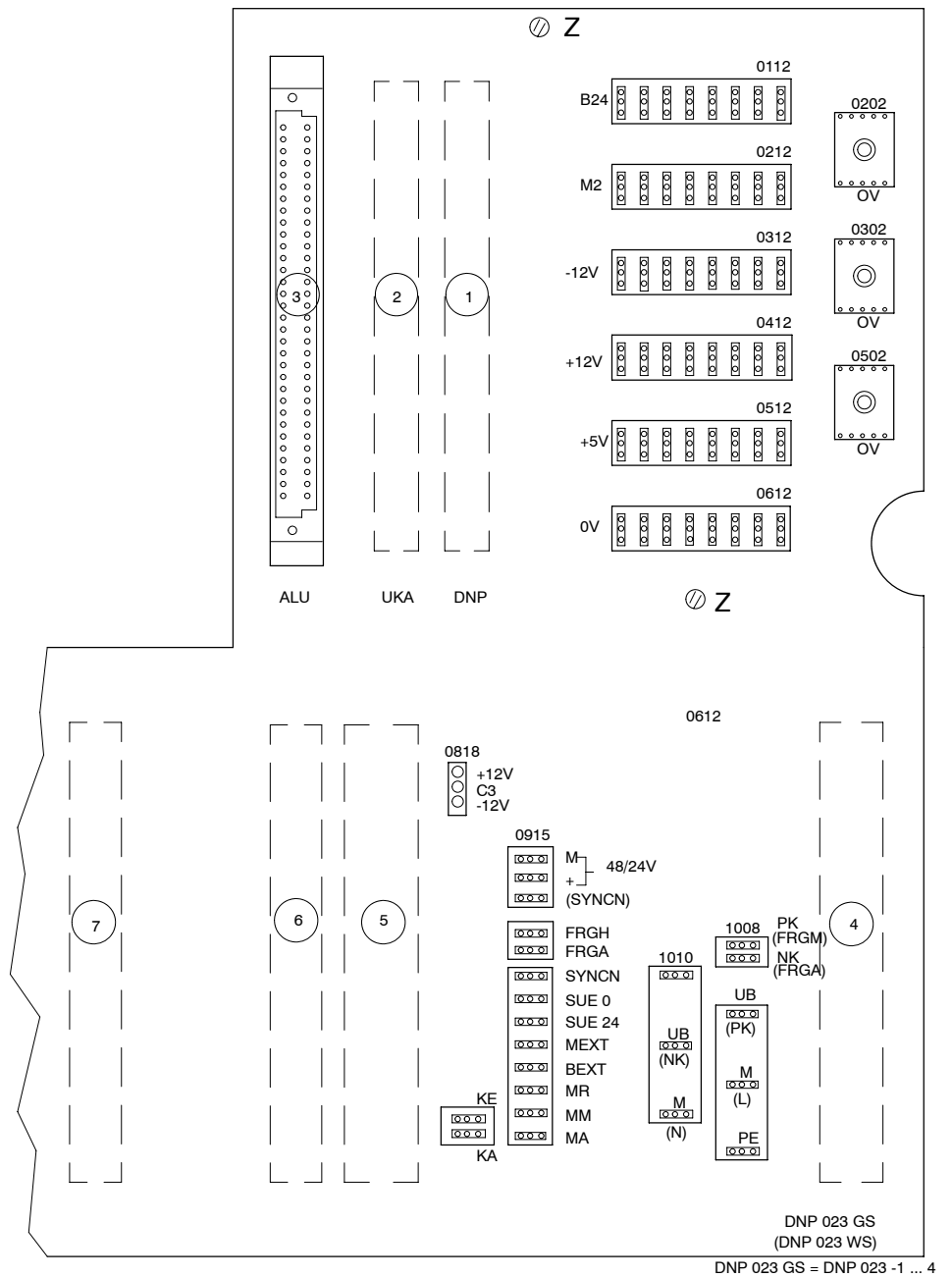
The exceptions are: Slot 0808 described in 3.6.1
Slot 0227, described in 3.13

All the secondary voltages of the power supply and the signals of the E48 connector of the UKA 024 (pilot relay contacts, SUE24/SUE0, B_{ext} / M_{ext}, monitoring the signal check loop) are guided to 6.3 mm flat pin terminals as well as all the supply voltages which are necessary to connect a B500-2 secondary subrack.

3.3 Fault Message

The potential-free changeover contact of the fault pilot relay which is located on the UKA 024 is wired to the MR, MM, MA flat-pin terminals. The contact can be loaded with 24 V/50 mA to evaluate the message. The following messages confirm the fault pilot relay:

- ☐ Undervoltage < 18 V
- ☐ Access temperature > 70 °C
- ☐ Cycle fault (deadman)



DNP 023 GS = DNP 023 -1 ... 4

- | | | | |
|-----|-----|--|---------------|
| (1) | (4) | Power supply | (C64F + H15) |
| (2) | (5) | Monitoring | (C64F + E48F) |
| (3) | (6) | Central processor with a PEAB cable port | |
| (7) | | 1st connector of the PMB area | |

Figure 145 Supply Ports (DTA 27.1, Subrack Rear)

3.4 Supply Wiring

Flat-pin terminals with insulating sleeves are to be used with a supply of 220 VAC (touch cover according to VBG 4). The voltage is guided to the L and N pins (Figure 146).

The 220 VAC supply lines (3 x 1.5 mm²) and the PK/NK lines (2 x 1.5 mm²) must be laid as shield lines whereby the shield is connected to the earth ground at one end. M4 screw ports are also available on slots 0202, 0302 and 0502 for a cabinet-to-cabinet connection of the 0 V reference potential.

The port of UB and M (M2 reference potential, contact blocks 1008, 1010, cf. Figure 146) is to be designed as double for DC supply. Cross-sections are to be taken from the "Specifications".

If the PMB slots of the DTA 27.1 subrack are to be expanded (e.g., with DTA 27.1 without a power supply) when setting up B500-2 systems, the 0 V and +5 V potentials are to be connected with 2 x 4 mm² each. The voltages ± 12 V can be wired simply.

3.5 Supply Monitoring

The wiring plan (Figure 146) which is different for AC and DC power supplies is stuck on the rear of the subrack.



Caution The wiring of the synchronizing signal is prepared (2 plug-in lines on depot slots = delivered stat) and is to be carried out in accordance with the information on the label. If the lines are left on the depot slot, the inserted power supply is blocked.

The wiring of the SYNCN signal for the operation of several power supplies in one system is to be taken from the description of the relevant power supply.

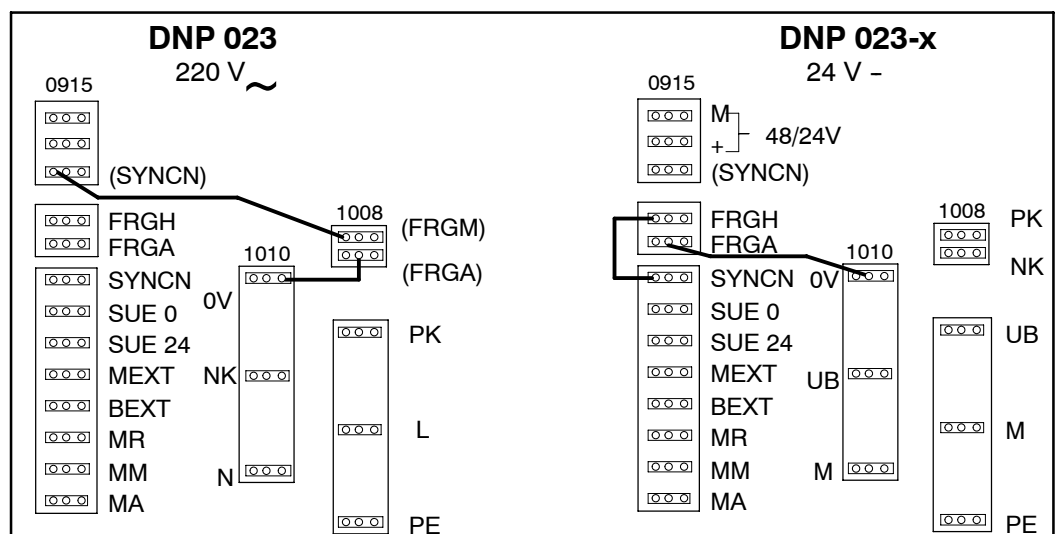


Figure 146 Sticky Label with the Wiring of the Synchronizing Signals (DTA 27.1)

3.6 Functional Jumpers in the Structure of the Power Supply

(see Figure 145)

3.6.1 Supply of PMB Components

- +12 V The jumper starting from C3 permits the selective supply of all the PMB
- C3 slots with 2 x +12 V (C3 → +12 V²⁵) or +12 V, e.g., for
- -12 V B500-2 (C3 → -12 V)

3.6.2 Current Loop Supply for UKA and UVL

The following voltage sources can be used as internal or external supply for the supply of serial interfaces:

- the primary 24 V supply when using DNP 023-1 (24 VDC), e.g., as SUE24/SUE0
- the secondary 24 V voltage (M, +) when using DNP 023-3/-4 (24/48 VDC), e.g., as Bext/Mext
- external 24 VDC when using DNP 023 (220 VAC), e.g. as SUE24 / SUE0 or B_{ext} / M_{ext}

The B24 (0112) and M2 (0212) flat-pin terminal blocks can be used as distributors for one of the voltages.

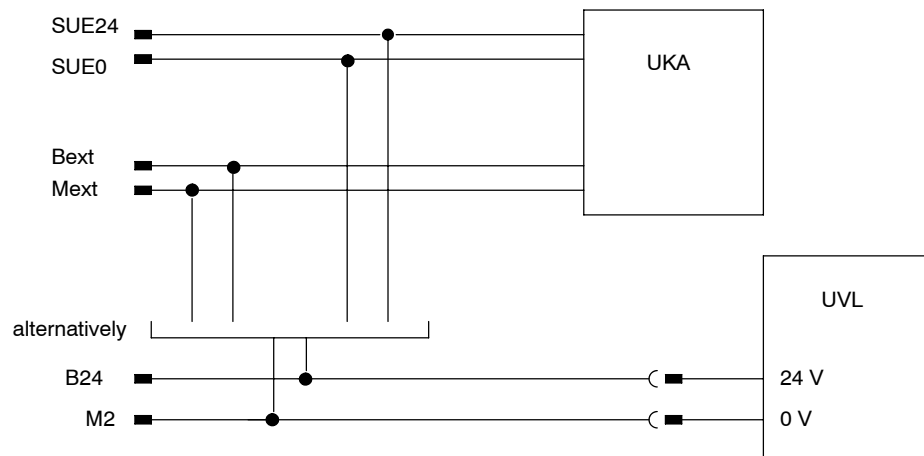


Figure 147 As Delivered: B24 → SUE24, M2 → SUE0 are Wired

The internal (SUE24, SUE0) and the external (B_{ext}, M_{ext}) supplies are wired to the UK slot. Which of the two circuits is used for the supply of the current loop interface can be selected on the UKA 024 itself using jumpers.

The other voltage can be used for the supply of the UVL interface if between UKA and UVL should be isolated. Since the UVL is not connected to a bus, the current loop supply is to be guided via the two flat-pin terminal ports of the cable plug chassis (YDL 21.n).

25) The jumper is open (neither +12 V nor -12 V) when delivered since the plug a03 plug points are jumpered with c03 for different components (e.g., KOS 882, COP 82) which can lead to the power supply being shorted if the circuit jumpers are in the incorrect positions.

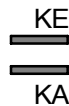
3.7 PEAB Coupling

Since the subrack does not have a slot for a PEAB coupler (DKV 023), the port of the PEAB is only possible via the post of the ALU connector which is accessible from the rear (slot 3 in Figure 145). The device is connected with the MDL 66.1 cable.

Not all the slots from the area of the slot references from 1 to 160 can be used for I/O modules. If a device is expanded for more than 14 I/O modules, the slot references of 1 ... 16 must be coded (4 subaddresses by the jumper position 0 → 0, 1 → 1), in the 1st DTA 025, whereby slots 1 and 16 must remain free for the use of the ALU 150 since their addresses are occupied by the UKA 024.

One of the slots from 2 ... 15 is converted to 3T notch elements in the process plug area (4T notch elements for process periphery). If this slot is equipped with a DKV 023, other DTA 025 can be operated with the MDL 67 cable. The first DTA 025 subrack connected to the MDL 67 must be equipped with a DKV 022.

Signal check loop



The signal check loop of the I/O modules connected in this way is connected to the rear of the DTA 27.1 at the flat-pin terminal blocks of KE / KA (see Figure 145 for the position).

3.8 Safety Measures Against Overvoltages

If the internal voltage of the modules is supplied via a power supply (belonging to the system) with a 24 VDC supply, it is to be guaranteed that no inadmissible overvoltages occur due to the switching operations of inductive actuators. These overvoltages can lead to semi-conductor inputs and outputs of the programmable controller becoming destroyed or damaged. Suitable safety measures (with suppressor diodes) are treated in detail in the user manual in the "Configuration" chapter. The safety circuits for internal voltages are integrated for the power supplies belonging to the system with a 220 VAC supply.

3.9 Backing Up the Mains

The standard backup time of the power supplies depends on the load and amounts to at least 150 μ s. An additional backup is required for industrial mains with short-term voltage dips. The +VE / -VE (PK, NK) flat-pin terminals are the port points for a back-up capacitor to extend the backup time. The capacitor must be installed outside the sub-rack. See point 3.4, "Supply wiring", for the type of wiring. The following is valid for the time extension for input : $C (PK, NK) = 2.2 \text{ mF/msec}$

3.10 Dimension Drawing of the Subrack

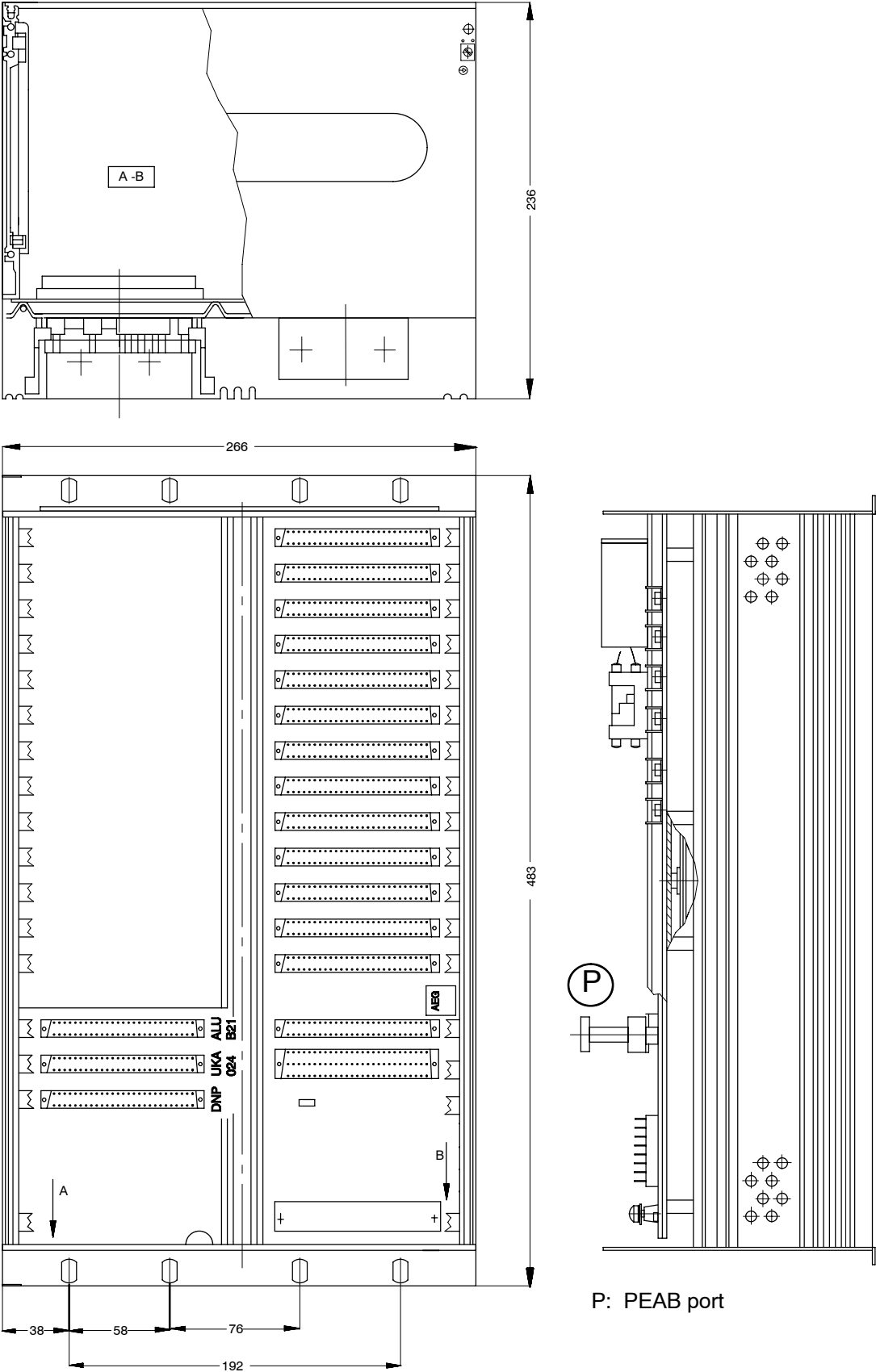


Figure 148 Dimension Drawing for the DTA 27.1

3.11 Z Screws (Central Earthing)

The chassis of each subrack is to be connected with the protective earth conductor (earthing screw on the side sheet metal) (at least 6 mm²) for reasons of touch cover.

For **reasons of interference suppression**, the internal reference potential (0 V) of the central processing unit is connected with the metal construction of the subrack (PE = protective conductor terminal = 0 V = central earthing point, as delivered) via 5 “Z screws” which are distributed over the entire wiring printed board. It is possible to loosen the 5 screws (only accessible from the rear) for an earth-free operation. The 0 V potential is the earth-free with the loosened screws and **can** be earthed capacitively (soldering eyelets in the layout). The following is preferably to be used here:

R = 1 mohm /0.5 W:	Equipment in structure 1 between the C64F connectors labelled with (DNP) and (UKA)
C = 0.1 µF/400 V:	Equipment in structure 1 between the C64F connectors labelled with (UKA) and (ALU)

The M1, M4 reference potential is to be earthed capacitively with **isolated inputs/outputs**, especially with semi-conductor outputs
with: C = 0.1 µF/ 400 V



Caution There is an increased risk of interference with earth-free operation; this is to be taken into consideration by suitable measures, e.g., physical separation between the signal and supply wiring.

3.12 Modnet 1/N Port

The signal transfer from KOS 882 to the UVL 841 (V.24 → current loop conversion) is created with the YDL 21.4 or YDL 21.8 cable types. 3 guides (can be expanded) are already available in the area of the PMB for the upper plug row.

The YDL 18.4 or YDL 18.8 cables which are connected to the E48 connector of the KOS 882 are to be used for the pure V.24 operation. The 25 pole Cannon plugs of the other side cable end can be mounted in a connector plate or in the SAE 2 cabinet connection unit. The V.24 interfaces are not supplied automatically with -12 V via the PMB but must be supplied separately via the E48 plug chassis of the YDL 18.x. The 0312 plug-in ports serve this purpose. The cable shields which are guided out at E48 plug chassis are to be connected with the “PE” flat-pin terminals (center rear).

3.13 Using the B500-2

The wiring printed board is open above the PMB area so that the VPU MEA bus (DUM 851) can be mounted here. The -12 V required for B500-2 can be derived

- at slot 0227 (inside of wiring board) via a 2.8 mm flat-pin terminal
- at slot 0312 (outside of wiring board) via 8 x 6.3 mm flat-pin terminals.

The Necessary Finishing

is carried out according to the draing no. 7328 M - 235 200.00 after the order is received. The mechanical separation of signal and control lines between the PMB and PMB' is described there. The desired division into memory slots for PMB and PMB' must be given with the order by the person carrying out the configuration, whereby the separation on the PMB board should be preferably foreseen between the following for an optimum utilization of the slots.

0849 - 0853T
or 0857 - 0861TZ

These recommended separations offer to differently size PMB' areas which also take into consideration that the DUM 851 bus board requires another 4T for RC protective circuits which protrude into the PMB area. However, this slot (49 or 57) can be used by a memory module which is 4T wide. The finishing is carried out by the manufacturer (Seligenstadt factory) exclusively and linked to the order.

Supply of CMOS Memory Modules:

When expanding the PMB structure by a complete subrack only 1 subrack may be equipped with a CMOS backup battery which then supplies both subracks. The connection - from battery slot to battery slot - is carried out by a 2-wired extension which is equipped with 2 pole ELCO connectors at both ends.

3.14 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are.

- included in the form block for conventional processing (see ordering data)
- included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

4 Specifications

4.1 Assignment

Product Family
Device

Modicon
A500, B500-2

4.2 Supply Interface	
24 VDC Supply	DNP 023-1, DNP 023-3 power supplies
48 VDC Supply	DNP 023-4 power supplies
220 VAC Supply	DNP 023 power supplies
Protective Earth	PE
Battery Block	RAM supply, NiCd pack, 3.6 V/1.8 Ah
□ Port	+B, -B (double, see operation/presentation)
Earth Grounding	M4 earthing screws on the side sheet metal
0 V → Earth Ground	Insulated structure, bridged by 5 "Z screws"; see also "3.11"
4.3 Physical Characteristics	
Module	INTERMAS, size: 6/84T with
Dimensions	W x H x T = 444 x 290 x 212 mm
Weight	3.4 kg
Dummy Plates	slots which are not occupied are to be closed with dummy plates (ventilation)
4.4 Type of Port	
□ Internal	Connector, see slots
□ NiCd Rechargeable Battery	2 x 2 pole connectors
□ Supply/Messages	Flat-pin terminals (2.8 mm or 6.3 mm)
Cross-Sections	
□ Backup Capacitor	2 x 1.5 mm ²
□ AC Supply	3 x 1.5 mm ²
□ DC Supply	2 x 2 x 2.5 mm ²
4.5 Environmental Conditions	
System Data	see A500 user manual
Safety Type	IP 00
Regulations	VDE 0100, 0110, 0160, part 1 Port means: insulation category C
4.6 Ordering Data	
DTA 27.1 Subrack	424 235 262
Dummy Plate (6HE/4T)	424 166 824
MDL 66.1 (MDL 66)	424 235 267 (192 306)
YDL 18.4 / YDL 18.8	424 200 928 / 200 929
YDL 21.4 / YDL 21.8	424 200 996 / 207 110
Connecting Board	424 200 937
A3 Form Block	A91M.12-234 721
A500 Ruplan Data Bank	in preparation

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DTA 028

Subrack

Module Description

Standard subrack with rear connection, construction size: 19"/6HE. The main features are:

- Use for A500 controllers with one of the following central processing units:
 - ALU 821 / ALU 150 and UKA 024
 - ALU 011
 - ALU 061
- 3 PMB slots
- 10 PEAB slots when using the DNP 028,
13 PEAB slots when using the DN0 028
- Supply slot with a H15 connector
- Connections for direct PEAB expansion and PEAB extension via DKV 023
- Integrated CMOS backup battery

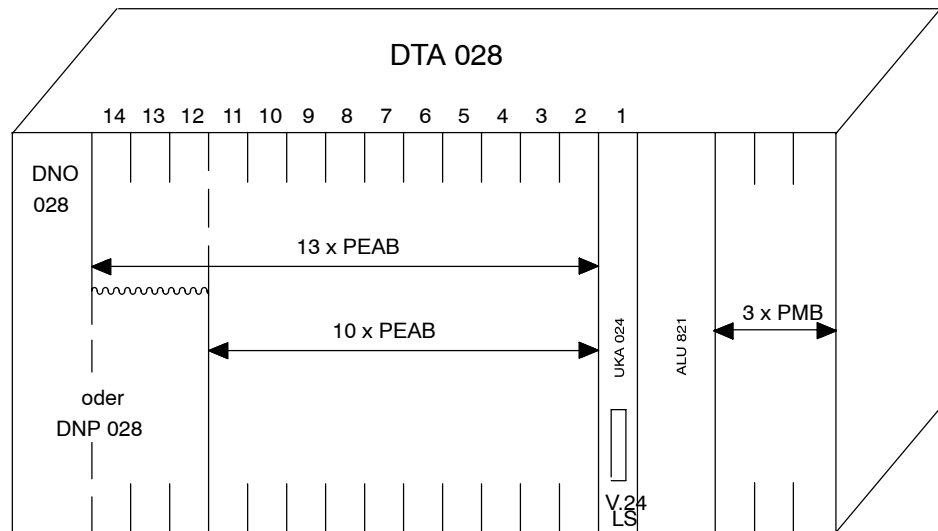


Figure 149 Front View of DTA 028

1 General

1.1 Use

The subrack is a primary subrack for a compact system structure. The PEAB area (I/O bus) offers 10 ... 13 slots for I/O modules and a fixed slot for UKA 024 (central monitoring, indicator) and ALU (central processing unit) each depending on the power supply used. The PMB are (memory bus) offers 3 slots.

1.2 Physical Characteristics

The subrack is 19" (84 T) wide and is suitable for the installation in racks and swing frames as components with rear connection. The wiring printed board designed in the press-in technique carries the connectors for the PEAB port of the insertion modules, the RAK and the subaddress plug-in jumpers on the equipment side as well as the ports for the supply, working voltage, PEAB coupling, non-isolation and EMC measures (Z screws) on the rear.

The standard equipment is to be taken from Figure 141.

2 Operating and Display Elements

The subrack does not have any of its own operating or indicating elements.

3 Configuration

The following is to be configured for the subrack:

- ☐ Supply, reference potentials
- ☐ Equipment
- ☐ Synchronization if there are several supply modules
- ☐ Mechanical supplement for different plug-in modules
- ☐ Wiring of monitoring signals
- ☐ Earthing and EMC measures
- ☐ PEAB extension / expansion

3.1 Switching of the Subrack

- ☐ Mains supply for the connector of the supply module
- ☐ Secondary operating voltages for flat-pin terminal contact strips
- ☐ Backup battery via 2-pole connectors
- ☐ Reference potential for the earth at screw connections

3.2 Supply

The supply of DNO 028 / DNP 028 is connected with flat-pin terminal contacts on the rear of the slot of the power supply. The individual voltages on the secondary side +5 V and ± 12 V are prewired to distribution soltering tags.

The accompanying, self-adhesive fill-in label next to the plug-in connection of the supply module (rear) is to be changed if necessary.

3.3 Synchronization

The SYNCN synchronization signal is prewired for the use of a single DNO 028 or DNP 028. The SYNCN signals of individual power supplies are to be wired according to the selected system configuration when using additional DNPs (e.g., DNP 025) in one system (see the module description of the corresponding power supply or the A500 publication, "Configuration").

3.4 Battery Block for CMOS Memory Modules

The battery connection is designed as double so that the battery can be changed without any interruptions even if the supply is switched off. The plug-in connections are separated when the device is delivered in order to avoid unchecked exhaustion during storage.

The discharge degree of the battery block is not defined.

The date for a battery change is to be entered on the battery block by the user / person starting up the device.

3.5 Equipment of the PMB Area

2 slots are available in the PMB area (memory bus).

Slot no. 73 ... 81 3 x 4T, memory bus node (C64F)

SC 8256, SF 8128, SF 8512, MPV 003, KOS 882

Slots which are not used can be occupied by supplementary modules which are not PMB nodes if the transfer connector is in the upper area of the F module (e.g., UVL 841). 1 slot of the memory area is equipped with guides for the direct connection of an MDL 48 cable for such supplementation.

3.6 Equipment of the PEAB Area

The PEAB area (I/O bus) offers 10 ... 13 slots for I/O modules and a fixed slot for UKA 024 (central monitoring, indicator) and ALU each depending on the power supply used. The signals of the monitoring module UKA 024 are guided to an E48F connector. The UKA is not required when the ALU 0x1 is used.

Slot 0249 = slot address 4 is preferably to be used to operate the operating console DBK 021 which is 12T wide (EQL entry), whereby the neighbouring slots of 2 and 3 are blocked mechanically. The DBK 021 occupies all 4 subaddresses.

3.7 PEAB Expansion / Extension

- ❑ without the PEAB networking (DKV 023)
Port of a DTA 025 secondary subrack with MDL 66.1 (notch elements for cable connectors are on the rear in slot area 0265, cable length 700 mm).
- ❑ with the PEAB networking (DKV 023) (bus length max. 20 m)
Select any PEAB slot for DKV 023, replace its 4T notch elements for 3T notch elements and connect the expansion to DKV 023 by directly plugging in MDL 67. Equip the DTA 025 with DKV 022.

3.8 RAK Chain

The RAK chain (RAK: Request acknowledge = request confirmation) determines the priority order of interrupt nodes. A continuous RAK chain is to be ensured here.

If an active interrupt node is used, the jumper of the corresponding equipment slots designated with "RAK" on the DUA 024 (a15 - c15) must be disconnected so that the RAK signal runs via the interrupt node.

3.9 Ventilation

If the subrack of the complete system has equipment gaps, slots which are not occupied are to be closed with dummy plates on the front of the subrack to ensure a correct guidance of the cooling air.

3.10 Port of the Periphery

- via the V.24 interface:
Slot 81 is prepared with 4T notch elements for serial I/O via the KOS 882 in the PMB area. The connection to the connecting board or SAE 2 is made with the YDL 18.4 or YDL 18.8 cable.
- via the V.24/LS interface with UVL 841:
If the V.24 interface of the KOS 882 is to be converted with UVL 841 to a current loop,
 - you must retrofit another PMB slot with 4T notch elements for UVL 841
 - you must connect the E48M connectors of KOS 882 and UVL 84x with the YDL 21.4 cable
 - you must loop the port of the periphery directly to the front panel of the UVL 84x or
 - you must loop the port of the periphery via the SAE 2 cabinet connection.

The RS 232C interface of the KOS 882 is to be supplied with -12 V by means of additional wiring in the following way:

- Use line with flat-pin terminals of 6.3 x 0.8 mm on both ends.
- Slot 0470 is to be connected to the "-12 V" port of the cable connector chassis on the rear of the subrack.

Shields of used cables are to be laid to PE on the DTA 028.

3.11 EMC Measures

The 4 Z screws which can be seen in the A3 form connect the internal 0 V potential to the PE cabinet earth.

If an operation with an isolated processing core becomes necessary due to malfunctions, these screws are to be removed (factory delivery: screwed in).

A capacitive connection to PE is also possible in this case if the potential rail designated with "0 V" (slot 0612) is connected to "PE" via 1 MOhm / 4.7 μ F-400 V - as described in part 40, configuration, page 40-31-03.

The reference potentials of M1 and M4 are to be earthed capacitively with isolated inputs/outputs and especially with semi-conductor outputs: 0.1 μ F / 400 V is sufficient.

3.12 Documentation

DIN A3 form sheets are available for the (Ruplan) processing for the project-specific documentation. Forced or standard settings of circuit elements are already entered here. These form sheets are included in the form block

- for conventional processing and in the A500 data bank
(see ordering data)
- for Ruplan processing (TVN version)
(in preparation)

Wiring
Rear

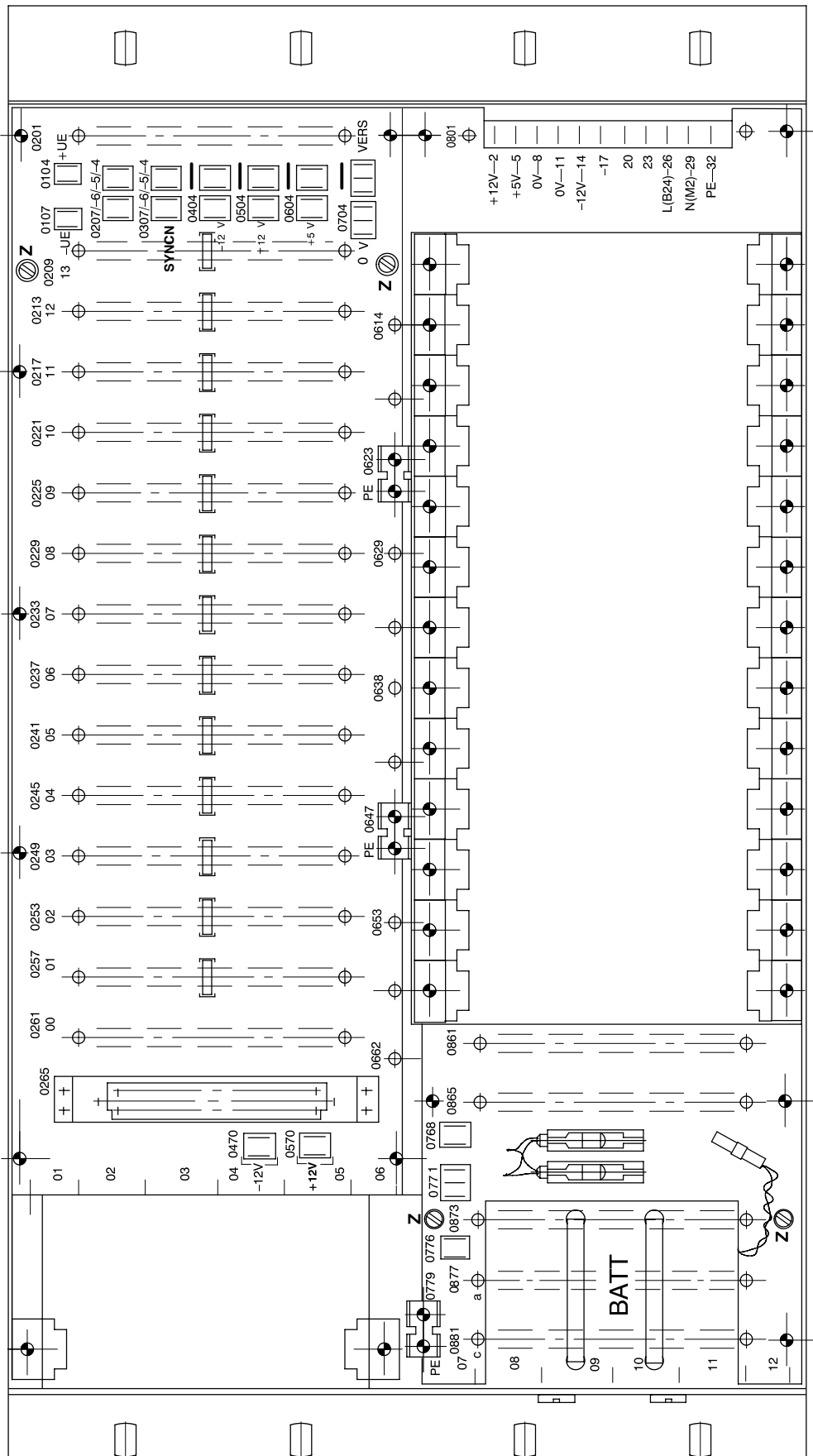


Figure 150 Rear View of the DTA 028

3.13 Dimensions

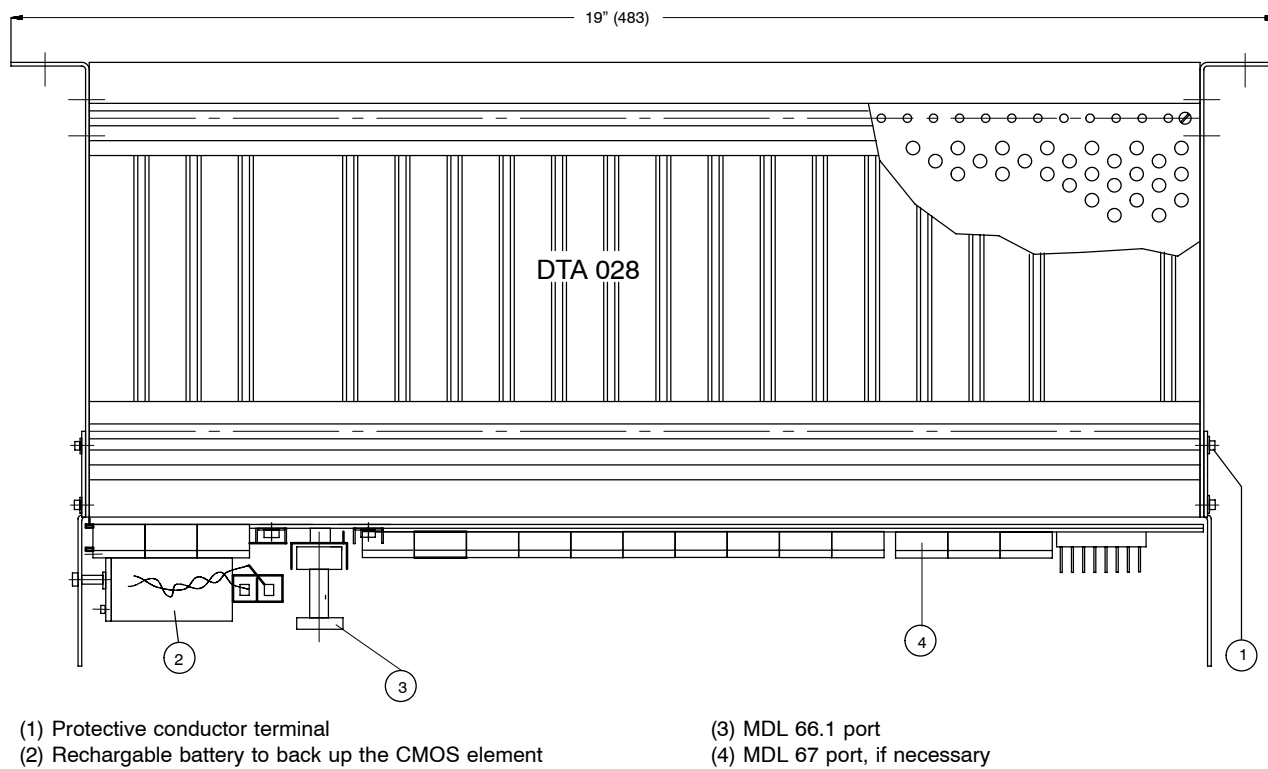


Figure 151 Locking at the Equipment Side of the DTA 028

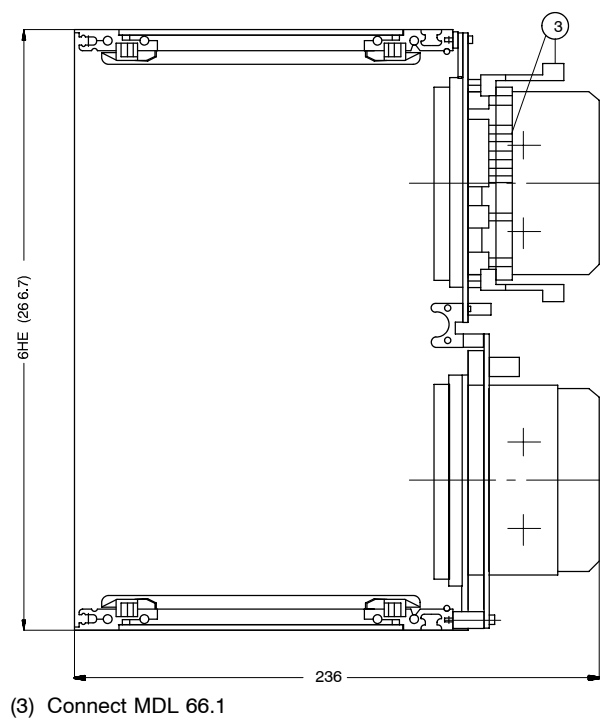


Figure 152 Illustration of DTA 028 without the lateral part

4 Specifications

4.1 Assignments

Product family	Modicon
Device	A500

4.2 Physical Characteristics

Construction	INTERMAS 19", size: 6/84
Includes	
□ DUA 028	Connecting printed board for PEAB and PMB busses, Supply
□ Capacitor Energy Store	Standard equipment: without with backup: ports H11-20, 23 for an external capacitor
□ Battery Block	NiCd pack, 3.6 V / 1.8 Ah, separate port when delivered
□ Connector	see supply
□ Guide	13 x 4T for MDL 48/48L (1 for serial I/O) 1 x 3T for MDL 66.1, PEAB extension 1 x 3T for direct extension (pick-a-pack)
Dummy Plates	Slots which are not occupied are to be closed with dummy plates (ventilation)
Slots	No. in the window in the front panel
□ No. 01	8T, supply for DNO 028 (C64F, H11) or 20T, supply for DNP 028 (C64F, H11)
□ Nos. 13(21) ... 57	13 (10) x 4T, I/O bus node (C64F)
Note:	Use 24/60 V components only!
□ No. 61	4T, UKA 024 slot reference 1 (C64F + E48F)
□ No. 65	8T, ALU 821 (2 x C64F)
□ Nos. 73 ... 81	3 x 4T, memory bus node (C64F)
Supply	via a H11 connector: DNO 028 (24 VDC) or DNP 028 (220 VAC)
Ports	for flat-pin terminals 6.3 x 0.8 mm
□ +5 V	H11-5 , 0604
□ +12 V	H11-2, 0504 , 0570
□ -12 V	H11-14 , 0404 , 0470
0 V Reference Potential	H11-8,11, 0704
PE	H11-32, 0623, 0647, 0779
Z Screws	0209, 0609, 0773, 1273: Central earthing screws for EMC measures; they connect 0 V with PE
RAM +B, -B Supply	Battery port (in duplicate, see function)

4.3 Environmental Conditions

System Data	see A500 user manual
Format	size: 6/84T
Safety Type	IP 00
VDE	0100, 0110, 0160, part 1
	Port means, insulation category C
Weight	approx. 4 kg

4.4 Ordering Data

DTA 028 Module	424 210 290
NiCd Rechargeable Battery	424 142 148
6HE/4T Dummy Plate	424 166 824
A3 Form Block	A91V.12 - 234 721

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DTA 101 Subrack Module Description

The DTA 101 subrack accepts controller modules in the left-hand half. The 2nd half which is separated electrically serves as an input/output unit for modules with front connection and is controlled via the Modnet 1/SFB.

The subrack is therefore equally suitable for programmable controllers with a small and large process signal scope; the subsequent hardware expansion of the inputs/outputs can simply be carried out by extending the Modnet 1/SFB.

The subrack is designed exclusively for inputs/outputs via the Modnet 1/SFB so that operating PEAB inputs/outputs are not possible even via a secondary subrack.



Caution The subrack is not suitable for the operation with the ALU 061!

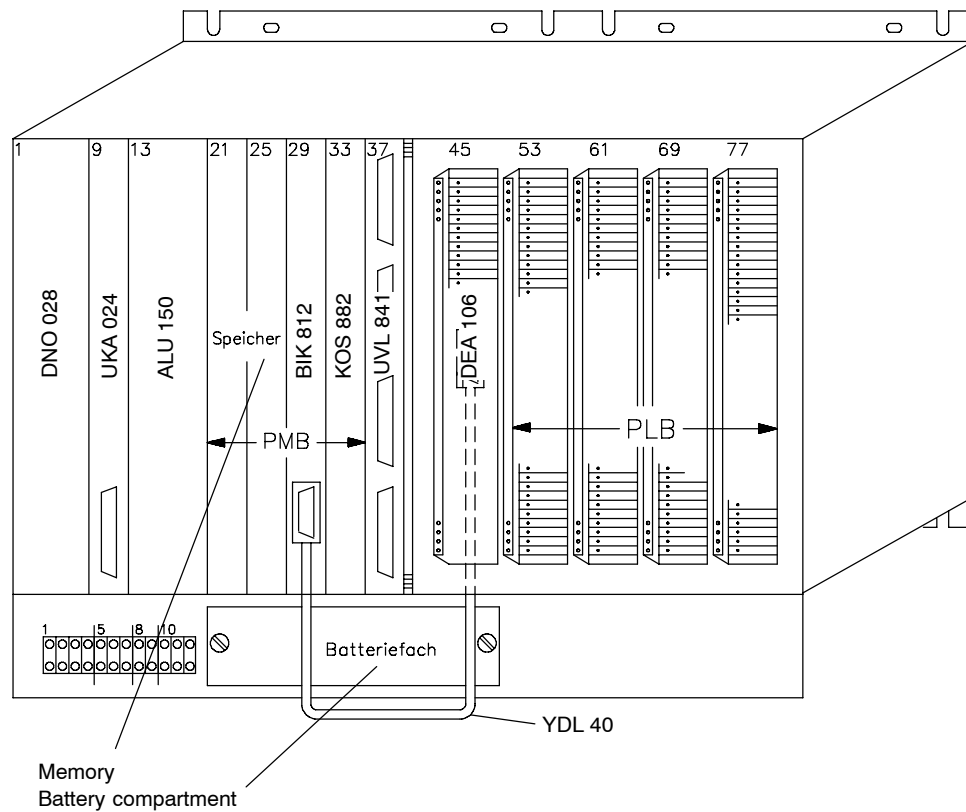


Figure 153 Standard Equipment of the DTA 101

1 General

1.1 Physical Characteristics

The subrack has a width of 19" and is suitable for a wall mounting and also for integration in 19" holders. Mounting flanges (6HE) are available as accessories for the latter installation. They are screwed down to the narrow sides of the subrack. The subrack includes 2 wiring printed boards, each with 40T for component slots.

Looking at the front, the left-hand half accepts the memory bus nodes of the controller (PMB = Parallel Memory Bus) while the PLB nodes (PLB = Parallel Local Bus) for (distributed) inputs/outputs are accommodated in the right-hand half. The connection to the right-hand half is to be created with the bus cable YDL 40 which connects the BIK 151 or BIK 812 with the DEA.

The standard equipment is to be taken from Figure 153.

1.2 Mode of Functioning

The front ports of the inputs/outputs are covered by a mobile front panel but the functional indicators and insertable individual labels for the port assignment can still be seen.

The components known by "A500" are used as controller modules. The right-hand half of the subrack is equipped exclusively with I/O modules with front connection. The two wiring printed boards are designed so that rear access for setting or service purposes is not necessary.

The plug order shown in Fig. 146 is to be observed when using KOS 882 with the adaptation module UVL 841 since the connection between KOS and UVL is only available in this area on the wiring printed board. This connection is to be created with the YDL 21.4 cable with the DTA 024 / 027.

The power supply is supplied via a 12-pole terminal block (see Figure 154). Signals for superior error messages (MR, MM, MA) and those for the synchronization of the power supplies (FRGM, FRGA) for more complicated systems are also available here. See "Configuration", section 3.2, for the labelling of the terminal block.

The internal supply of the inputs/outputs flows via the Modnet 1/SFB port as far as the I/O coupling is concerned. The isolated working and sensor voltages and the relevant reference potential are guided directly to the I/O modules via the front terminals.

2 Operating and Indicating Elements

A plastic holder for the 11-pole screw/plug-in terminals is inserted in the dummy cover (center of the subrack) (process coupling). The accompanying gray labels are foreseen for the numbering of the subracks and are to be stuck above the notch lever of the front panel.

Service Intervention:

The lower edge of the subrack is formed by a mounting angle which carries the supply terminals and a covered battery compartment. The NiCd rechargeable battery required to back up the RAM modules is accessible after opening the cover (snap fastening). The port is one of the two 2-pole connectors. However, the connection is separated when the machine is delivered and the charge status undefined. The label on the front of the subrack informs you about the deadline for changing the battery. You are to make an entry when you start up the machine.

The two connectors for the battery connection which are wired in parallel permit

❑ a back-up free of interruption

when the system is not supplied with voltage while the old (still functioning battery is replaced by a new charged battery (see the entry of the guarantee date).

❑ if the system is supplied with energy,

the old battery can be replaced by a new battery the charging condition of which is undefined. Changing the battery does not affect the back-up if there is sufficient re-charging time available until the next interruption in the supply.

3 Configuration

The following is to be configured for the subrack:

- ❑ Occupation with modules (A3 form)
- ❑ Supply port
- ❑ Supply monitoring (enable wiring)
- ❑ Mains backup
- ❑ Safety measures against overvoltages
- ❑ Z screws, Z jumpers
- ❑ Mounting type

3.1 Occupation of the Subrack

The standard equipment shown in Figure 153 is to be supplemented with memory and I/O components in accordance with the task.

A DIN A3 form, in which required entries are made for the equipment, ordering, spatial requirements, slot no. and operating means designation (components and system parts), is available for the occupation.

The slot no. can be read through the bore in the top left-hand corner of module front panels; it is not identical to the slot reference to be given during the programming.

3.2 Supply

3.2.1 Terminals

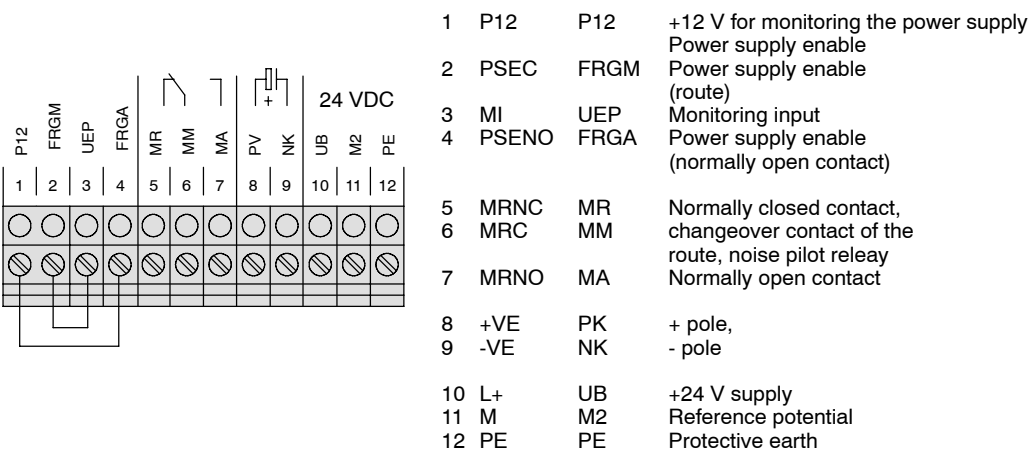


Figure 154 Terminals on the DTA 101

3.2.2 Supply Monitoring

The ports of the DNO 028 to monitor and enable other power supplies are guided to terminals 1 ... 4 (see 3.2.1).

Terminals 1 + 4 and 2 + 3 are jumpered as standard and as shown (wiring for systems with only 1 power supply). See the module description of DNO 028 for extensions for several power supplies.

3.2.3 Error Message

The potential-free changeover contact of the noise pilot relay which is located on the UKA 024 or ALU 0x1 is wired to terminals 5 ... 7 (MR, MM, MA).

The contact can be loaded with 24 VDC / 50 mA to evaluate the message.

The following messages confirm the noise pilot relay:

Undervoltage	< 18V
Excess temperature	> 70 °C
Cycle malfunction	(deadman)

3.2.4 Safety Measures against Overvoltages

The internal voltage supply of the modules is carried out via a power supply belonging to the system with 24 VDC supply. Three-phase power supplies which consist of a transformer and three-phase jumper only are normally used for this and for the supply of sensors and actuators; smoothing capacitors are not normally necessary.

However, it is to be guaranteed that no inadmissible overvoltages occur through switching operations of inductive actuators. Such overvoltages can lead to the semi-conductor inputs and outputs of the programmable controller being damaged or destroyed.

Suitable safety measures (with suppressor diodes) are treated in detail in the user manual in the "Configuration" chapter.

3.2.5 Mains Backup

The standard backup time of the power supply depends on the load and amounts to at least 150 µs. An additional backup is required for industrial mains with short-term voltage dips. Terminals 8 and 9 (PK, NK) are the connecting points for a back-up capacitor to extend the backup time.

The following is valid for input voltages > 19 VDC for the time extension:

$$C \text{ (PK, NK)} = 2.2 \text{ mF} / \text{msec}$$

3.3 Z Screw, Z Jumper

The chassis of each subrack is to be connected to the protective earth conductor for reasons of interference suppression (via the earthing screw on the side sheet with at least 6 mm² Cu).

The internal reference potential of 0 V of the central processing unit is connected to PE via “Z screw” for EMC reasons (= central earthing, delivery state). Loosening the 3 screws is possible to achieve more favourable EMC conditions for certain spatial arrangements (the screws are accessible after removing the rear cover).

The central earthing of distributed unit (DTA 102, DTA 103) is also possible using the “Z jumper” accessible from the front.

The 0V potential is earthed capacitively if the jumper is open (depot slot = factory delivery (1.2 MΩ / 0.5 W and 2 x 0.1 μF / 400 V distributed capacity)).

You should preferably proceed as in Figure 155: The Z screws in the primary subrack remain screwed in; the Z jumpers are located on the depot slot (right) in all other sub-racks.

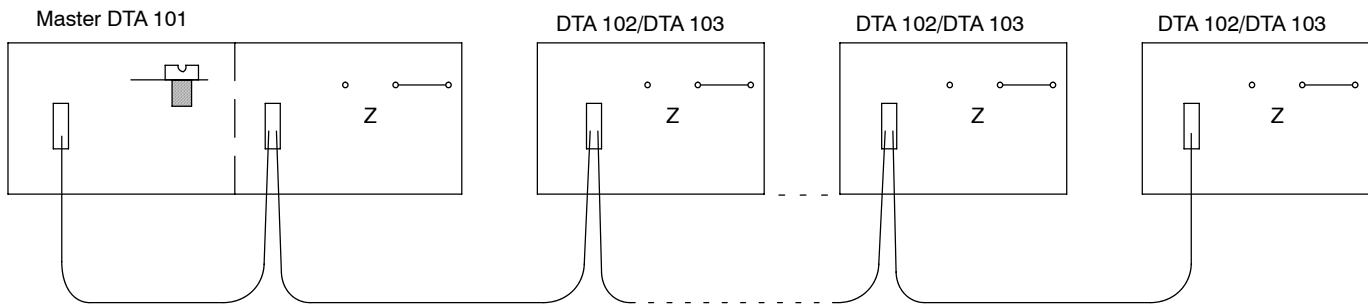


Figure 155 Z Screws (DTA 101)

3.4 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 data bank for Ruplan processing (Technical Sales Office version) (in preparation)

3.5 Dimension Drawing - Subrack

*) for M5

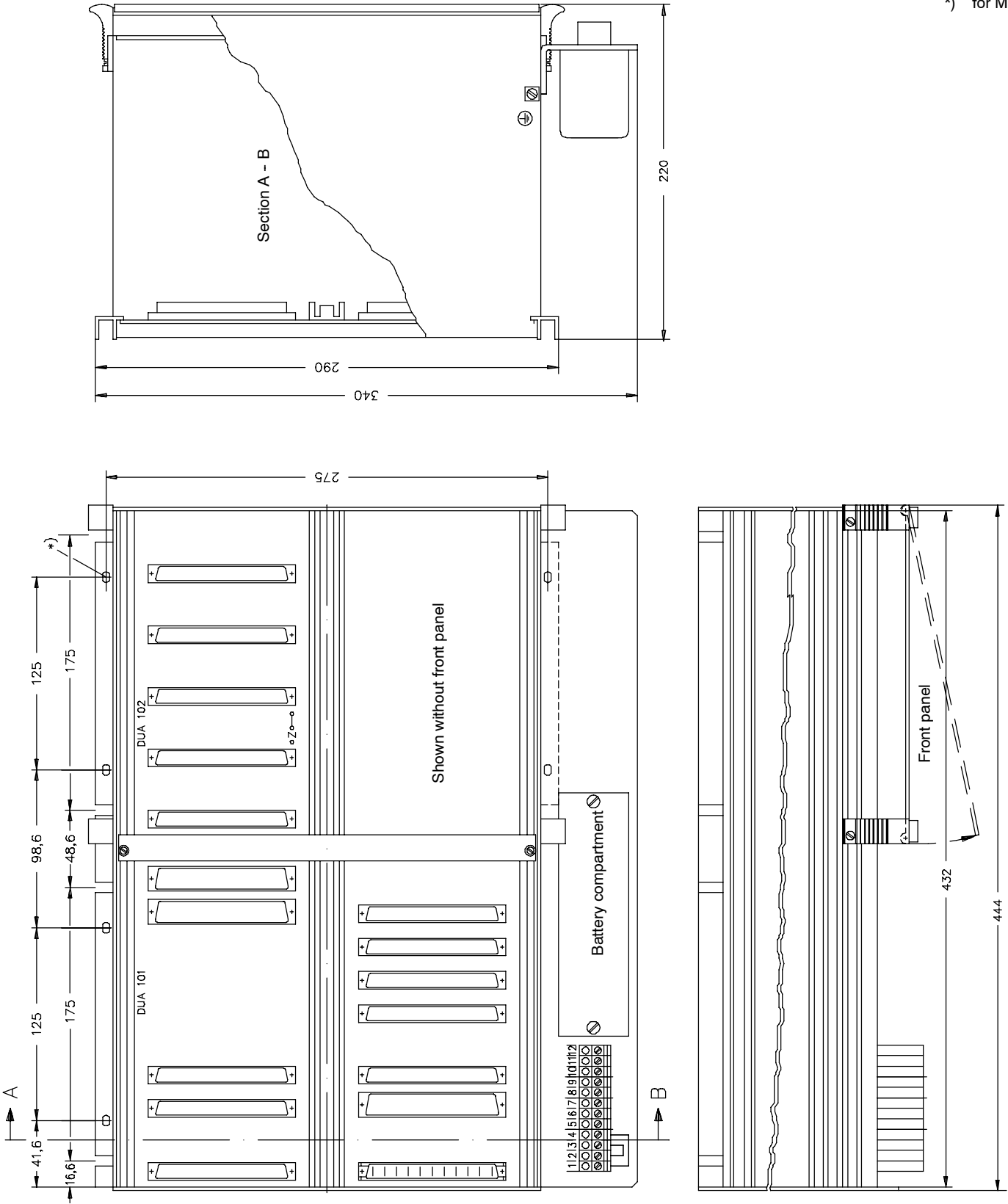


Figure 156 Dimension Drawing of the DTA 101

Mounting Flange for 19" Holders (Grid According to DIN 41 494 and DIN 43 660)

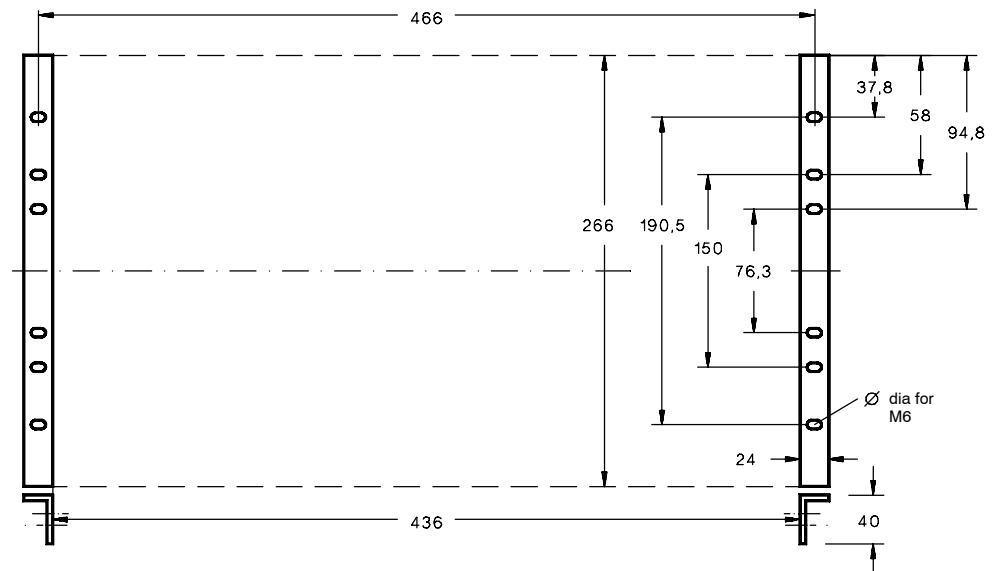
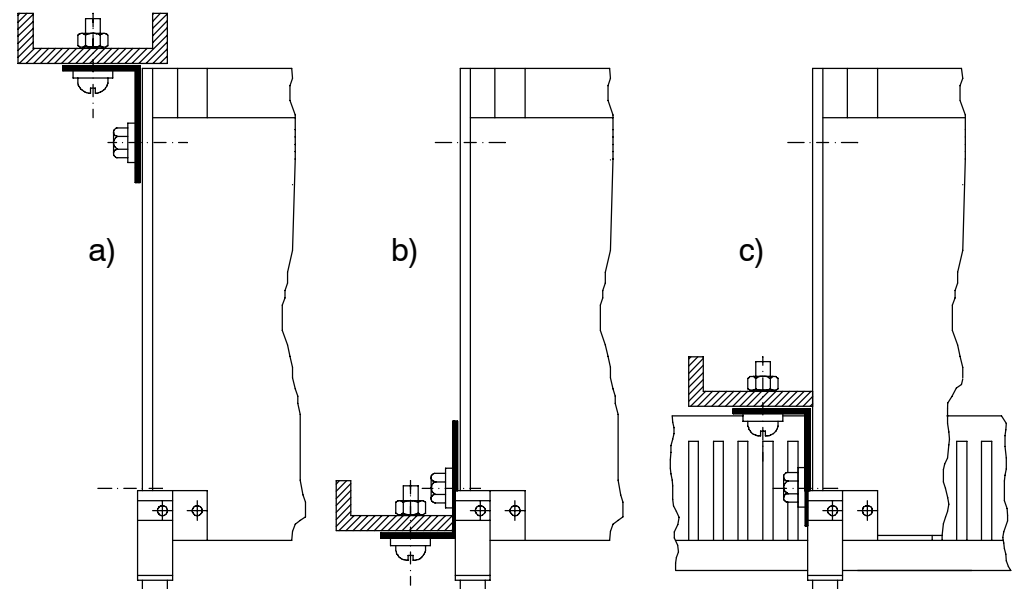


Figure 157 Dimension Drawing of the Mounting Flange for DTA 101

Mounting flange use



- (a) Rack mounting from the rear
- (b) Mounting in 19" structure
- (c) Mounting in 19" structure with a front wiring duct (mounting level is moved back)

Figure 158 Mounting Flange used for the DTA 101

4 Specifications

4.1 Assignment

Product family	Modicon
Device	A500

4.2 Supply Interface

U_{B24}	+16.5 ... 24 ... 41 VDC (DNO 028 data)
I_{B24} max.	< 4.5 ... 3 ... 1.8 A (DNO 028 data)
Reference Potential	M2
Protective Earth	PE
Battery Block	RAM supply, NiCd pack 3.6 V/1.8 Ah
Port	+B, -B (double, see function) the port is separated when the device is delivered, the charging state undefined
Earth Grounding	M5 earthing screws on the side sheet Insulated structure, connection via: 3 Z screws (left-hand half, controller) 1 Z jumper (right-hand half, I/O port)

4.3 Physical Characteristics

Constructional Form	INTERMAS, size: 6/84T
Dimensions	444 x 290 x 220 mm (W x H x D rear) 444 x 340 x 220 mm (W x H x D front)
Weight	4.7 kg

Table 58 Equipment Possibilities of the DTA 101

Slot No.	Width (T)	Module	Connector
01	8	Power supply DNO 028 with PEAB port	(C64F+H11)
09	4	UKA 024, LS / V.24 (for ALU 150, ALU 821 only)	(E48F+C64F)
17	8	Central processing unit ALU 011, ALU 150 or ALU 821	(2 x C64F)
21, 25, 29, 33	4 x 4	PMB node (see Figure 153) SC..., SF 8128/8256, BIK 812, BIK 151, KOS 882 or KOS 152	(C64F)
37	4	UVL 841, if necessary	(E48F)
40	4	Dummy plate with holder	
45	4	Modnet 1/SFB coupling DEA 106 or DEA 156	(C64M)
53, 61, 69, 77	4 x 8	I/O node (front connection) in any combination	(C64F)

Dummy Plates	slots which are not occupied are to be closed with dummy plates (ventilation)
--------------	---

4.4 Type of Port

Internal	Connector, see slots
NiCd Rechargeable Battery	2 x 2-pole connector (separated when the device is delivered)
System Field Bus Cable	Connection within the subrack
YDL 40	BIK 151/812 → DEA 106/156 (front)
Supply / Message	12-pole terminal blocks, for line cross-sections of 0.25 ... 2.5 mm ²

4.5 Environmental Conditions

System Data	see user manual
Safety Type	IP 00
Regulations	VDE 0100, 0110, 0160, part 1 Port means: insulation category C

4.6 Ordering Data

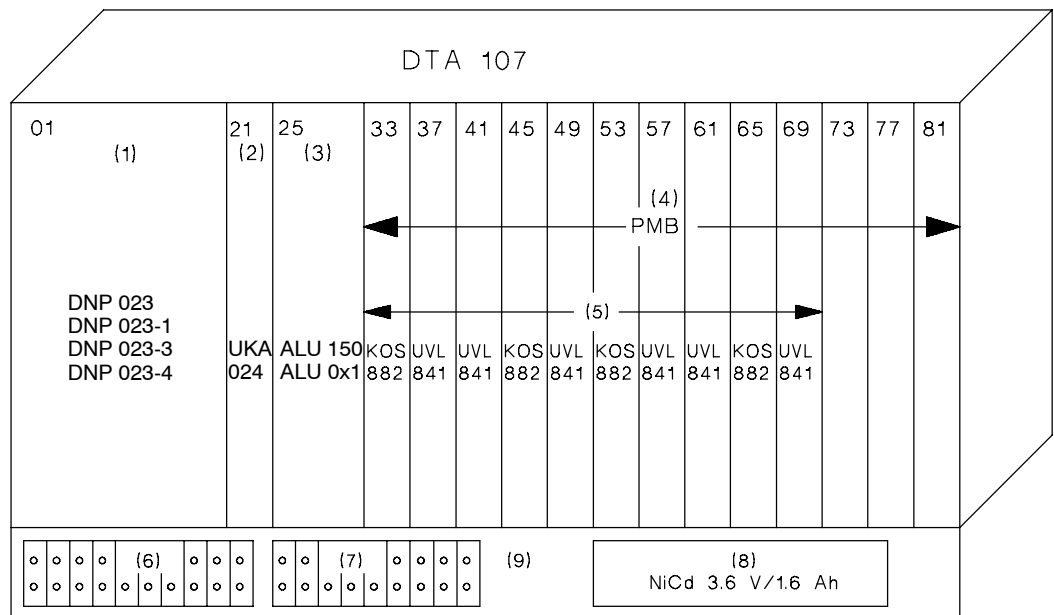
DTA 101 Subrack	424 233 850
YDL 40	424 234 184
(System Field Bus Cable)	
Mounting Flange (x 2)	424 234 113
Dummy Plate 6HE/4T	424 166 824
A3 Form Block	A91M.12 - 234 721

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DTA 107 Subrack Module Description

The DTA 107 subrack with front connection permits a structure of A500 controllers with a maximum of 13 memory and interface modules and process coupling exclusively via Modnet 1/SFB. The DKV 023 cannot be inserted and a PEAB expansion is not possible either.

Various DC and AC power supplies serve the supply. This subrack can also be used for B500-2 systems (in 10 MHz technique, when modified physically).



- | | | |
|--|--|--|
| Standard equipment | (3) Central processing unit | (7) von Versorgungsbaugr abhängiger Anschluß |
| (1) Power supply | (4) Program or communications buffer Port area dependent on the power supply | (8) Akkufach |
| Prewired slots | (5) vorverdrahtete Steckplätze | (9) Anschlußwinkel |
| Rechargeable battery compartments | (6) von Versorgungsbaugruppe unabhängiger Anschlußbereich | |
| (2) Monitoring (for ALU 150 only) | | |
| Port area independent of the power supply Port angle | | |

Figure 159 Front View of the DTA 107

1 General

1.1 Physical Characteristics

The subrack has a width of 19" with an equipment width of 84 T and is suitable for wall mounting and for the integration in 19" holders. Mounting flanges (6HE) which are screwed onto the narrow sides of the subrack are available as accessories for the cabinet integration (see Figure 165).

The wiring printed board carries the connectors for the power supply and controller components including the standard wiring which permits numerous equipment variants (Figure 159). A few switchover jumpers for application variations are accessible in the structure of the power supply.

Supply ports and event outputs lie on screw terminals on the port angle of the subrack. The battery compartment of the backup battery for memory modules is located next door.

The standard equipment is to be taken from Figure 159; the specifications can be found under "Specifications".

The components known for "A500" for firmware and user programs, serial communication, system field bus coupling and monitoring functions can be used as controller modules. The wiring printed board designed in the press-in technique totally covers the rear and is designed so that a rear access is not necessary for setting or service purposes except for the Z screws.

The equipment order shown in Fig. 152 is to be observed when using the KOS 882 communications buffers together with the UVL 841 adaptation module. Certain slots of the subrack carry a standard wiring for 48-pole connectors in the upper structure. This wiring foresees the equipment with max. 4 x KOS 882 and 6 x UVL 841, whereby 2 KOS can be used with 8 interfaces (2 x UVL each) and 2 KOS with 4 interfaces only (1 x UVL each).

Mains and additional supplies as well as wiring to other subracks are carried out via the 29-pole terminal block (see Figure 160). Signals for superior error messages (MRNC, MRC, MRNO), for the synchronization of the power supplies for more complicated systems ($\overline{\text{SYNC}}$, PSEC (FRGM), PSEN0 (FRGA)) and the memory time extension (+VE (PK), -VE (NK)) are also available here. See section 3.1 "Port angle", for the labelling of the terminal block.



Warning DC and AC power supplies do not have a uniform port wiring; changing the wiring in an inadmissible way can lead to the destruction of the relevant power supply if the type is changed.

2 Operating and Indicating Elements

The subrack does not possess any of its own indicating element. The setting of functional jumpers is treated in section 3 "Configuration".

Service Intervention:

The lower edge of the subrack is formed by a mounting angle which carries the supply terminals and a covered battery compartment. The NiCd rechargeable battery required to back up the RAM modules is accessible after opening the cover (snap fastening). The port via one of the two 2-pole connectors is to be carried out during the start-up: The connection is separated when the machine is delivered and the charge status undefined. The label on the front of the subrack informs you about the deadline for changing the battery. You are to make an entry when you start up the machine.

The two connectors for the battery connection which are wired in parallel permit

- a back-up free of interruption when the system is not supplied with voltage while the old (still functioning) battery is replaced by a new charged battery (see the entry of the guarantee date).
- if the system is supplied with energy, the old battery can be replaced by a new battery the charging condition of which is undefined. Changing the battery does not affect the back-up if there is sufficient recharging time available until the next interruption in the supply.

3 Configuration

The following is to be configured for the subrack:

- ❑ Documentation on an A3 form for supply, backup and equipment
- ❑ Wiring depending on the power supply, jumpers
- ❑ System field bus coupling (bit bus)
- ❑ Modifications for B500-2 applications
- ❑ Backup battery for CMOS memory modules

3.1 Port Angle

All the supply voltages, even those necessary to connect a B500-2 secondary subrack, and all the interference event and synchronization signals are guided to the port angle. Figure 160 shows the different terminal assignments for AC and DC supply. Enable wiring, see 3.3.

	Term.	DNP 023 (AC)	DNP 023-1 (DC)	
Port area independent of the power supply (6) in Figure 159)	1		0 V	Secondary voltages
	2		0 V	
	3		0 V	
	4		0 V	
	5		+5 V	
	6		+5 V	
	7		+12 V	
	8		-12 V	
	9	--	L+ 2	only DNP 023-3,4
	10	--	M 2	
	11		MRNC	UKA pilot relay
	12		MRC	
	13		MRNO	
	14		VCK 24	
	15		VCK 0	Explanations s. 3.6
	16		L+ EXT	
	17		M EXT	
Port area dependent of the power supply (7) in Figure 159)	18		0 V	Explanations s. 3.4, 3.9
	19	--	SYNC	
	20	--	PSEC	
	21	--	PSENO	
	22	SYNC	--	Supply
	23	PSEC	+VE	
	24	PSENO	-VE	
	25	+VE	L+	
	26	-VE	L+	
	27	L	M	
	28	N	M	
	29	PE	PE	

V: Wiring for 1 x AC power supply per system: (18 - 23; 24 - 22)
 Delivery state: without jumpers
 Wiring for 1 x DC power supply per system: (18 - 20; 21 - 19)

Figure 160 Terminal Assignment on the Port Angle of the DTA 107

3.2 Supply Wiring

The 220 VAC ($3 \times 1.5 \text{ mm}^2$) supply lines and the +VE / -VE ($2 \times 1.5 \text{ mm}^2$) lines must be laid as shield lines whereby one side of the shield is laid to the earth ground on the terminal block.

If the DTA 107 subrack is to be expanded by slots for PMB nodes (e.g., with DTA 107 without a power supply) when setting up B500-2 systems, the reference potentials of 0 V and +5 V are to be wired with $2 \times 4 \text{ mm}^2$ each. The $\pm 12 \text{ V}$ voltages can be wired simply.

3.3 Supply Monitoring

The enable input ($\overline{\text{SYNC}}$) and the PSEC/PSENO (FRGM/FRGA) switch contact of the enable relay lie on different terminals depending on the power supply used (see Figure 160). The necessary connections for systems with one or several power supplies are to be taken from the descriptions of the power supplies, for systems with one power supply only from the key to Figure 160 as well.

The function of the power supply is blocked without the enable wiring!

3.4 Mains Backup

The standard backup time of the power supply depends on the load and amounts to at least $150 \mu\text{s}$. An additional backup is required for industrial mains with short-term voltage dips. The +VE / -VE (PK, NK) terminals are the connecting points for a back-up capacitor to extend the backup time. The capacitor must be installed outside the subrack. See "3.2 Supply wiring" for the type of wiring.

The following is valid for input voltages $>19\text{V}$ for the time extension:
 $C (+\text{VE}, -\text{VE}) = 2.2 \text{ mF/msec}$

3.5 Occupation of the Subrack

The standard equipment shown in Figure 159 is to be varied according to the task and documented with the A3 form. The necessary entries are made here for the equipment, ordering, spatial requirements, slot no., operating means designation for components and system parts, etc. Field bus couplers and memory modules can be inserted in the PMB area as desired but they should be mounted so that prewired slots remain reserved for KOS/UVL combinations.

3.6 Functional Jumpers in the Structure of the Power Supply

The port interpolation points (partly covered) and functional jumpers shown in Figure 161 are accessible from the front with the power supply disconnected. The Z screws shown here and in Figure 163 are only accessible from the rear of the subrack.

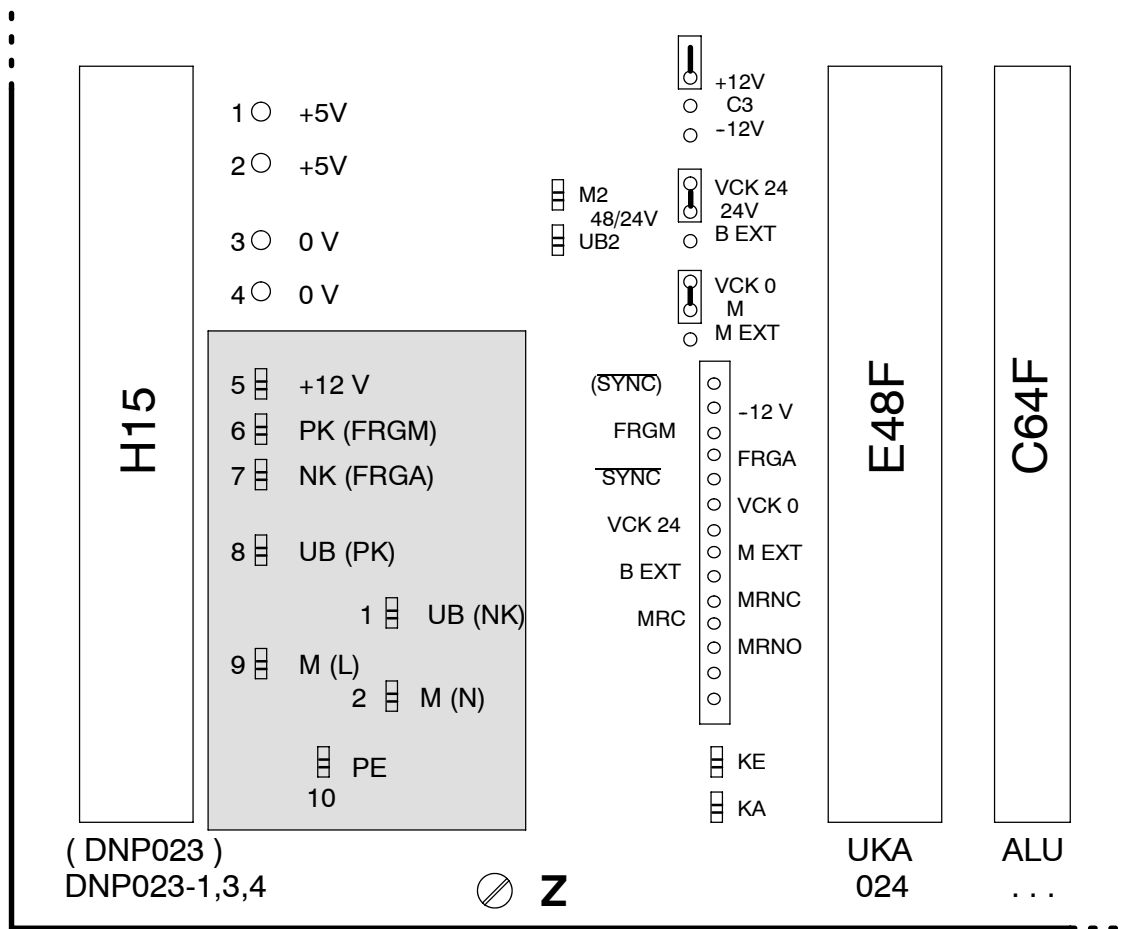


Figure 161 Section of the Wiring Printed Board with the Position of the Functional Jumpers for the DTA 107

3.6.1 Supply of PMB Components

- a) b) The jumper starting at C3 permits the selective supply of PMB components with 2 x +12 V (a) ²⁶⁾ or ±12 V, e.g., for B500-2 (b)

²⁶⁾ The jumper is open when the device is delivered (neither +12 nor -12) since the connector points of A03 are jumpered with C03 for various components (e.g., KOS 882, COP 82) and this can lead to the power supply being shorted with the circuit jumpers in the incorrect position.

3.6.2 Current Loop Supply for UKA and UVL

The internal (VCK 24, VCK 0 (VCK = checked voltage)) and the external ($L+_{ext}$, M_{ext}) supply is wired to the UKA slot. Which of the two circuits is used to supply the current loop interface can be selected on the UKA 024 itself with a jumper.

The selection of the supply circuit is also possible for all UVL together in order to be able to realize an isolated supply for the UKA. If the system is equipped with a DNP 023-3 power supply, the potential-free 24 VDC voltage source also available at the $L+/M2$ terminal block can be wired to VCK 24/VCK 0 or B_{ext}/M_{ext} . The position of the switchover jumpers and their electrical mode of functioning is to be taken from Figure 162.

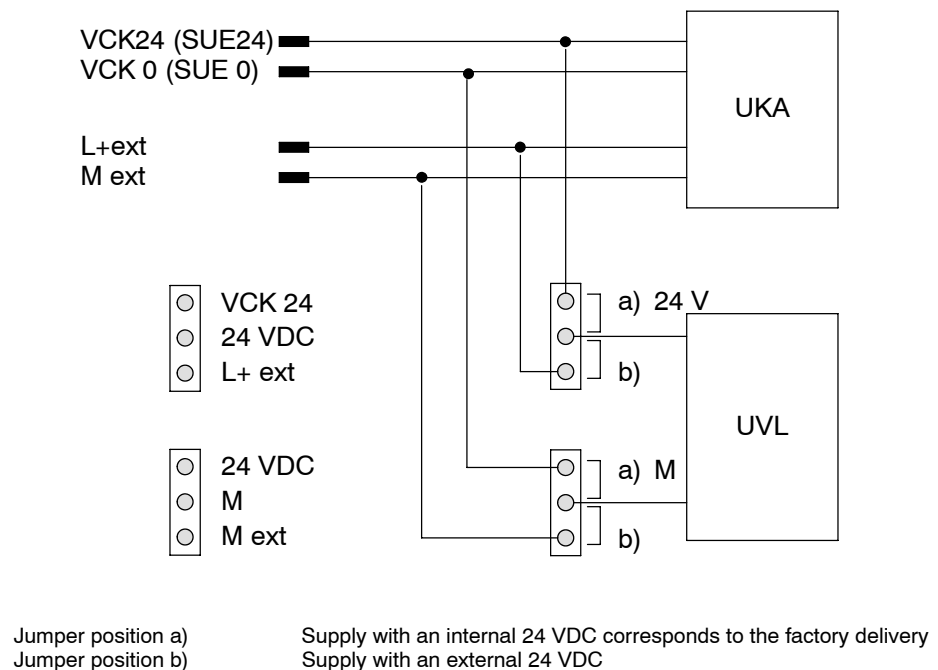


Figure 162 Jumper Position for Voltage Monitoring for the DTA 107

3.6.3 Signal Check Loop

KE ○ The signal check loop is to be connected to the monitored subrack at
KA ○ these interpolation points.

3.7 Error Message

The potential-free changeover contact of the noise pilot relay which is located on the UKA 024 is wired to terminals 11 ... 13 (MR, MM, MA). The contact can be loaded with 24 V / 50 mA to evaluate the message. The following messages confirm the noise pilot relay:

- Undervoltage < 18 VDC
- Access temperature > 70 °C
- Cycle malfunction (Deadman)

3.8 Safety Measures against Overvoltages

If the internal voltage supply of the modules is carried out via a power supply belonging to the system with 24 VDC supply, it is to be guaranteed that no inadmissible overvoltages occur through switching operations of inductive actuators. These overvoltages can lead to the semi-conductor inputs and outputs of the programmable controller being damaged or destroyed.

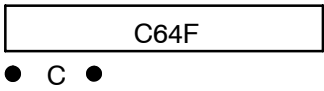

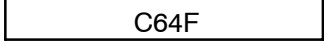
Suitable safety measures (with suppressor diodes) are treated in detail in the user manual in the "Configuration" section. The safety circuits for internal voltages are integrated for power supplies belonging to the system with a 220 VAC supply.

3.9 Z Screws (Central Earthing)

The chassis of each subrack is to be connected to the protective earth conductor for reasons of interference suppression (via the earthing screw on the side sheet) with at least 6 mm².

The internal reference potential of 0 V of the controller is connected to the metal construction of the subrack via 7 "Z screws" which are distributed over the entire wiring printed board (see Figure 163) for reasons of interference suppression. The Z screws are only accessible after removing the rear shield plate (loosening 2 screws attached to each side)
(PE = protective conductor terminal = 0 V = central earthing point, delivery status).

Loosening these 7 screws marked with "Z" is possible (only accessible from the rear) for an earth-free operation. The 0 V potential is then earth-free and can be earthed capacitively if the Z screws are loosened. You should preferably use the following for this:

	ALU	C = 0.1 µF/400 V: Equipment between the C64F connectors designated with UKA and ALU
	UKA	R = 1 MOhm /0.5 W: Equipment between the C64F connectors designated with DNP and UKA.
	DNP	See Figure 163 for the position of the interpolation points.



Caution There is an increased risk of interference with earth-free operation; this is to be taken into consideration with suitable measures, e.g., spatial separation between signal and supply wiring.

3.10 B500-2 Use

The wiring printed board consists of connected part printed boards which realize the prewiring for the standard equipment with KOS 882 and UVL 841 and can be separated to the advantage of other PMB nodes. These connected part printed boards are above the PMB area.

Part boards are to be dismantled depending on the desired division onto PMB and PMB' so that the VPU-MEA bus (DUM 851) can be mounted there. The -12 V required for B500-2 can be taken from slot 0227 of the wiring board via a 2.8 mm flat-pin connector.

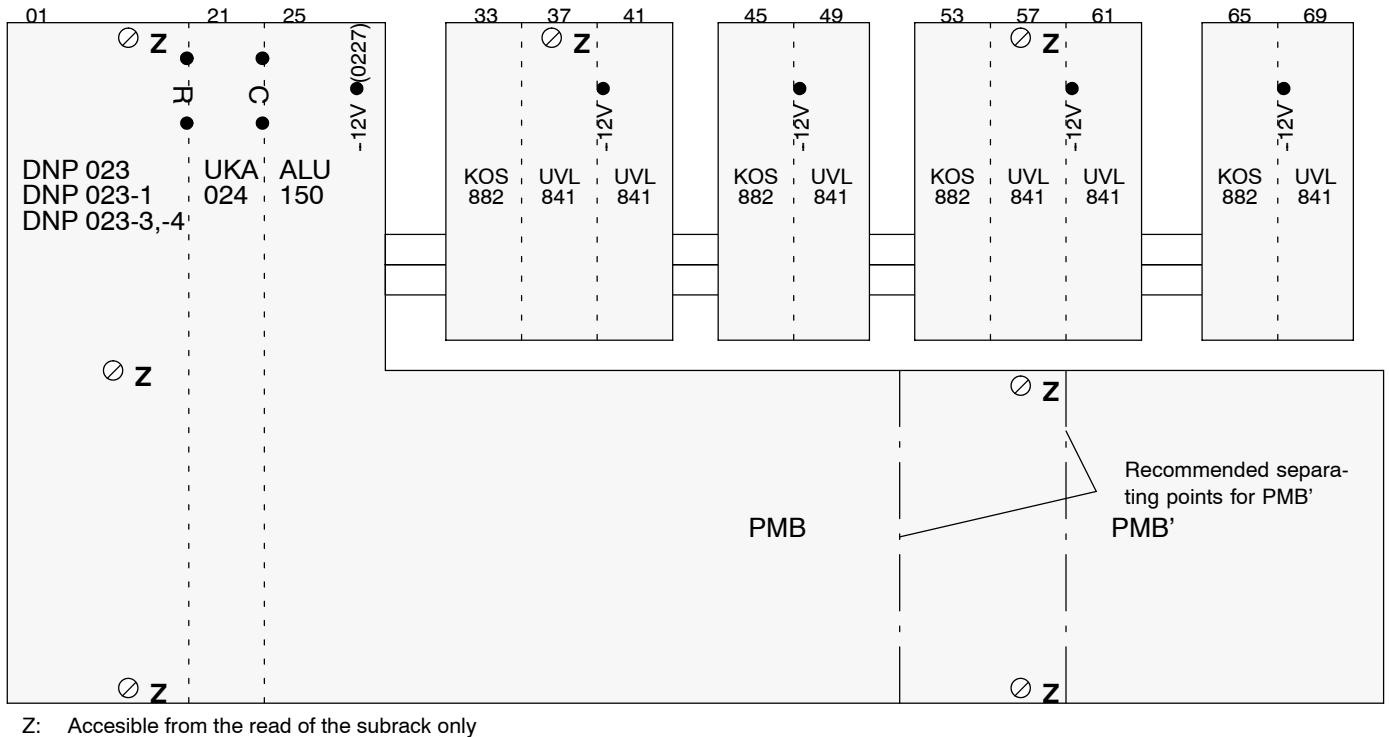


Figure 163 Wiring Printed Board of the DTA 107

The required work is to be carried out according to the drawing no. 7328 M - 235 200.00. The mechanical separation of signal and control lines between PMB and PMB' is described here. The desired division into memory slots for PMB and PMB' must already be given with the order by the configurator, whereby the separating point on the PMB board is preferably to be provided between the following pitches for a optimum slot utilization:

0849 - 0853
or 0857 - 0861

These recommended separating points offer two PMB' areas which have different sizes and also take into account the fact that the DUM 851 backplane also requires 4 pitches for RC connections which penetrate the PMB area. However, this slot (49 or 57) can be used by a memory module which is 4 pitches wide.

This work can only be carried out by the manufacturer (Seligenstadt factory) as part of the order.

3.11 Mounting Flange for 19" Holders

(Grids according to DIN 41 494 and DIN 43 660)

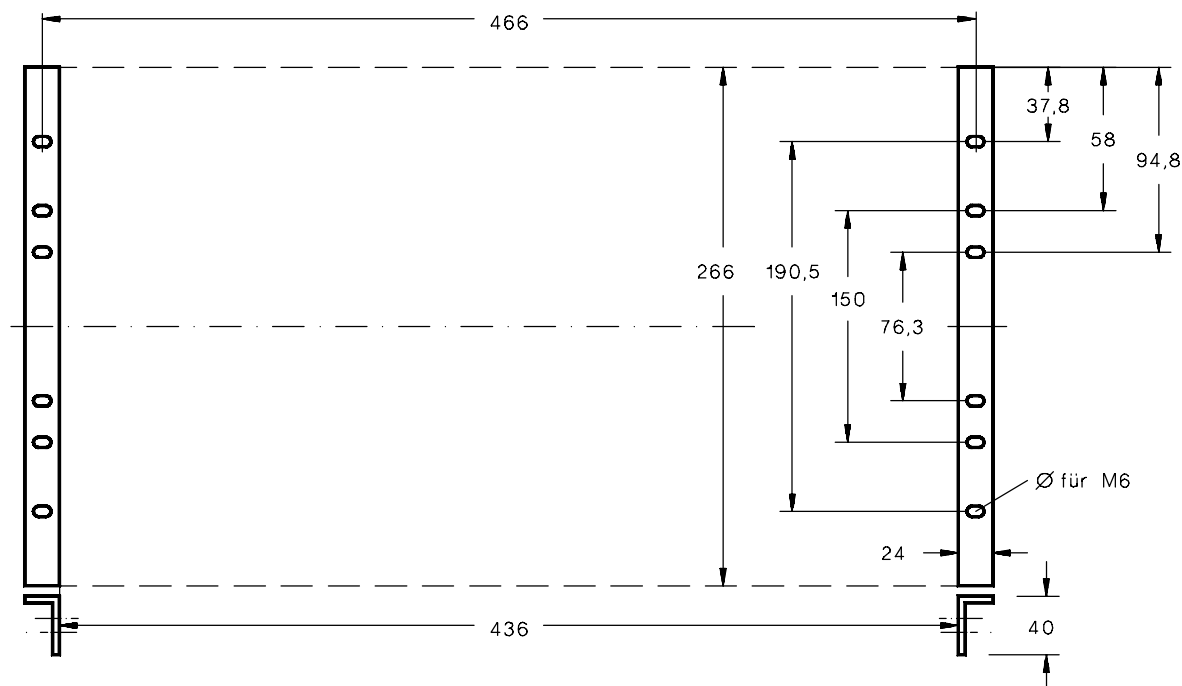


Figure 164 Dimension Drawing of the Mounting Flange for DTA 107

Mounting Flange Use

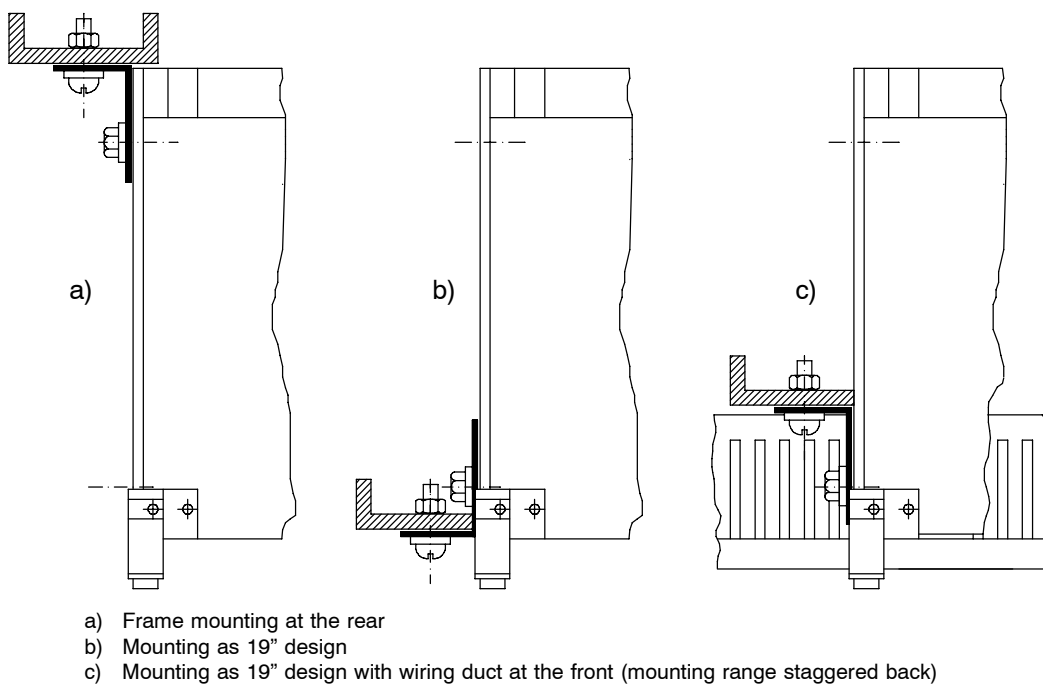


Figure 165 Mounting Flange Use for the DTA 107

3.12 Subrack Dimension Drawing

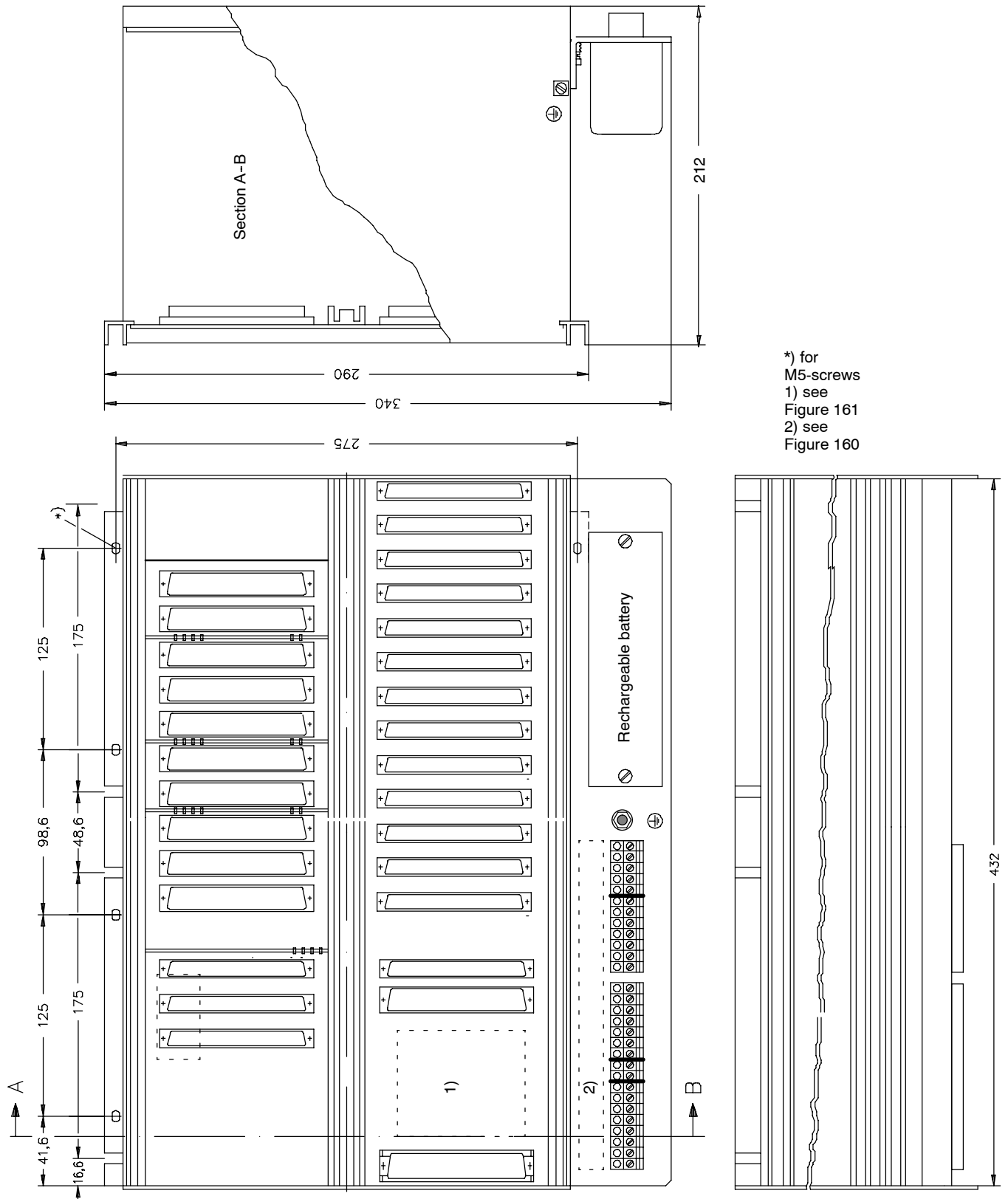


Figure 166 Dimension Drawing: DTA 107

3.13 Supply of CMOS Memory Modules

When extending the PMB structure by a complete subrack only 1 subrack may be equipped with a CMOS backup battery which then supplies both subracks. The connection is carried out from battery slot to battery slot with a 2-wired line which is equipped with 2-pole ELCO connectors on both sides.

The following order is to be observed for changing the battery when the system is not supplied:

1. Connect the new rechargeable battery in the empty rechargeable battery compartment.
2. Disconnect and remove the old rechargeable battery in the second rechargeable battery compartment.

3.14 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings or circuit elements are already entered. These form sheets are

- included in the form block for conventional processing
(see ordering data)
- included in the A500 data bank for Ruplan processing (Technical Sales Office version)
(in preparation)

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500

4.2 Supply interface

Supply	24 VDC	Supply interfaces	DNP 023-1, DNP 023-3
	48 VDC	Supply interface	DNP 023-4
	220 VAC	Supply interface	DNP 023
Protective Earth		PE	
Assignment of the			
Terminal Block		see 3.1	
Battery Block		RAM supply RAM, NiCd pack 3.6 V/1.8 Ah	
Port		+B, -B (double, see function)	
Earth Grounding		M4 earthing screws on the side sheet	
0 V → Earth		Isolated structure, jumpered via 7 "Z screws", see also 3.9	

4.3 Physical Characteristics

Constructional Form	INTERMAS, size 6/84T			
Dimensions	W	x	H	x D
Rear	444	x	290	x 212 mm
Front with Port	444	x	340	x 212 mm
Angle				
Weight	5.0 kg			

Table 59 Equipment Possibilities for DTA 107

Slot No.	Width (T)	Module	Connector
-01	20	Power supplies	(C64F+H15)
-21	4	UKA 024 (for ALU 150 only)	(E48F+C64F)
-25	8	Central processing unit ALU 0x1 or ALU 150	(2 x C64F)
-33 ... -81	13 x 4	PMB node (see Figure 159)	(13 x C64F)
or		reserved equipment on the slots	
-33, -37, -41	3 x 4	KOS 882 + UVL 841 + UVL 841	(+3 x E48F)
-45, -49	2 x 4	KOS 882 + UVL 841	(+2 x E48F)
-53, -57, -61	3 x 4	KOS 882 + UVL 841 + UVL 841	(+3 x E48F)
-65, -69	2 x 4	KOS 882 + UVL 841	(+2 x E48F)
-73, -77, -81	3 x 4	any PMB nodes	

Dummy Plates

slots which are not occupied are to be closed with dummy plates (ventilation)

4.4 Type of Port

Internal	Connector, see "Physical structure"
NiCd Rechargeable Battery	2 x 2-pole Elco connector
Terminal Block	for line cross-sections of 0.25 ... 2.5 mm ²
AC Supply	3 x 1.5 mm ²
DC Supply	2 x 2 x 2.5 mm ²
Back-Up Capacitor	2 x 1.5 mm ²

4.5 Environmental Conditions

System Data	see user manual
Safety Type	IP 00
Regulations	VDE 0100, 0110, 0160 part 1
	Port means insulating category C

4.6 Ordering Data of the Subrack

DTA 107	424 235 200
Mounting Flange (x2)	424 234 113
Dummy Plate: 6HE/4T	424 166 824
A3 Form Block	A91M.12 - 234 721
A500 Ruplan Data Bank	in preparation

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KOS 152

Modnet 1N Interface

Module Description

The Modnet 1N interface KOS 152 provides 2 serial interfaces (RS 232C or current loop). These interfaces can be operated as communications or Tesy ports.

The following options are possible dependent on the equipped firmware:

- Modnet 1N networks or Tesy together with standard firmware
- Modnet 1N networks or Modnet 1F networks together with firmware CFW 502 (optional). This version is a cost-effective communication interface for telecontrol tasks.

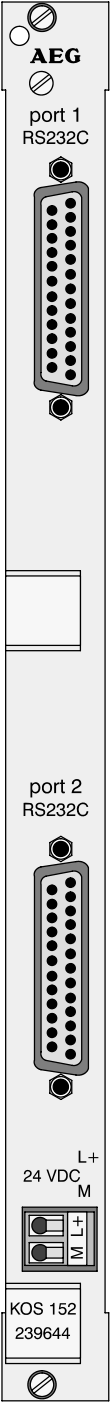
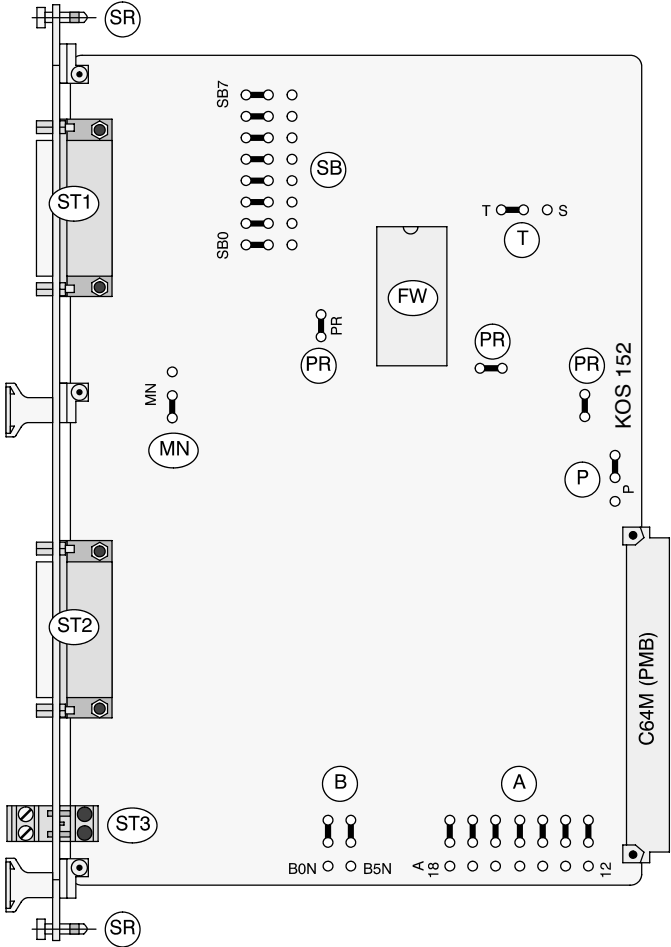


Figure 167 Front View of KOS 152



- (A) Address Jumpers
- (B) 2 Status Bit
- (FW) EPROM type 27256 (firmware)
- (MN) M5 Signal
- (P) Interrupt Changeover
- (PR) Test Field Jumpers
- (SB) Status Byte
- (SR) Screws for Earthing Metal Shield Parts
- (ST1) Serial Interface 1 (SEA1), Connection 24-pole
- (ST2) Serial Interface 2 (SEA2), Connection 24-pole
- (ST3) Screw/Plug-in Terminal 9-pole Supply current loop
- (T) Changeover Testy <=> Networking

Figure 168 Survey of Configuration the Elements on KOS 152

1 General

The Modnet 1N interface KOS 152 provides 2 serial interfaces (RS 232C or current loop). Via an efficient, quick memory with a capacitance of 4 KByte a 16 bit wide data communication to each ALU is possible.

1.1 Mechanical Structure

The module has a double European format with a width of 4T. A standardized (DIN 66 020) 25-pole connector (socket) is provided in the front panel for each of the two RS 232C interfaces to peripherals.

An EPROM element type 27256, with 32 KByte memory volume is available as firmware. The accessibility is limited in each case to 16 KByte. Via the plug jumpers there an alternative access to the "upper" or "lower" 16 KByte (Modnet 1N or Tesy) is permitted.

1.2 Mode of Functioning

The module contains an efficient, quick communications memory for 16 bit wide data communication to each of the ALU nnn.

The firmware required for Tesy and Modnet 1N star and bus networking is contained in the EPROM referred to. The selection of Tesy or SEAB networking activation takes place via a plug jumper. With a KOS 152 these two are not possible simultaneously.

Alternatively the module can be equipped with the firmware CF 502 that alternatively either permits Modnet 1N or Modnet 1F networks. Via plug jumper you can either activate the Modnet 1N or the Modnet 1F network ("upper" or "lower" 16 Kbytes of the EPROM), never both at the same time.

The transmission rate in the RS 232C (V.24) is individually for each of the two interfaces adjustable in the range of 50 Bd ... 19 200 Bd with current loop from 50 Bd to 9600 Bd. The adjustment is done via the respective software. For both interfaces a potential separating signal conversion of RS 232C/V.28 standard to 20 mA (40 mA) current loop on the module is available.

The integrated ACIA units have in- and outputs secured against short circuiting.

Two programmable time pulses each control one interrupt. An interrupt of PMB, one to the PMB, facilitates interrupt control messages.

2 status bits, 1 status byte (bits adjustable individually via jumpers on the module) and the states of the two interrupt markers can be queried via particular addresses of the central processor via the internal data bus.

The wire break signal state of the V.24 can be jumped for M5 signals in both valency modes. According to DIN 66 020, the "D"-signals switch on with the negative input level the ON state, all other signals such as "M" and "S" the OFF state.

2 Operation and Display

The module contains no operational or display elements.

3 Configuration

For the module the following are to be configured:

- ☐ fixing the address area on the PMB
- ☐ Networking or Tesy
- ☐ relaying for desired functions (A3 form sheet)
- ☐ evaluating the M5 signal
- ☐ RS 232C or current loop
- ☐ user software
- ☐ transmission rate

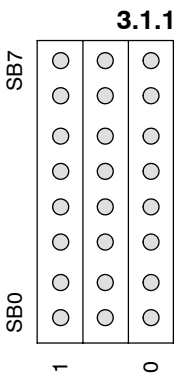


Warning The jumpers marked with PR may not be opened/alterd. They serve exclusively for testing purposes.

3.1 Jumpers

The KOS 152 can be used for various tasks. Depending on whether it is used for Tesy or networking capabilities, different jumper settings are required.

Now some general information concerning jumpers is given. How they have to be set for networking and Tesy will be explained in chapter 3.3 and chapter 3.4.



Status Byte (SB0 - SB7)

SB0 ... SB7 Jumper between middle and right row: valence "0"
 Jumper between middle and left row: valence "1"

These jumper settings can be read via address F and I/O read to the data bit 0 to 7.

- 3.1.2 **Changeover Tesy ↔ SEAB Networking**
 T/S changeover to program Tesy or SEAB networking
 ○ ○

- 3.1.3 **Relay Signal M5**
 ○ If the M5 signal is "On" when wire break occurs, the jumper must not be plugged in on the labelled side, in reverse case on the MN labelled side. For current loop operation the jumper **must** be plugged in on the unlabelled side.
 MN ○

- 3.1.4 **Interrupt P**
 The interrupt to the PMB can alternatively be switched to the MSPFN (parity error) or to the MPARN (address).

- Jumper between middle and bottom: interrupt is switched to MSPFN
 ○ Jumper between top and middle: interrupt is switched to MPARN
 ○ No jumper: no interrupt

- 3.1.5 **Status Bit (B0N, B5N)**
 These jumper settings can be read via address I and I/O to data bit 0 and data bit 5.

- ○ B0, B5 Jumper between middle and bottom: valence "0"
 ○ ○ Jumper between top and middle: valence "1"
 B0N ○ ○ B5N
 On data bit 6 the interrupt memory state FF-CPU, i.e. interrupt of the CPU can be read.
 On data bit 7 the interrupt memory state FF-PMB, i.e. interrupt of the PMB can be read.

3.2 Addressing

3.2.1 General Addressing

The module occupies a memory space of 8 Kbytes. The configuration must define at which address this memory begins within the entire memory. From the two tables following, the general addressing can be derived.

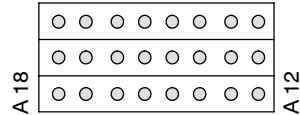


Table 60 Setting the Segment Addresses for KOS 152

Segment	32k Block Address (hex)	A18	A17	A16	A15	A14
1	00000 - 07FFF	0	0	0	0	0
2	08000 - 0FFFF	0	0	0	0	1
3	10000 - 17FFF	0	0	0	1	0
4	18000 - 1FFFF	0	0	0	1	1
5	20000 - 27FFF	0	0	1	0	0
6	28000 - 2FFFF	0	0	1	0	1
7	30000 - 37FFF	0	0	1	1	0
8	38000 - 3FFFF	0	0	1	1	1
9	40000 - 47FFF	0	1	0	0	0
10	48000 - 4FFFF	0	1	0	0	1
11	50000 - 57FFF	0	1	0	1	0
12	58000 - 5FFFF	0	1	0	1	1
13	60000 - 6FFFF	0	1	1	0	0
14	68000 - 6FFFF	0	1	1	0	1
15	70000 - 77FFF	0	1	1	1	0
16	78000 - 7FFFF	0	1	1	1	1
17	80000 - 87FFF	1	0	0	0	0
18	88000 - 8FFFF	1	0	0	0	1
19	90000 - 97FFF	1	0	0	1	0
20	98000 - 9FFFF	1	0	0	1	1
21	A0000 - A7FFF	1	0	1	0	0
22	A8000 - AFFFF	1	0	1	0	1
23	B0000 - B7FFF	1	0	1	1	0
24	B8000 - BFFFF	1	0	1	1	1
25	C0000 - C7FFF	1	1	0	0	0
26	C8000 - CFFFF	1	1	0	0	1
27	D0000 - D7FFF	1	1	0	1	0
28	D8000 - DFFFF	1	1	0	1	1
29	E0000 - E7FFF	1	1	1	0	0
30	E8000 - EFFFF	1	1	1	0	1
31	F0000 - F7FFF	1	1	1	1	0
32	F8000 - FFFFF	1	1	1	1	1

Table 61 Setting the Module Addresses for KOS 152

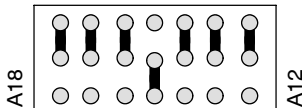
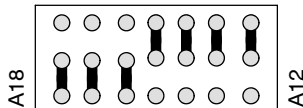
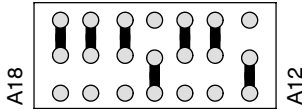
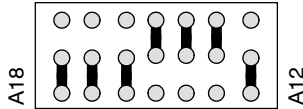
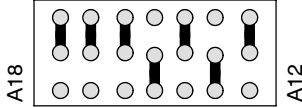
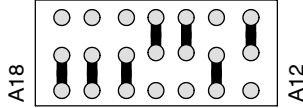
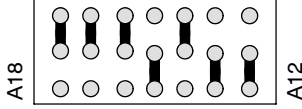
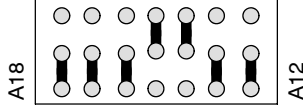
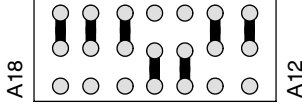
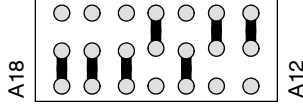
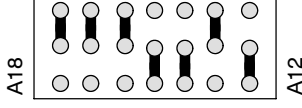
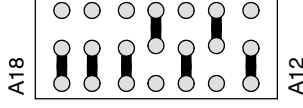
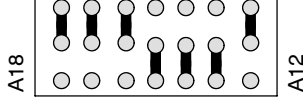
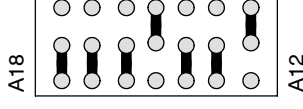
16K block	Address (HEX)	A13	A12
1	0000 - 1FFF	0	0
2	2000 - 3FFF	0	1
3	4000 - 5FFF	1	0
4	6000 - 7FFF	1	1

The PMB is occupied with the first 4 K addresses of the 8 K card area via the dual port. When the interrupt is not activated from or to the KOS the upper 4 K on the PMB are free to be used.

3.2.2 Addressing the KOS 152 for Installation in A350/A500

When using the KOS 152 the segments 3 and 4 (with segment 4 only the 1st - 3rd 8K-block) are available (exception: in connection with the ALU 821 segments 29 and 30 are available, with segment 30 only the 1st - 3rd 8K-block). When using the A350, a maximum of two KOS 152 may be operated. These should preferably be addressed in segment 3, 1st and 2nd 8K-block. In the A500 a maximum of seven KOS may be operated.

Table 62 Addressing the KOS 152 for Installation in A350/A500

KOS No.	8 k Block	Address ALU 0x1, ALU 150 Segment	Jumper Setting	Address for ALU 821 Segment	Jumper Setting
1	1	3		29	
2	2	3		29	
3	3	3		29	
4	4	3		29	
5	1	4		30	
6	2	4		30	
7	3	4		30	

3.3 Settings for Networking

Optionally the following types of firmware are available:

- ☐ Standard firmware for Modnet 1N networks or Tesy or optionally
- ☐ Firmware CFW 502 for Modnet 1N Networks or Modnet 1F Networks

Possibilities of Installation with Modnet 1N

SEA1 can be used as: bus-master, bus-slave, star-master, star-slave
SEA2 can be used as: bus-master, star-master, star-slave

Possibilities of Installation with Modnet 1F

SEA1/SEA2 can be used as: bus-master

The bus and star procedure can be mixed (e.g. SEA1 = star-slave, SEA2 = bus-master). In this case it applies that for mixed operation the baudrate of the bus procedure is a maximum of 9600 Bd, and that of the star procedure a maximum of 19200 Bd. The setting is attained via software (see user manual on system networking).

3.3.1 Status Byte (SB0 - SB7)

Is not evaluated for Tesy.

3.3.2 Changeover Tesy ↔ Modnet 1N (with standard firmware)

Modnet 1N is activated



3.3.3 Changeover Modnet 1N ↔ Modnet 1F (with optional firmware CFW 502)

The firmware CFW 502 will be exchanged for the standard firmware when networking procedures occur with optionally 1F or 1N messages. The Type of message (Modnet 1N / Modnet 1F) is selected as follows:

Modnet 1N is activated



Modnet 1F is activated



3.3.4 Relay Signal M5

On the standard design the M5 signal is not simulated (adjacent jumper setting). The signal must then be produced by the connected device. If the signal is missing, then the error marker AF is set on the Dolog unit TEEI. This makes it possible to determine whether a device is connected.



If the signal is not to be evaluated, then the adjacent jumper setting is to be selected. For current loop operation the jumper on the unlabelled side must be plugged in.



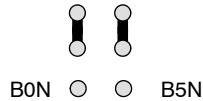
3.3.5 Interrupt P

Place the jumper in this position.

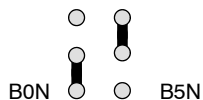


3.3.6 Status Bit (B0N, B5N)

B0N defines the waiting time t_{ws} . If there is networking between two KOS, then the represented jumper position is always to be selected. B5N has no meaning.



For this jumper position, $t_{ws} = 0.8$ s applies. In this setting the networking to an alien system using star networking is possible depending on the type. B5N has no meaning.



The following data apply here (see user manual on system communication):

Alien system is master
 permissible transmission rate: > 75 ... 19200 Bd
 tvn (master) > 0.8 s

3.3.7 Addressing

See chapter 3.2.2

3.4 Settings for Tesy

The standard firmware (Modnet 1N/Tesy) is required.

The transmission rate is separately defined by the software for each interface. It is adjustable within the range from 50 ... 19200 Bd (see Tesy handbook).

3.4.1 Status Byte (SB0 - SB7)

Is not evaluated.

3.4.2 Changeover Tesy ↔ Modnet 1N Networking

Tesy is activated



3.4.3 Relay Signal M5

On the standard design the M5 signal is not simulated (adjacent jumper setting). The signal must then be produced by the connected device. If the signal is missing, the trace can be recognized with the Bsdol function. It makes it possible to determine whether a device is connected or whether there is a break in the cable.



If the signal is not to be evaluated, the adjacent jumper setting is to be selected. For current loop operation, the jumper on the unlabelled side **must** be plugged in.



3.4.4 Interrupt P

Place the jumper in this position.



3.4.5 Status Bits (B0N, B5N)

Are not evaluated for Tesy.

3.4.6 Addressing

See chapter 3.2.2

3.5 Current Loop Operation

The choice of whether RS 232C or current loop operation should take place occurs via the corresponding connection cable.

For operating as an active 20 mA current loop interface, the 24 VDC must be fed to the screw plug terminals UB24 and M2. For passive current loop operation 40 mA are also permissible (current loop is supplied by the "opposite part"). The 24 VDC supply is then not necessary.

3.5.1 Connection Example of an Active Current Loop Interface

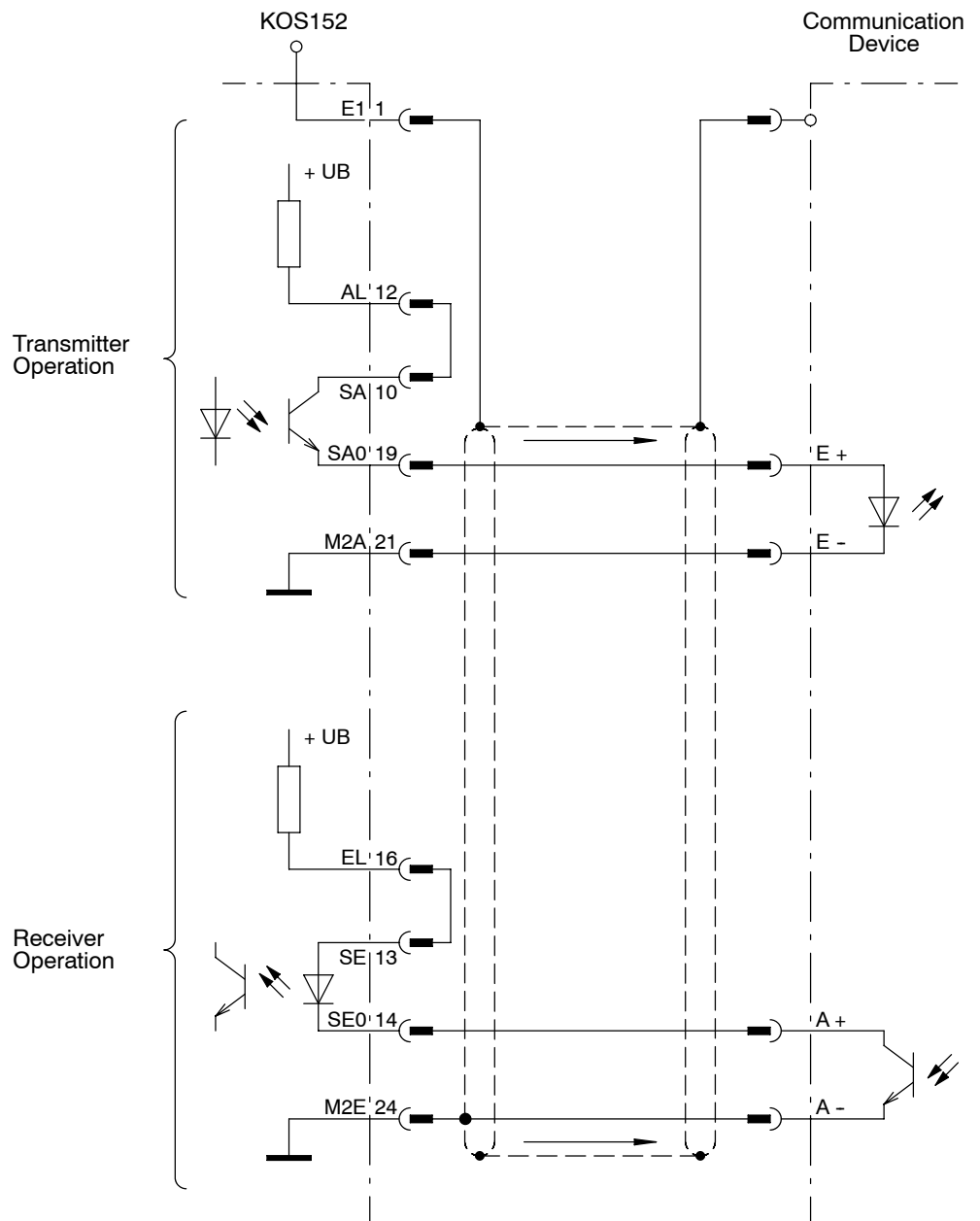
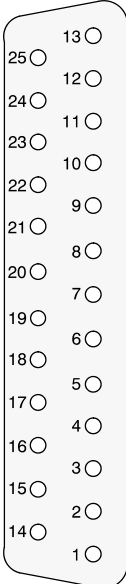


Figure 169

3.6 Connector Pin Assignment of the Serial Interfaces

Table 63 Connector Pin Assignment of the Serial Interfaces (KOS 152)

	SEA1 / SEA2 RS 232C (V.24)			Current Loop
	1	E1	protective earth	protective earth
	2	D1	transmitted data	
	3	D2	received data	
	4	S2	request to send	
	7	E2	signal ground	
	8	M5	clear to send	
	10	SA		serial output (transmitter +)
	12	AL		current loop source output (24 V/20 mA)
	13	SE		serial input (receiver +)
	14	SE0		serial input (reference potential, receiver -)
	16	EL		current loop source input (24 V/20 mA)
	19	SA0		serial output (reference potential, sender -)
	21	M2A		current loop reference potential output
	24	M2E		current loop reference potential input

3.7 Connection Cable

YDL 8	1 to 1 connection to the cabinet connection unit or connection board (only on the cabinet construction)
YDL 14.1	for RS 232C networking
YDL 10.1/YDL 10.1L	for current loop networking to another device (e.g. A350, A500, B500, ...)



Caution If you use the cables YDL 10.1 or YDL 10.1L, you have to unplug the connections 7 → 21 and 7 → 24.

3.8 Ventilation

If the KOS 152 is to be operated without ventilators, i.e. with free convection cooling, then it must be ensured that below and above the module there is sufficient free space left for an air current to flow.

3.9 Interference Suppression Measures (EMC)

To eliminate interference currents via the cable screen, cable plugs and the module handles are to be screwed firmly to the magazine.

To lower the sensitivity to interference on current loop operation, it is recommended that the external voltage is filtered through. For this the mains filter type Eichhoff F11.037/034 may be used (interference eliminator filter 2 A/250 VAC, AEG E-No. 424-084 047). The supply voltage is to be set through two poles. The framing connection of the filter casing is to be carried out with a low voltage.

3.10 Documentation

An A3 form sheet with explanations is available for the system documentation, showing which type and E-No. of the module's firmware is set used as well as the operating conditions of jumpers and switches. These form sheets are:

- part of the form pad and intended for conventional processing (see ordering details)
- part of the Ruplan processing database (under development) and intended for Ruplan processing (technical sales office version)

4 Specifications

4.1 Allocation

System	A350, A500
Slot	primary subrack, PMB area

4.2 Supply Interface

External	
(only for Current Loop)	+24 V/100 mA typical (150 mA max.)
Reference Potential	0 V
Internal (PMB)	+5 V/1.0 A typical (1.5 A max.)
	+12 V/20 mA typical (30 mA max.)

4.3 Serial Interfaces

V.24/V.28	Interfaces according to DIN 66 020 max. 19200 Bd
current Loop	Max. 9600 Bd

Input

0-Signal	SE, SE0
1-Signal	0 ... 2 mA
	15 ... 50 mA

Output

0-Signal	SA, SA0
1-Signal	≤ 2 mA (no load voltage ≤ 60 V)
	≤ 50 mA (voltage drop ≤ 5 V)

4.4 Processor

Type	Intel 8085 A
------	--------------

4.5 Memory	
Communications Memory	RAM 8K x 4 bit (NMOS type 2148)
Firmware	2 x 16 KByte (1 EPROM type 27256) on the plug-in terminal
Factory Supplied	Assembled with firmware Modnet 1N / Tesy
Optional	firmware CFW 502 for Modnet 1N / Modnet 1F
4.6 Mechanical Structure	
Module	Double European format according to DIN 41 496,
Format	6/4T
Mass (Weight)	350 g
4.7 Connection	
PMB	Plug connector C64M according to DIN 41 612
Peripherals	2 x (D25-socket) for RS 232C / current loop
	2-pole front connection for peripheral voltage 24 VDC
4.8 Environmental Conditions	
System Data	see user manual A350 or A500, chapter 4
Power Dissipation	7 W typical
4.9 Ordering Details	
Module KOS 152	424 239 644
Firmware CFW 502	424 247 164
A3 Form Pad	A91M.12-234 785

Specifications subject to change without notice.

KOS 882

Communication Processor

Module Description

The KOS 882 communication processor is an intelligent PMB node. A data link (which is 16 bits wide) to the central processing unit of the A500 programmable controller is given via a high-performance, fast communications buffer (waitstate-free = without a wait state for the node) with a capacity of 4 kbyte.

2 (can be retrofitted to 8) serial interfaces (RS 232 C) with different transmission rates create the connection to the periphery. See the "Mode of functioning" for further functions.

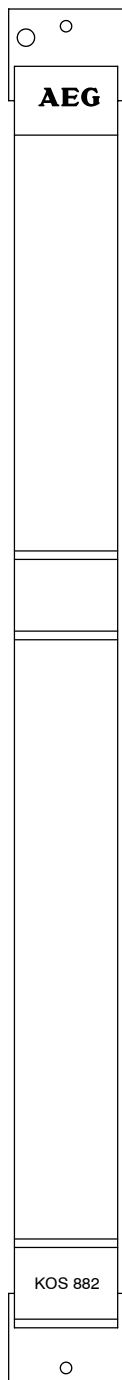
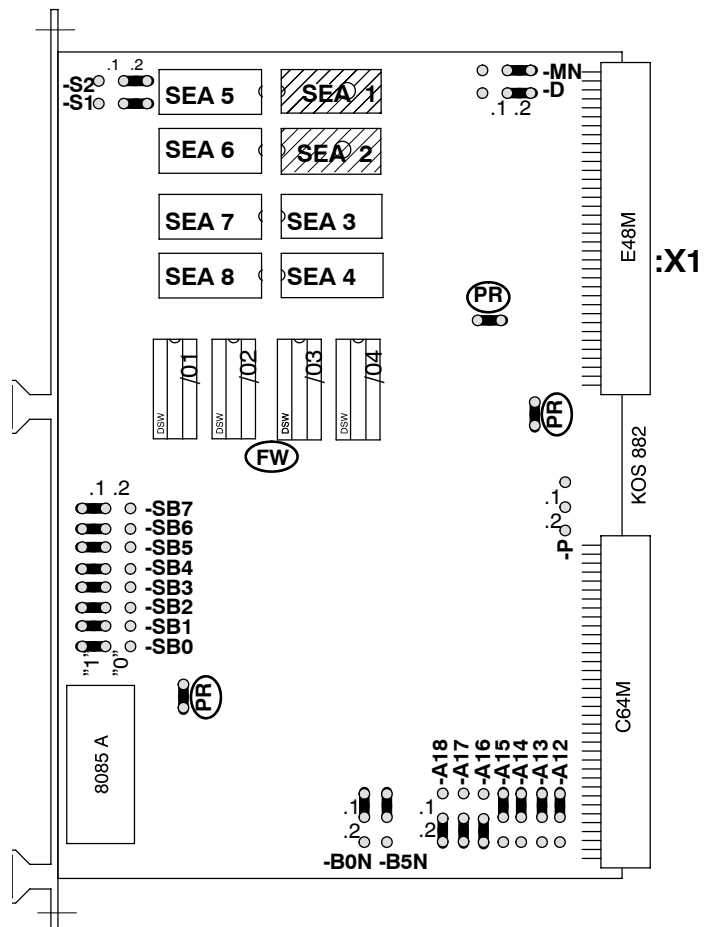


Figure 170 Front View of the KOS 882



- Slots 1 ... 2: interface elements soldered in for SEA1 and SEA2
 Slots 3 ... 8: UART interface elements can be retrofitted for SEA3 ... SEA8
 PR: test field jumpers; do not alter them!

Figure 171 Survey of the Configuration Elements on the KOS 882

1 General

1.1 Physical Characteristics

The module has a double Europe format with a width of 4T and rear contacting for peripheral signals (E48M, top) and a PMB port (C64M, bottom) and can therefore only be inserted in the PMB area of the subrack. Of the 8 possible interfaces, 2 are permanently equipped (soldered in), 6 interfaces can be retrofitted.

A maximum of 4 EPROM elements of the 2732 type can be inserted as the program memory. They produce a memory volume of 16 kbytes. These slots can also be equipped with firmware:

- ☐ Star network
- ☐ Bus networking
- ☐ TESI

A mixed equipment for the use of the maximum number of available interfaces is not possible.

1.2 Mode of Functioning

This module includes a high-performance, fast communications buffer for a data link to the ALU 821 which is 16 bits wide. The 8085 microprocessor is used as the processor type. The networking procedure (firmware) is included in the mentioned EPROMs.

The **serial V.24 interfaces** can be set to a total of 4 different transmission speeds from 50 ... 19 200 bd. 2 of the interfaces can also be operated externally with the clock. The integrated ACIA blocks are controlled in the scan method by the central processor and have short-circuit-proof inputs and outputs. The I/O addresses come from a table. Control bits are written and read with $A_0 = 0$; data are addressed with $A_0 = 1$.

2 programmable time clocks control one interrupt each. 2 interrupts, one from the PMB, one from the PMB, permit interrupt-controlled messages.

2 status bits, 1 status byte (the bits can be set individually on the block) and the statuses of the two interrupt markers can be prompted via the internal data bus (not used with A500 with the exception of the B0N status bit, see configuration) via certain addresses of the central processor (internal μP is the 8085).

The open-circuit signal position for V.24 with ± 12 V can be jumpered in both valency types for the M5 and D2 signals. The "B" signals switch the ON status for a negative input level in accordance with DIN 66 020, all other signals, such as "M", "S" and "T" the OFF status.

The OFF status of the D2 line (receiving datum) is pre-given by the jumper to DN (next to D) **if a cable becomes broken**, the ON status of the M5 line (receiving level) by the jumper to M (next to MN).

The interfaces can also be operated without -12 V. "0 V" must therefore be connected with the -12 V pin (1c6) or jumpered. However, the signal levels no longer correspond to DIN 66 020. The jumpers on MN and D are to be plugged in for the operation with-

out -12 V. The T1 transmitter clock (V.24) is connected to the transmitter clock of the corresponding ACIA. The T4 receiving clock can be switched to the receiver clock of the corresponding ACIA for an external clock.

2 Interfaces can be switched to an external or internal receiver clock with the S1 and S2 jumpers. T4 supplies the receiver clock in the externally clocked operation; T4 has no effect in the internally clocked operation. T1 always supplies the transmitter clock.

The SEA1 and SEA2 interfaces include one independent, programmable transmission speed each. The interface signals are D1, D2, S2, M5, T1 and T4. SEA3, SEA5 and SEA6 have another programmable transmission speed, SEA4, SEA7 and SEA8 yet another one. The 3, 4, 5 and 8 interfaces are to be operated with the D1, D2, S2 and M5 signals. SAE6 and SEA7 are to be operated with the D1 and D2 signals.

2 Operating and Indicating Elements

The module does not include any operating or indicating elements whatsoever.



3 Configuration

The following is to be configured for the module:

- ☐ Specifying the memory address areas (module, segment)
- ☐ Number and equipment of the necessary interfaces
- ☐ Forced ventilation, if required
- ☐ Selection of the necessary firmware
- ☐ User software
- ☐ Transmission rate
- ☐ Protective circuit for the desired functions (A3 form)
- ☐ Connection cable inside the cabinet

3.1 Functional Jumpers



S Receiver Clock Guide

S		External	} S1: Interface 1 S2: Interface 2
S		Internal	

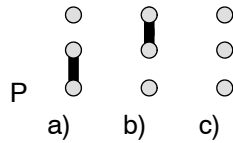
MN Event Signal Position (M5)

	MN	"OFF"	(receiving level without 12 V)
	MN	"ON"	(mentioned cable breakage position)

Data Signal Position (D2)

	D	"ON"	(receiving data without -12V)
	D	"OFF"	(see open-circuit signal position)

P Interrupt

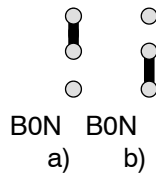


- a) Interrupt to the PMB via MPARN (call)
- b) Interrupt to the PMB via MSPFN (parity error)
- c) I. disabled (to be used with A500) = jumper is not plugged in

A12 ... A18

see section 3.2 "Addressing"

Status Bits



The assignment is addressed with KOS firmware, SEAB-1 start, DSW 078/99 starting from revision index .01

a) B0N = "0"
Waiting period for an answer in the slave, $t(ws) = 60T$ bit (WS = waiting period for slave) (as delivered)

b) B0N = "1"
Waiting period for an answer in the slave, $t(ws) = 0.8$ sec

Extending the waiting period is only valid for SEA1 of the KOS 882, if this is a slave, the remaining SEAs are not affected.

The waiting period must be selected via the B0N jumper **before the standardization** of the KOS 882 module.

B5N, status byte

B5N and SB0 ... SB7 are not used in A500

3.2 Addressing

A memory area of 8 kbytes must be made available during the configuration. The coding for the desired address area is read from the two tables.

			Jumpers									
		64 k-Block Address (Hex)	Segments	A18	A17	A16	A15	A14	A13	A12	8k-Block for	
Segments 3, 4: for ALU xxx except for ALU 821	→	00000	1, 2	0	0	0	0		0	0	0	1. KOS
		10000	3, 4	0	0	0	1		0	0	1	2. KOS
		20000	5, 6	0	0	1	0		0	1	0	3. KOS
		30000	7, 8	0	0	1	1		0	1	1	4. KOS
		40000	9, 10	0	1	0	0		1	0	0	5. KOS
		50000	11, 12	0	1	0	1		1	0	1	6. KOS
		60000	13, 14	0	1	1	0		1	1	0	7. KOS
		70000	15, 16	0	1	1	1		1	1	1	8. KOS
		80000	17, 18	1	0	0	0					
		90000	19, 20	1	0	0	1					
Segments 29, 30: for ALU 821	→	A0000	21, 22	1	0	1	0					
		B0000	23, 24	1	0	1	1					
		C0000	25, 26	1	1	0	0					
		D0000	27, 28	1	1	0	1					
		E0000	29, 30	1	1	1	0					
		F0000	31, 32	1	1	1	1					

"0" = \overline{Axx}

Jumppered to the non-labelled side

"1" = Axx

Jumppered to the labelled side

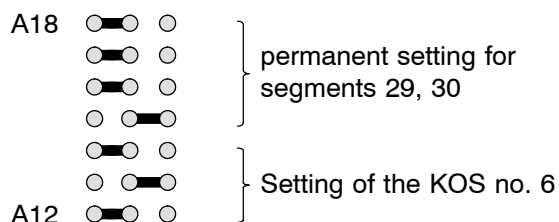
(xx from 12 ...18)

Figure 172 Addressing on KOS 882

The PMB is occupied by the DUAL port with the first 4 k addresses of the 8 k module area.

Addressing example for A500 with ALU 821

The KOS 882 is to be inserted as the 6th KOS module in segments 29 and 30. A12, A14, A16, A17 and A18 are jumpered here (see below).



3.3 Programming

- RAM area Via the bit-serial SST interface on UKA 024, with the corresponding Bsdol functions for configuring the data traffic for A500
- PROM area Insert the application-orientated firmware on EPROMs

3.4 Transmission Rate

The transmission rate can be set using the software from 50 ... 19 200 bits/sec.

3.5 Connection Cable inside the Cabinet

- see "System description, part 40: configuration" on page 40-23-07ff for a detailed treatment.
- port of periphery via the V.24 interface

KOS 882 ↔ SAE 2: subrack → cabinet connection unit
YDL 18.4
YDL 18.8

- Port of peripheries via the V.24/LS interface

KOS 882 ↔ UVL 84x ↔ SAE 2: subrack → cabinet connection unit
YDL 21.4 YDL 18.4
YDL 21.8

3.6 Ventilation



Caution If the KOS 882 module is equipped with more than 6 interfaces (UART), a forced ventilation is necessary!

3.7 Connector Pin Assignment with Serial Interfaces

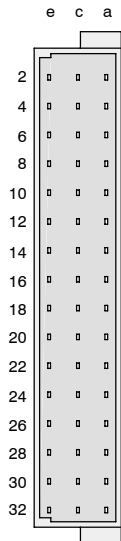


Table 64 Connector Pin Assignment of the E48M Connector in the KOS 882

e Row		c Row		a Row	
e 2	SEA 5D1	c 2	0 V	a 2	SEA 1D1
e 4	SEA 5D2	c 4	+12 V	a 4	SEA 1D2
e 6	SEA 5M5	c 6	-12 V	a 6	SEA 1M5
e 8	SEA 5S2	c 8	+5 V	a 8	SEA 1S2
e 10	SEA 6D1	c 10	Signal check loop	a 10	SEA 2D1
e 12	SEA 6D2	c 12	Signal check loop	a 12	SEA 2D2
e 14	-	c 14	SEA 1T4	a 14	SEA 2M5
e 16	-	c 16	SEA 1T1	a 16	SEA 2S2
e 18	SEA 7D1	c 18	SEA 2T4	a 18	SEA 3D1
e 20	SEA 7D2	c 20	SEA 2T1	a 20	SEA 3D2
e 22	-	c 22	0 V	a 22	SEA 3M5
e 24	-	c 24	0 V	a 24	SEA 3S2
e 26	SEA 8D1	c 26	0 V	a 26	SEA 4D1
e 28	SEA 8D2	c 28	0 V	a 28	SEA 4D2
e 30	SEA 8M5	c 30	0 V	a 30	SEA 4M5
e 32	SEA 8S2	c 32	0 V	a 32	SEA 4S2

nD1: Transmitter data
nD2: Receiver data

nM5: Receiver message
nS2: Transmitter

nT4: Receiver clock
nT1: Transmitter clock

n = 1 ... 8

3.8 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- ☐ included in the form block for conventional processing (see ordering data)
- ☐ included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

4 Specifications

4.1 Assignment

Product Family
Device

Modicon
A500

4.2 Supply Interface

U_{B5} (Internal) / I_{B5}

+ 5 V \pm 3%, typically 1.0 A (2 x UART + 2 x EPROM)
max. 2.1 A (4 x UART + 2 x EPROM)
max. 2.6 A (max. equipment)
+12 V \pm 5%, typically 30 mA
-12 V \pm 5%, typically 30 mA
0 V

Reference Potential

4.3 Data Interface	
Serial Data	V.24 interface according to DIN 66 020
SEA1, SEA2	2 permanently equipped V.24 interfaces; can be extended to max. 8 interfaces by means of ACIA blocks (68 A 50); can be equipped on sockets
4.4 Memory Structure	
Communications Buffer	RAM 8 k x 4 bits (NMOS, 2148 type) (variable assignment)
EPROM	4 x 4 kbytes (2732 type) on a socket, selective assignment with various firmware
Factory Delivery	unequipped, since it depends on the application
EPROM:	data safe: equipped, protect from UV light or sun light
RAM:	not backed up!
Memory Cycle Time	1 µs Hol cycle
4.5 Physical Characteristics	
Module Format	Size: 6 HE/4
Weight	340 g
4.6 Port	
PMB	C64M connector
Periphery	E48M connector
4.7 Environmental Conditions	
System Data	see user manual
Power Dissipation	max. 5.5 W ... 14 W
4.8 Ordering Data	
KOS 882 Module	424 167 619 (2 interfaces)
KOS 842 Module	424 211 843 (4 interfaces)
KOS 862 Module	424 211 840 (6 interfaces)
UART 68A50 Module	424 075 142 (interface element)
A3 Form Block	A9M.12-234 720

Technical rights are reserved!

LLB Air Guide Module Description

The air guide has to be built into control cabinets and serves as a cooling air duct between the subracks.

1 General

The air guide has to be built into cabinets and serves as a cooling air duct between the subracks. It is supplied in two designs:

- LLB 2: as cooling air duct between the subracks (ventilation duct without slanted plate)
- LLB 2.1: as cooling air diversion to the wiring room above the power dissipation intensive subracks (ventilation duct with slanted plate)

2 Operation and Display

The module has neither operational nor display elements.

3 Configuration

3.1 Dimension Drawing

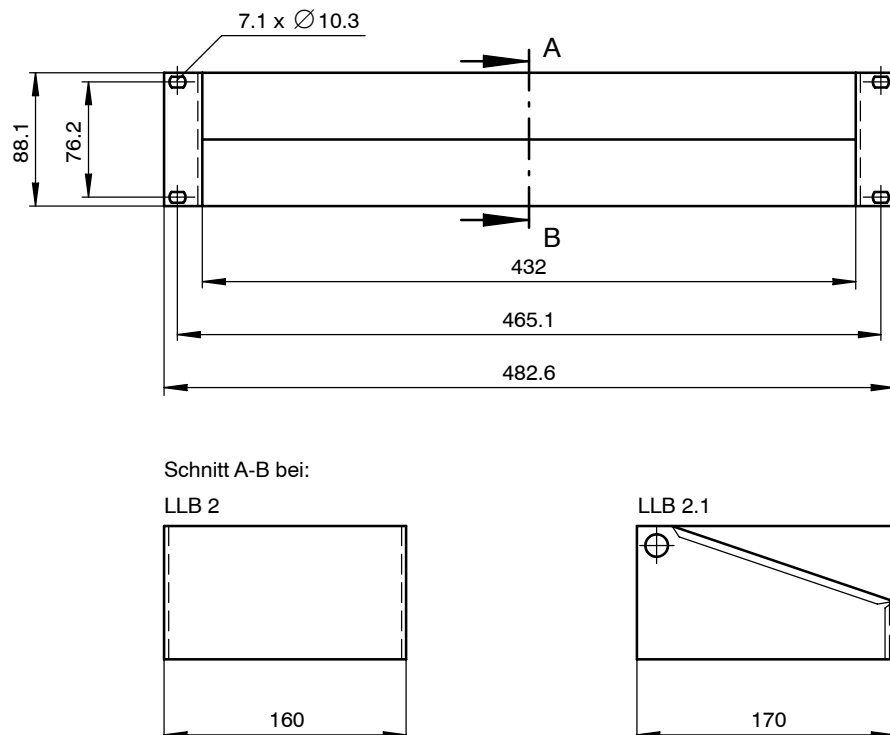


Figure 173 Dimension Drawing LLB 2, LLB 2.1

4 Specifications

4.1 Allocation

Devices	A350, A500
Assembly Area	Cabinet/swing frame

4.2 Mechanical Structure

Dimensions	Rack 19" x 2HE (482 x 170 x 88 mm) according to DIN 41 494
------------	--

Mass (Weight)

LLB 2:	Approx. 1.1 kg
LLB 2.1:	Approx. 1.5 kg

Surface	Zink galvanized, bare
---------	-----------------------

4.3 Ordering Details

Module LLB 2	424 142 110
Module LLB 2.1	424 166 807

Specifications subject to change without notice.

MAT 827

Arithmetic Processor

Module Description

The additional module MAT 827 facilitates the function expansion of the central processing units ALU 150 and ALU 821 by commands for mathematical and automatic control engineering tasks.

1 General

The additional module MAT 827 facilitates the function expansion of the central processing units ALU 150 and ALU 821 by commands for mathematical and automatic control engineering tasks. It is necessary for all software units with floating point operations (SW blocks which are characterized by "G" or belong to the packages "floating point arithmetic" and "floating point measuring value processing").

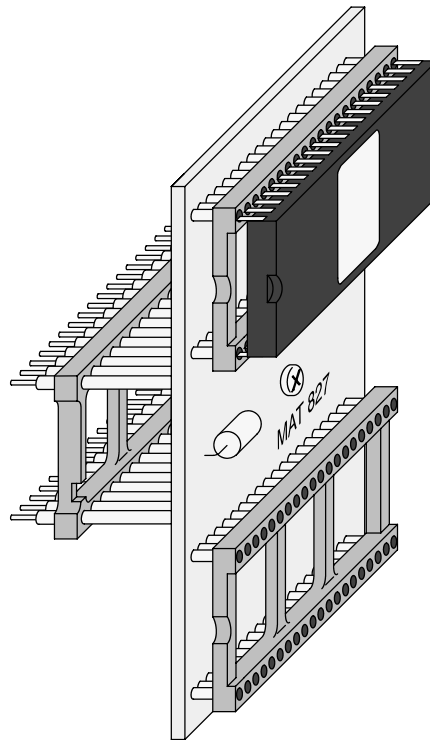


Figure 174 Front View of MAT 827

1.1 Physical Characteristics

The module is a printed circuit board in the special format with two 40-pole DIP sockets for microprocessors and a 40-pole DIP socket for equipment mounting on the central processing unit. The upper DIP socket is equipped with the numerical data processor 8087.

1.2 Mode of Functioning

The module MAT 827 carries the parallel operating processors 8086 (drawn from the respective ALU) and 8087, from which the latter expands the functions of the ALU for processing mathematical and automatic control engineering programs.

Via equipping with the numerical data processor 8087, the processing of numerical mathematical problems attains a 10 to 100-fold calculation speed.

In terms of software the MAT 827 expands the ALU 150 or 821 by several data registers for processing the additional command store. Bit 6 of the status byte (I/O address 800 H) which has been free up to now is now occupied by the signal "PEAB time error".

The description of the applicable commands can be drawn from the corresponding problem-orientated software packages.

2 Operating and Display

The module contains neither operational nor display elements.

3 Configuration

The additional module MAT 827 is plugged in instead of the microprocessor 8086 to the basic board of each central processing unit and is screwed onto this.

3.1 Mounting the MAT 827

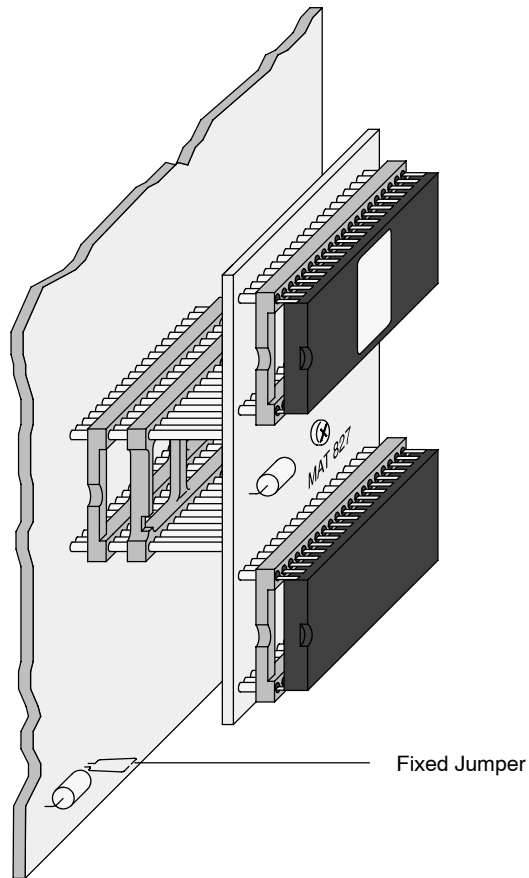


Figure 175 Mounting the MAT 827 on the ALU

- Step 1** Remove the microprocessor 8086 from the ALU and insert it in the empty socket of the MAT 827
- Step 2** Insert the MAT 827 on the slot of the microprocessor 8086 of the ALU
- Step 3** Screw together both PCBs on the rear of the ALU
- Step 4** Unplug the fixed jumper "B" of the ALU (see Figure 175)

3.2 Documentation

For the system documentation the module is integrated in the A3 form sheet of the carrier module.

4 Specifications

4.1 Allocation

Devices	A350, A500
Structure	Instead of the microprocessor on the carrier module ALU 150 and ALU 821

4.2 Supply

Taken over by carrier module ALU xxx

4.3 Data Interface

PMB	Parallel microprocessor bus
-----	-----------------------------

4.4 Mechanical structure

Dimensions	60 x 56 x 30 mm
Mass (Weight)	50 g

4.5 Mode of Connection

1 x DIP connector 40-pole
2 x DIP connector 40-pole

4.6 Environmental conditions

System Data	See user instruction, chapter 4
Power Dissipation	2.5 Watt typical

4.7 Ordering Details

Module MAT 827	424 203 633
A3 Pad	See carrier module

Specifications subject to change.

SAE 2

Cabinet Connection Unit

Module Description

The cabinet connection unit SAE 2 has to be mounted in the swing frame of the control cabinets and serves

- ▣ to feed in voltage into the cabinet
- ▣ to connect interfaces between the controller and the cabinet

Therefore, it is fitted with a disconnection choke and radio protection filter elements.

1 General

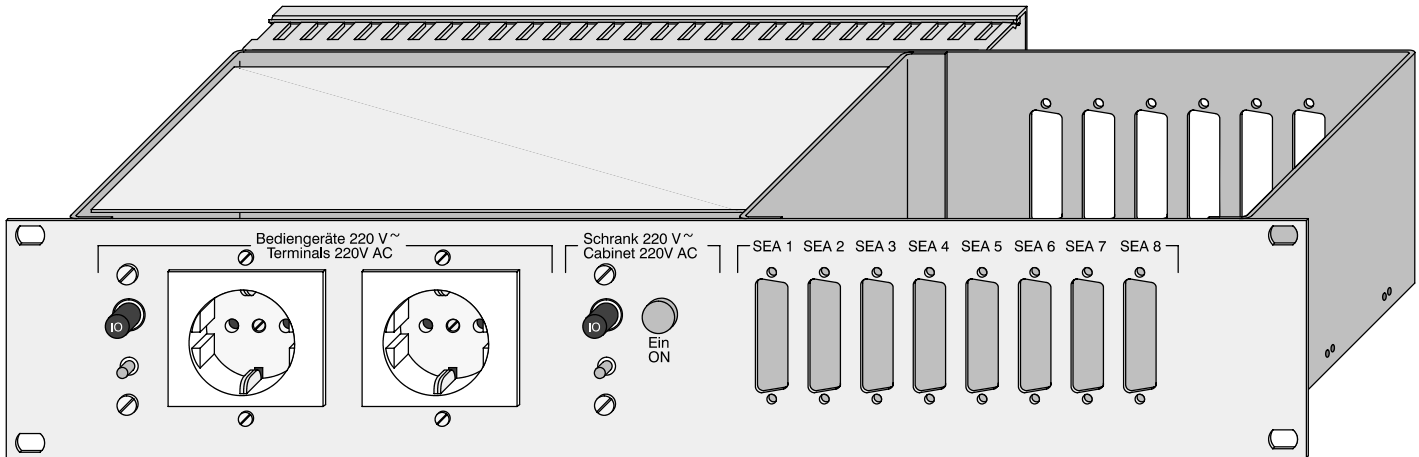


Figure 176 Cabinet Connection Unit SAE 102

1.1 Mode of Functioning

Disconnection of Interference is gained by the following measures:

- ☐ Voltage input and output is disconnected from conducted noise by interference suppression filter and HF partition
- ☐ The PE terminals of the input and output are connected via chokes (may not be connected directly)
- ☐ There is a touch cover partition between power supply and serial interfaces

2 Operation and Display

The front plate of the module has one indicator:

- ☐ 1 green LED for Voltage supply
 - ON: Swing frame supply available
 - OFF: Swing frame supply not available

3 Configuration

3.1 Connection of SAE 2

Figure 177 shows the connection of SAE 2

Input voltage is fed in frame below, output voltage is led out to the top (spatial disconnection).

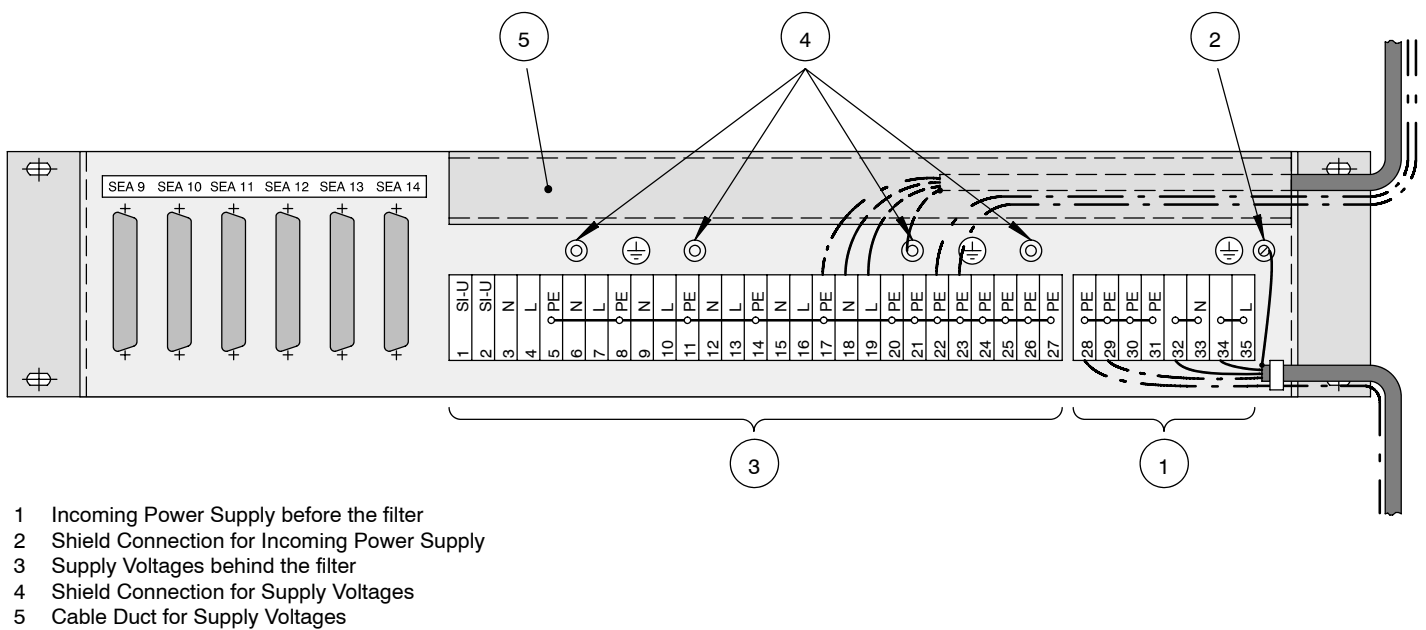
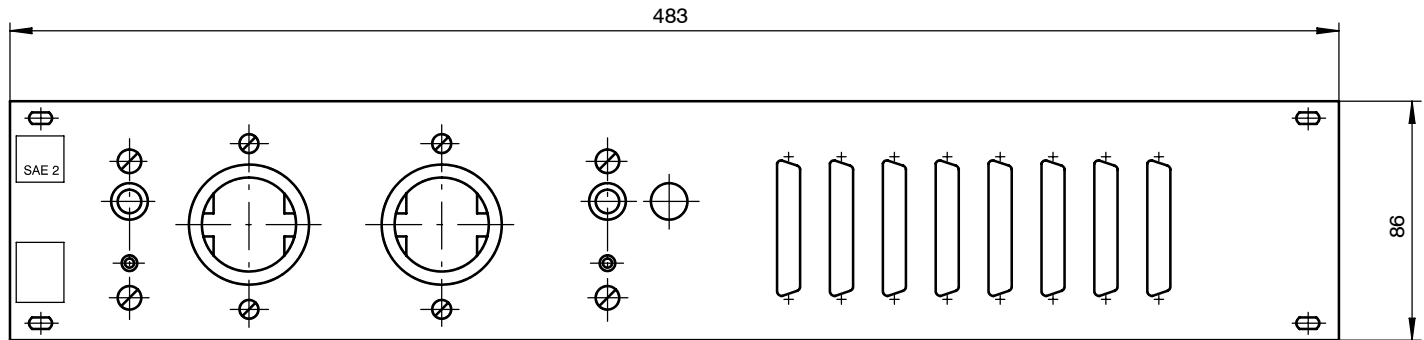


Figure 177 Connection of SAE 2

3.2 Dimension Specifications

Front View



Side View

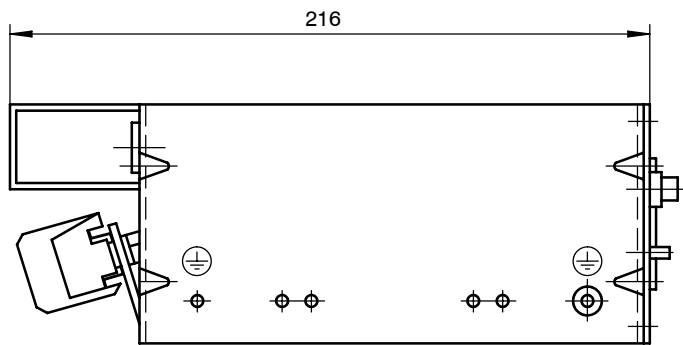


Figure 178 Dimension Drawing of Cabinet Connection Unit SAE 2

3.3 Documentation

For the system documentation an A3 form sheet with explanations is available in which the connection wiring is given. These form sheets are

- ☐ part of the form pad and intended for conventional processing (see ordering details)
- ☐ part of the Ruplan processing data base (under development) and intended for Ruplan processing (technical sales office version)

4 Specifications

4.1 Allocation

Devices	A350, A500
Slot	Cabinet/swing frame

4.2 Voltage Input

Phase L	220 VAC,	class 34, 35
Neutral N	MP,	class 32, 33
Reference Potential PE	Protective earth,	class 28 ... 31

4.3 Voltage Outputs

Unfiltered	2 protective contact sockets for peripheral devices	
Fuse	10 A overload trip	
Filtered		
Phase L	220 VAC,	class 4, 7, 10, 13, 16, 19
Neutral N	MP,	class 3, 6, 9, 12, 15, 18
Reference Potential PE	via choke,	class 5, 8, 11, 14, 17, 20 ... 27
Fuse	10 A overload trip for consumers within the cabinet	

4.4 Connections for Data Interfaces (Line Current Loop, V.24)

Front	8 breaks	} Prepared for 25-pole standardized plug connections with screen connections
Rear	6 breaks	

4.5 Physical Characteristics

Dimensions (W x H x D)	Rack 19" x 2HE (483 x 86 x 216 mm) according to DIN 41 494
Mode of Connection	35 series connectors 0.5 ... 4 mm ²
Mass (Weight)	2 kg

4.6 Ordering Details

Module SAE 2	424 207 112
A3 Form Pad	A91M.12- 234 721

Specifications subject to change.

SC 8128 / SC 8256 Memory Module (RAM) Module Description

The SC 8256 / SC 8128 module is a memory bus node and complements the microprocessor of the ALU 150 and the ALU 821. The memory capacity amounts to 128 kbytes (SC 8128) or 256 kbytes (SC 8256) depending on the IC equipment and is equally suited to save process data or user programs (during the start-up phase). The module is non-volatile only if a backup battery is connected. This is the case of the module is inserted in the subrack.

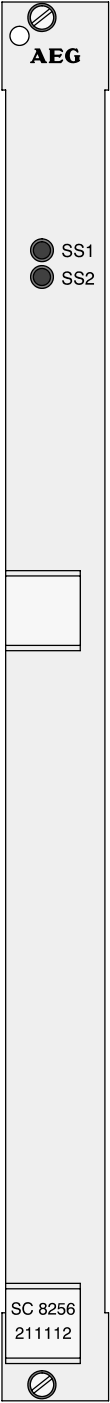
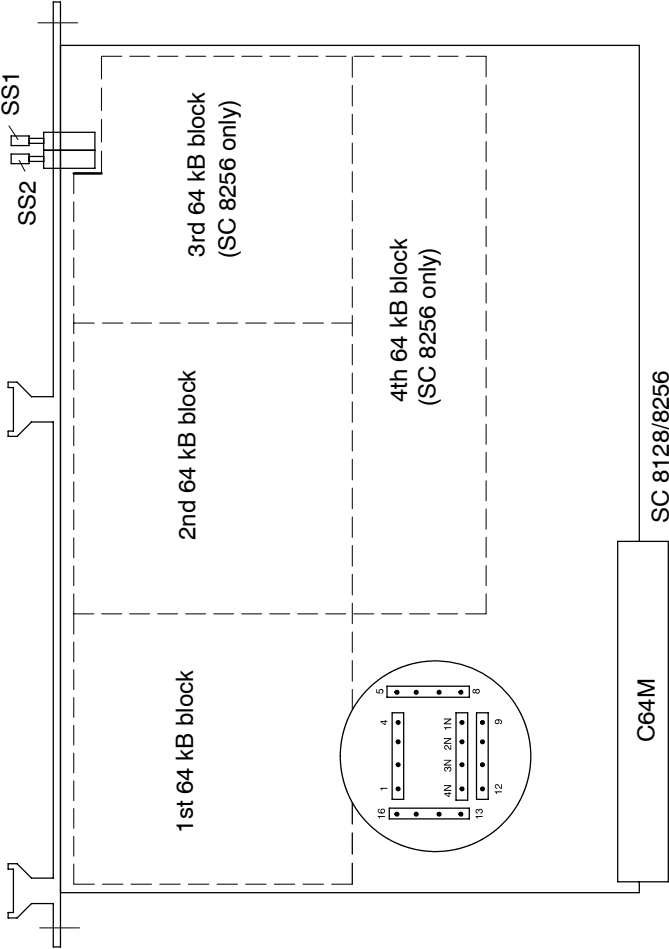


Figure 179 Front View of the SC 8256



- SS1 / SS2: Contact pins for write disable
- 1N ... 4N: Code post for 64k blocks
- 1 ... 16: Code post for segment pairs

Figure 180 Survey of the Configuration Elements for SC 8128 / SC 8256

1 General

1.1 Physical Characteristics

The two modules have a double Europe format with a construction width of 4T, similar layout with a code field to set the block address and a 64 pole connector for the PMB area. They only differ due to the number of the permanently soldered writing/reading memory elements is different.

1.2 Mode of Functioning

The module has an internal 16 bit word structure, from which the pair assignment of the memory elements results. These are summarized in blocks of 64 kbytes each as regards the addressing and are addressed in the code field using code lines or assigned to corresponding segment pairs of the entire memory area (1 mb). Memory blocks can be write-protected individually (with 128 kb) or in pairs (with 256 kb) with 2 contact pins in the front panel.

The two types thus only differ in the functions due to the memory capacity, the number of code lines (4 or 2) and the assignment of the write disable areas (see operation / presentation). The latter are specified by the memory scope.

2 Operating and Indicating Elements

The module has no operating and indicating elements.

3 Configuration

The following is to be configured for the modules:

- ☐ Addressing the memory blocks
- ☐ Specifying the write disable areas
- ☐ Documentation on standard forms

3.1 Coding

The address area is specified by the assignment of the 64 kbyte blocks to the segment pairs. The 32 segments correspond to the whole memory/address area.

The 1N ... 2N (1N ... 4N) code posts are assigned to the 2 (4) blocks, the 1 ... 16 code posts to the segment pairs.

64 kbyte blocks which are not coded are disabled for the module; however, their address areas can be occupied by other modules.

Table 65 Coding the RAM blocks for the SC 8128/SC 8256

Contact Pin	Segment	Contact Pin	Segment
1	1, 2	9	17, 18
2	3, 4	10	19, 20
3	5, 6	11	21, 22
4	7, 8	12	23, 24
5	9, 10	13	25, 26
6	11, 12	14	27, 28
7	13, 14	15	29, 30
8	15, 16	16	31, 32

Coding Example

The 2nd 64 kb block is to be coded to segments 9 and 10.

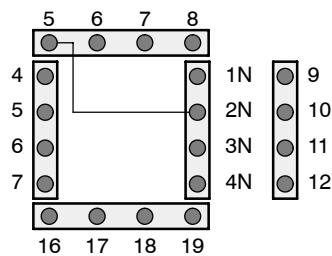


Figure 181 Coding Example for the SC 8128/SC 8256

3.2 Write Disable

The module includes 2 contact sockets in the front panel which serve the specification and are to be write-protected for the memory blocks. The following specifications are valid:

SS1 (top) plugged in:

- ☐ SC 8256: 1st and 2nd 64 k block is write-protected (contact post 1N and 2N)
- ☐ SC 8128: 1st 64 k block is write-protected (1N)

SS2 (bottom) plugged in:

- SC 8256: 3rd and 4th 64 k block is write-protected (contact post 3N and 4N)
- SC 8128: 2nd 64 k block is write-protected (2N)



Caution This configuration measure may not be altered by the process operator!

3.3 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version) (in preparation).

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500

4.2 Data Interface

PMB	Parallel microprocessor memory bus
Address Area	1 mbyte
Coding	flexible jumpers
Data Save	RAM: non-volatile due to the backup battery, if it is inserted in the subrack

4.3 Capacity

SC 8256	256 kbytes
SC 8128	128 kbytes (partially equipped)

4.4 Supply Interface

U_{B5} / I_{B5}	typically +5 V / 0.3 A (max. 0.5 A)
Backup Current (battery)	typically 10 ... 100 μ A (max. 3.2 mA) (for SC 8128: approx. 50 % backup current)

4.5 Physical Characteristics

Module	Double Europe format, size: 6/4 T
Type of Port	1 C64M connector
Weight	350 g

4.6 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	typically 1.5 W (max. 2.5 W)

4.7 Ordering Data

SC 8256 Module	424 211 112
SC 8128	424 211 838

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SF 8512

Memory Module (EPROM)

Module Description

The SF 8512 module includes a memory field with sockets for UV deletable EPROMS (permanent value memory). The memory field can accept 32 memory elements. The module is designed for an address area of 1 mbyte.

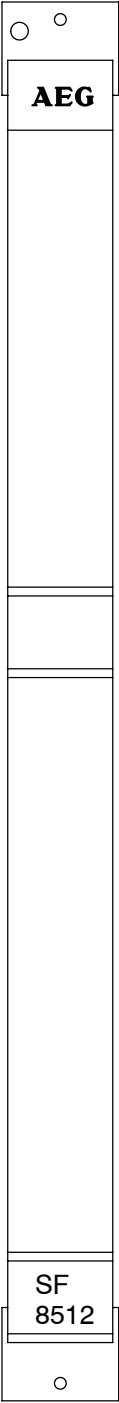
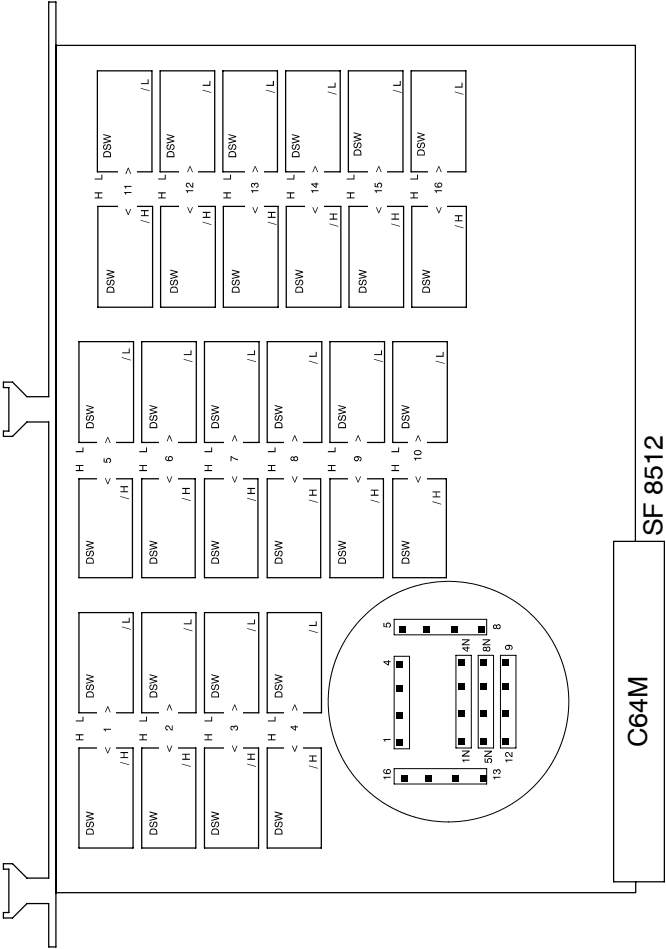


Figure 182 Front View of the SF 8512



Equipment

8 blocks of 64 kbyte each	Seg.
1st block	1L ... 2H (+)
2nd	3L ... 4H (+)
3rd	5L ... 6H (+)
4th	7L ... 8H (+)
5th	9L ... 10H (+)
6th	11L ... 12H (+)
7th	13L ... 14H (+)
8th	15L ... 16H (+)

Figure 183 Survey of the Configuration Elements for SF 8512

1 General

1.1 Physical Characteristics

The module is 4T wide and has rear connection and a double Europe format. It is equipped with a C64M connector. The address area is set on the equipment side with flexible jumpers.

1.2 Mode of Functioning

The module includes a memory field with a socket for 16 high byte and 16 low byte elements. 2 memory elements only are activated each time for the addressing; all other elements are then on standby and thus require only very little supply current.

The module is designed for the entire address scope of 1 mb and can be coded for any 8 blocks of 64 kb each. This is carried out with 8 flexible jumpers.

2 Operating and Indicating Elements

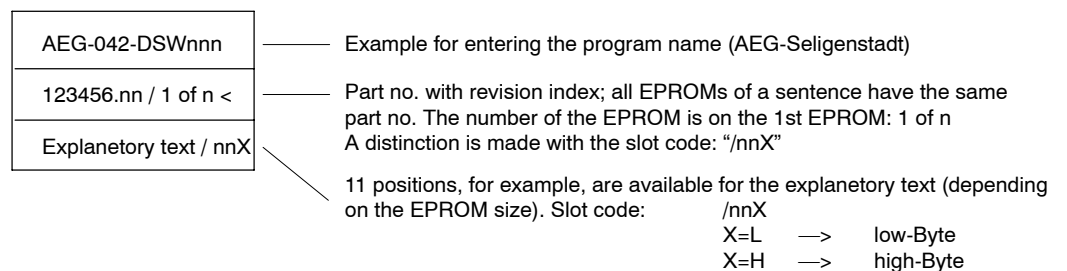
The front panel includes no operating and indicating elements whatsoever.

3 Configuration

The following is to be configured for the module:

- ☐ Specifying the slot
- ☐ Physically coding the memory addresses (cf. 3.2)
- ☐ Documentation

3.1 Labelling of the EPROMs



3.2 Coding the Address Areas

The following table shows:

- the 64 k block assignment of the 1H-2L, 3H-4L, ..., 15H-16L slots to the 1N ... 8N code pins.
- the physical assignment of the 1 ... 16 code pins to segment pairs 1, 2 ... 31, 32 and their address groups.

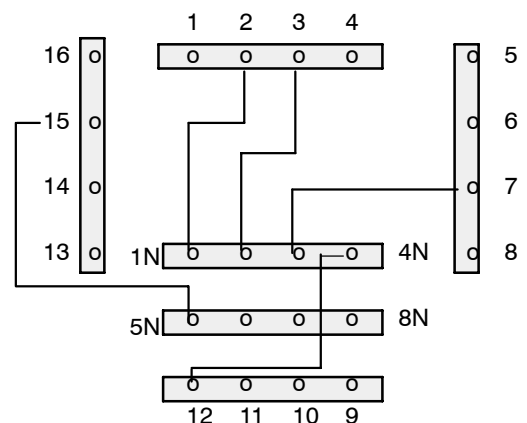
The assignment of 84 k blocks to the address groups can be arranged freely between the table halves (with a grey background) with a maximum of 8 flexible wire jumpers.

Table 66 Coding the EPROM Addresses on the SF 8512

Slot	C o d e Pins		Segment	Address	
1H - 1L	1N	→	1	1, 2	00000 - 0FFFF
2H - 2L	1N		2	3, 4	10000 - 1FFFF
3H - 3L	2N		3	5, 6	20000 - 2FFFF
4H - 4L	2N		4	7, 8	30000 - 3FFFF
5H - 5L	3N	free	5	9, 10	40000 - 4FFFF
6H - 6L	3N		6	11, 12	50000 - 5FFFF
7H - 7L	4N	assignment	7	13, 14	60000 - 6FFFF
8H - 8L	4N		8	15, 16	70000 - 7FFFF
9H - 9L	5N	with flexible	9	17, 18	80000 - 8FFFF
10H - 10L	5N	jumpers	0	19, 20	90000 - 9FFFF
11H - 11L	6N		1	21, 22	A0000 - AFFFF
12H - 12L	6N		2	23, 24	B0000 - BFFFF
13H - 13L	7N		3	25, 26	C0000 - CFFFF
14H - 14L	7N		4	27, 28	D0000 - DFFFF
15H - 15L	8N		5	29, 30	E0000 - EFFFF
16H - 16L	8N	→	6	31, 32	F0000 - FFFFF

Coding Example:

4 EPROM areas are to be specified to
 1st 10000 - 2FFFF (128 kB): 1N → 2
 (Segm. 3, 4, 5, 6) 2N → 3
 2nd 60000 - 6FFFF (64 kB): 3N → 7
 (Segm. 13, 14)
 3rd B0000 - BFFFF (64 kB): 4N → 12
 (Segm. 23, 24)
 4th E8000 - EFFFF (32 kB): 5N → 15
 (Segment 30, segment 29 is addressed
 as well and therefore cannot be used on
 another module)



3.3 Ventilation

If the module is to be operated without a fan (convection only), it is to be ensured that sufficient space is left above and below the subrack to create an air current. Air guides are also to be provided.

3.4 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard entries of circuit elements are already entered. These form sheets are

- included in the form block for conventional processing
(see ordering data)
- included in the A500 Ruplan data bank for Ruplan processing (Technical Sales Office version)
(in preparation)

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	PMB node, memory slots
Application	Carrier module for UV deletable EPROMs (permanent value memory)

4.2 Data Interface

Information	form the PMB
Capacity	512 kbytes
EPROM Type	27128 = 16 k x 8 bits
Address Area	1 MB
Addressing	can be addressed in 64 k blocks
Occupation with Programming	system software, basic software, user software plugging in programs EPROMs, note the order for high and low data bytes (see protective circuit)
Factory Delivery	not equipped

4.3 Supply Interfaces

U_{B5}	+ 5 V
I_{B5} for 32 kbytes	typically 300 mA (max. 450 mA)
Each Further 32 kBytes	30 mA

4.4 Physical Characteristics

Module	Double Europe format, size: 6/4T
Type of Port	1 C64M connector
Weight	
□ not Equipped	280 g
□ fully Equipped	320 g

4.5 Environmental Conditions

System Data	see user manual
Power Dissipation	
□ for 32 kBytes	typically 1.5 W (max. 2.4 W)
□ fully Equipped	typically 3.75 W (max. 9 W)

4.6 Ordering data

LLB 2 Air Guide	424 166 807
SF 8512 Module	424 211 115
A3 Form Block	A91M.12-234 720

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UKA 024

Monitoring Module

Module Description

The UKA 024 module is used together with the ALU 150, ALU 286 and ALU 821 central processing units. It is an I/O bus node with a fixed slot in the DTA 024, DTA 27.1, DTA 028, DTA 101 or DTA 107 subracks.

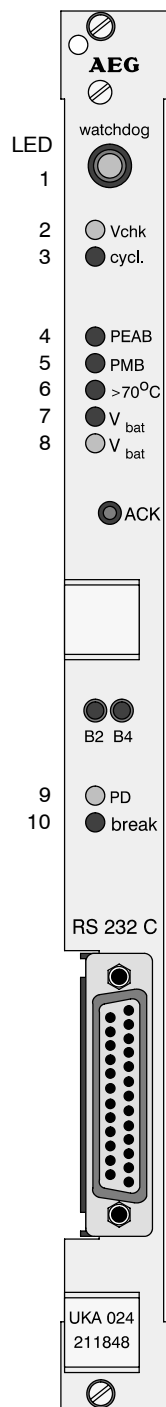
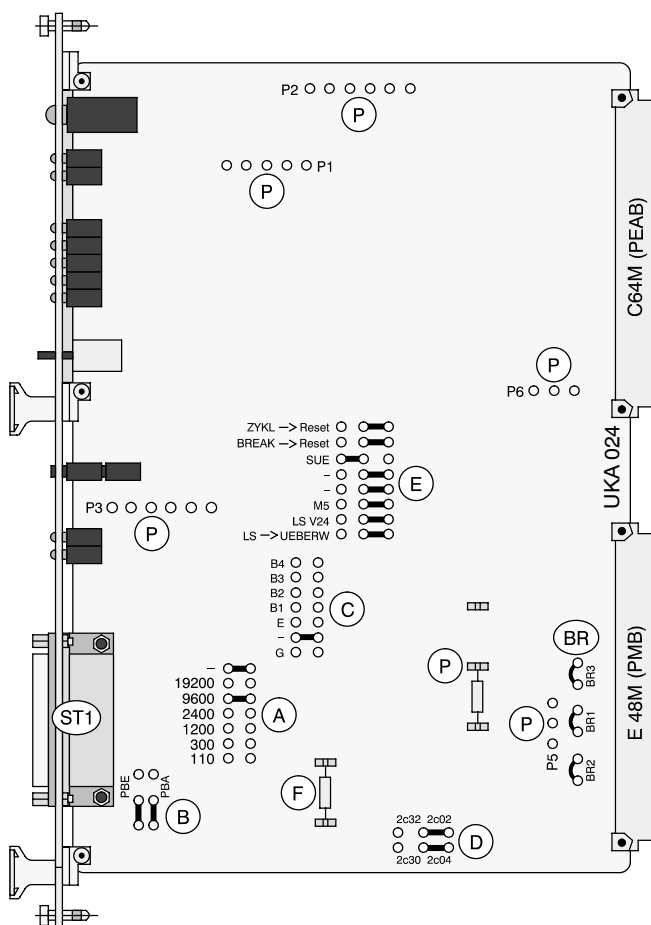


Figure 185 Front View of the UKA 024



- A Transmission rates
- B Non-isolation for LS or potential-free (FREE)
- BR Voltage monitoring, 24 / 48 / 60 VDC
- PBE: Input circuit, PBA: Output circuit
- C B1 ... B4, E, G status bits, single bit setting
- D External / internal supply of the current loop source (LSQ)
- E Monitoring, conversion, special functions
- F Program cycle time
- Factory delivery: R462 = 82 kohms = 82 ms
- P Test field ports

Figure 186 Survey of the Configuration Elements UKA 024

1 General

1.1 Physical Characteristics

The module has a double Europe format with rear connection and a width of 4T, with rear contacting for peripheral signals, front operating elements and a serial interface for communication devices.

1.2 Mode of Functioning

It realizes greater (as opposed to the UKA 023) operating and control functions with LED indicators, push buttons and pilot relays and offers a serial interface which can be switched over in the front panel and is non-isolated for V.24 and isolated when converted to the current loop for the operation of periphery. It cannot be used in the DTA 022 with DNO 022 as a replacement for the UKA 023. It does not include the 5 VDC supply to operate the PTY pocket terminal either.

2 Operating and Indicating Elements

"Watchdog" Indicator (LED 1)

This green LED signifies the correct operation of the system with the pilot relay picked up. The relay drops out if

- there is undervoltage of the voltage to be monitored (voltage check: "Vchk" = LED 2)
- the Vlist is stationary (cycl = LED 3)
- the Vlist is running but there is a group error (marker 60 is set)

PEAB, PMB (LEDs 4, 5)

The functions are to be defined with the software. They indicate the valances of the 61 and 62 markers.

Access Temperature (LED 6)

Temperatures > 70 °C are evaluated (marker 22) and indicated with the red LED ">70 °C".

Battery Check (LED 7)

The backup battery for the CMOS memory is checked at the time when the mains is switched on and any undervoltage (information loss) is indicated with a red LED and evaluated (marker 23 = rechargeable battery undervoltage; this can be acknowledged with the "ACK" key on the front panel and it prevents the program start).

Rechargeable Battery Load Test (LED 8)

The load test is carried out automatically every 4 hours or with the "ACK" key:
The backup battery is loaded with 650 mA for 1 s; if V_{bat} does not reach the limit value of 3.5 V, the green LED " V_{bat} " starts to flash.
Marker 28 (rechargeable battery load test with boot loading) and 38 (rechargeable battery load test since restart) are set as well if the PEAB monitoring is entered with "DKU 022" in the EQL list for slot reference 16 (I = 5; O = 5).

The green LED goes out if the nominal voltage is not reached between 2 load tests and marker 23 is not set.

Programming panel indicator (LED 9)

This green indicator lights up if a programming panel is connected and the M5 signal given (see section 3.9).

Break indicator (LED 10)

This indicator lights up if the “break” is sent by the programming panel and the “BREAK → RESET” jumper is closed (as delivered).

3 Configuration

The following is to be configured for the module:

- ☐ UKA 024 ↔ programming panel transmission rate
- ☐ EQL list standardization
- ☐ PEAB monitoring, if required (section 3.6)
- ☐ Monitoring a voltage (section 3.3)
- ☐ External LS supply, if required
- ☐ Adapting the signal level
- ☐ Non-isolation for LS operation
- ☐ Adapting the program running time, if necessary (section 3.1)

3.1 Program Cycle Time

The checking time set to approx. 82 ms by the factory with R462 = 82 kΩ (reset pulse for each program cycle) is indicated if exceeded (LED “watchdog” is deleted) and evaluated (pilot relay drops out). Change the checking time for long programs: 220 kΩ results in 220 ms. F in Figure 186 shows the position of the resistor to be changed.

3.2 Single Bit Entry (G, E, B1 ... B4)

The signal level (plugged in jumper = low level) pre-given on jumper group (C) is switched through to the data lines by entering the 0 subaddress. B2 and B4 are also available on the front panel parallel to the internal jumpers.

For **automatic RESET** and **BREAK detection**, see chapter 3.8, jumper group E

3.3 Voltage Monitoring (LED 2, Jumper SUE)

Any supply voltage (can be switched over with BR1 ... BR3, see Table 67) is monitored for undervoltage. It is evaluated, if

- ☐ the “SUE” jumper is plugged in on the jumper slot (jumper field E)
- ☐ the limit value for $t > 1$ ms is exceeded

The event is indicated for at least 100 ms (LED “Vchk” and “watchdog” go out, the pilot relay drops out).

Table 67 Setting the Value of the Voltage to be Monitored (on UKA 024)

SUE (2c04) SUE0 (2c02)	BR 2	BR 1	BR 3	Limit
24 VDC				18 VDC
48 VDC				34 VDC
60 VDC				44 VDC

The operation enable is executed if the supply and the voltage to be monitored for t > 100 ms exceed the minimum value.

Acknowledgement (ACK key)

Error messages can be acknowledged with the ACK key (front panel) if the error is no longer valid at the time of the acknowledgement. The length of the acknowledgement signal is the same as the time while the key is pressed.

3.4 Graphical Symbols

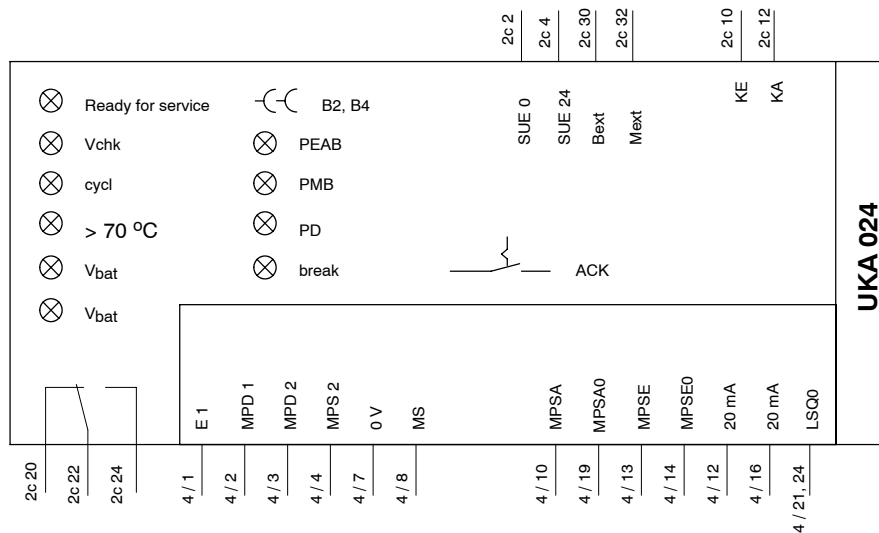


Figure 187 Graphical Symbol for UKA 024

3.5 Plug-In Check

Output 2c12 (KA) outputs a 12 V signal which is looped via all the I/O modules of the controller. The loop is closed at 2c10 (KE) of the UKA. An interrupted loop is evaluated (marker 20). If a signal check loop is not to be connected, 2c10 is to be jumpered with 2c12.

3.6 PEAB Monitoring

The perfect condition of the PEAB is monitored and signalled by saving and rewriting PEAB signals. The following figure shows the hardware prerequisites for a system

which is to be operated with PEAB monitoring. All the types of primary subracks are permitted.

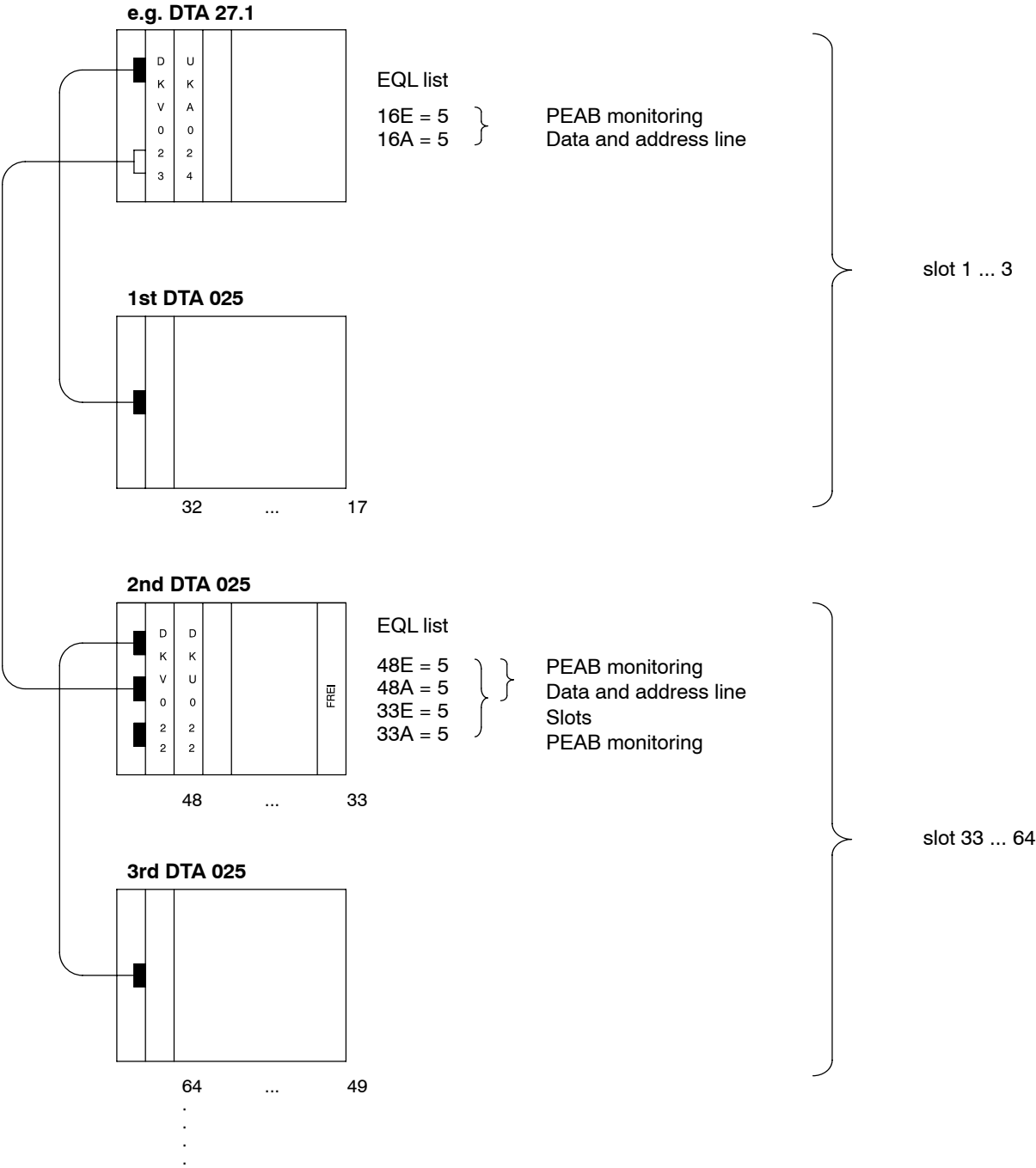


Figure 188 A500 Configuration when Extending PEAB with Monitoring

The information summarized in the following table is saved by the UKA 024 for monitoring with software comparative evaluations:

Table 68 Saving Information by the UKA 024 for Monitoring Purposes

Time	Saving
each output cycle each input (EIX) cycle and each addressing (ADX) cycle except for slot 16, subaddress 0+1	Information concerning <input type="checkbox"/> Data lines <input type="checkbox"/> Address lines <input type="checkbox"/> Control lines
Input cycle on slot 16, subaddress 10	Rereading the <input type="checkbox"/> data of the last PEAB cycle
Slot 16, subaddress 1	<input type="checkbox"/> Slot references and subaddresses <input type="checkbox"/> Level of the control lines of the last PEAB cycle

Monitoring Range:

Primary subrack + 1st secondary subrack (without DKU 022)

☐ Entry in the EQL list:

The following is to be entered in the EQL list for slot 16
(slot reference 16 in the DTA 024/027/028) to activate the PEAB monitoring:
16E = 5, 16A = 5

Effect: The perfect condition of I/O bus data lines and address lines is tested when the Vlist starts.

Expanded Monitoring Range:

starting from the 2nd secondary subrack

☐ Hardware supplement:

The PEAB monitoring module (DKU 022) is also required. It is inserted in the secondary subrack on the righthand side next to the DKV 022.

☐ Entry in the EQL list:

The following is to be entered for the DKU 022 slot: e.g., 48E = 5, 48A = 5

Effect: The data line test is executed when the Vlist is stated.

☐ Additional entry in the EQL list:

The following is to be entered for the lowest slot of the 2nd secondary subrack:
e.g., 33E = 5, 33A = 5

This slot can then no longer be occupied with an I/O module!

Effect: The address line list is also executed for the 2nd and 3rd secondary subracks (addressed via DKV 023).

The mentioned monitoring can be used for the following subracks:

- ☐ DTA 024 starting from revision index 06
- ☐ DTA 025 starting from revision index 05
- ☐ DTA 027 starting from revision index 06
- ☐ DTA 028 in full

3.7 Software Evaluation and Indicating Error Messages

The following table gives a summary of error messages which are available in the signal memory as system markers.

Table 69 Summary of the system markers set by the UKA 024

Type of marker		Indicator if there is an error	Comment
Plug-in check	20/30*	--	
Access temperature	22/32*	red "> 70 °C", ON	
SUE undervoltage, stationary Vlist, any group error	60	green "Vchk", red "cycl", none OFF ON	
Rechargeable battery undervoltage with mains ON	23/33*	red "V _{bat} ", ON	prevents program start can be acknowledged with the "Q" key
Rechargeable battery load test	28/38*	green "V _{bat} ", OFF flashing (after OFF as well)	with undervoltage between the regular load tests with undervoltage after the load test
PEAB monitoring	61 28/38 **)	red "PEAB", ON	The function is saved, i.e., the reset must be carried out with the Vlist
PMB monitoring (memory test)	62	red "PMB", ON	

*) since boot loading / RESET

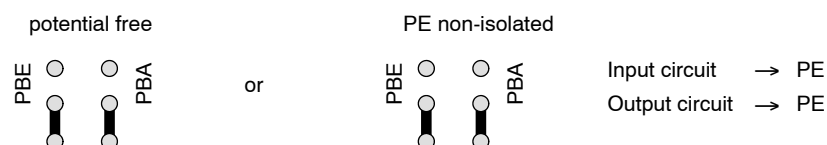
**) in addition, if "DKU 022" is entered in the EQL list for program monitoring

3.8 Explanations for the Functional Jumpers

All the jumper slots designated with "-." can be used as storage slots for plug-in jumpers.

A described function is only realized if the plug-in jumper is plugged in on the side of the jumper slot which is labelled for the corresponding function.

Jumper Group (B): Reference potential for current loop sources:



Jumper Group (D): Supply of the two 20 mA current loop sources (LSQ):



Caution If a voltage of 48 VDC or 60 VDC is monitored with BR1 ... BR3, the current loop sources must be supplied from B_{ext}.

Jumper Group (A):

19 200 ... 110 Selection of the transmission rate between A500 and periphery according to the jumper field labelling in bits/s.

Jumper Group (C):

- B3 ... B4 Freely available bits, can be defined by the software
- B2 Transparent mode for B500
- B1 System variables are automatically restored
- System variables are **not** automatically restored

E Single bit entry

G Sensor bit standardization

} see part 20-26, "Programming"

} 2 status bits; software evaluation



Caution The "E" jumper may not be plugged in when using the system field bus version 2.3 since otherwise the EQL list processing is blocked.







Jumper Group (E):

Table 70 Settings on the E Jumper Field of the UKA 024

Label	Position	Switch Status	Meaning
CYCLE → RESET	(9—8)		These two jumpers are to be left in the state shown and not used by t he user RESET is only possible with the contact pin through the front panel of the ALU!
BREAK → RESET	(10—7)		
SUE	(11—6)		Monitoring no monitoring
	(12—5)		without meaning, storage slot for jumpers
	(13—4)		without meaning, storage slot for jumpers

3.9 Connecting a Programming Panel

Table 71 Start-Up Characteristics of the A500 set by the UKA 024

System Status	M5 Jumper	Programming Panel Status	Effect
Switching on the A500		not connected	automatic program start or switched off (automatic start)
		connected and switched on (M4 signal is present)	no automatic program start (manual start)
A500 is switched on		is being connected	none
		M5 signal is present	HE: program stop
		M5 signal is not present	HE: short program interruption with restart
Switching on the A500		not connected	no automatic program start (manual start)
		switched off, pin 8 on the cable connector is open or high-impedant	
A500 is switched on		random	HE: program stop S, START: Program start
		is being switched off	none
LS → V.24		received signals of periphery are converted to V.24 for the ALU by the current loop (LS)	
		peripheral signals are handed over as V.24 signals	
LS MONITORING (16 - 1)		the current loop (LS) transmit data are saved on M5; a flowing current loop is thus detected.	
		Jumper position for V.24 signals	

Start-up order

The start-up order is described in the user manual in the "Initial start-up" section.



Caution If I/O modules without isolation (e.g., DEO 013, DAO 012) are inserted in an A500 equipped with UKA 024, it is to be ensured that the ports for 0 V and M2 are jumpered on the primary subrack (DTA 024, DTA 027, DTA 028).

3.10 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings of circuit elements are already entered. These form sheets are

- ❑ included in the form block for conventional processing
(see ordering data)
- ❑ included in the A500 Ruplan data bank for Ruplan processing (Technical Sales version)
(in preparation).

3.11 Connector Pin Assignment

Serial Interface (25 Pole)

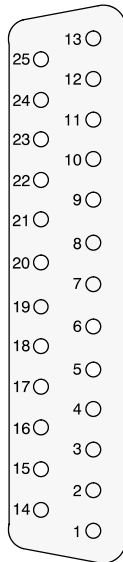


Table 72 Connector Pin Assignment of the Serial Interface on the UKA 024

RS 232C (V.24)			Current Loop
1	E1	Protective ground	Protective ground
2	D1	Transmitted data	
3	D2	Received data	
4	S2	Request to send	
7	E2	Signal ground	
8	M5	Clear to send	
10	SA		serial output (transmitter +)
12	AL		current loop source output (24 V/20 mA)
13	SE		serial input (receiver +)
14	SE0		serial input (reference potential, receiver -)
16	EL		current loop source input (24 VDC, 20 mA)
19	SA0		serial output (reference potential, transmitter -)
21	M2A		current loop reference potential output
24	M2E		current loop reference potential input

Process Interface(E48M)

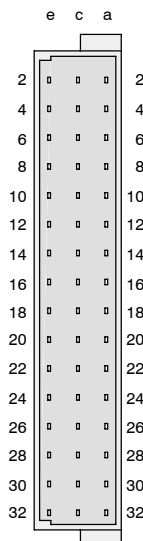


Table 73 Connector Pin Assignment of the E48M Connector on the UKA 024

e Row	c Row	a Row
e 2	-	c 2 SUE 0 (-)
e 4	-	c 4 SUE (+) 24 V
e 6	-	c 6
e 8	-	c 8
e 10	-	c 10
e 12	-	c 12 Signal check loop E
e 14	-	c 14 Signal check loop A
e 16	-	c 16
e 18	-	c 18
e 20	-	c 20 Event normally open contact
e 22	-	c 22 Event root contact
e 24	-	c 24 Event normal closed contact
e 26	-	c 26
e 28	-	c 28
e 30	-	c 30 B _{ext}
e 32	-	c 32 M _{ext}

3.12 Operating Modes of the Serial Interface

External Supply of the Current Loop Source

If the supply of the current loop source comes from an external power supply via 2x30, 2c32, please select the following jumper setting:



Figure 189 Supplying the LS Interface from an external power supply set by the UKA 024

Supplying the Current Loop Source from the Voltage Which is also Monitored

If the current loop source is supplied from the voltage which is also monitored, please set the jumpers as shown in the following figure. This operating mode is only possible for SUE = 24 VDC.



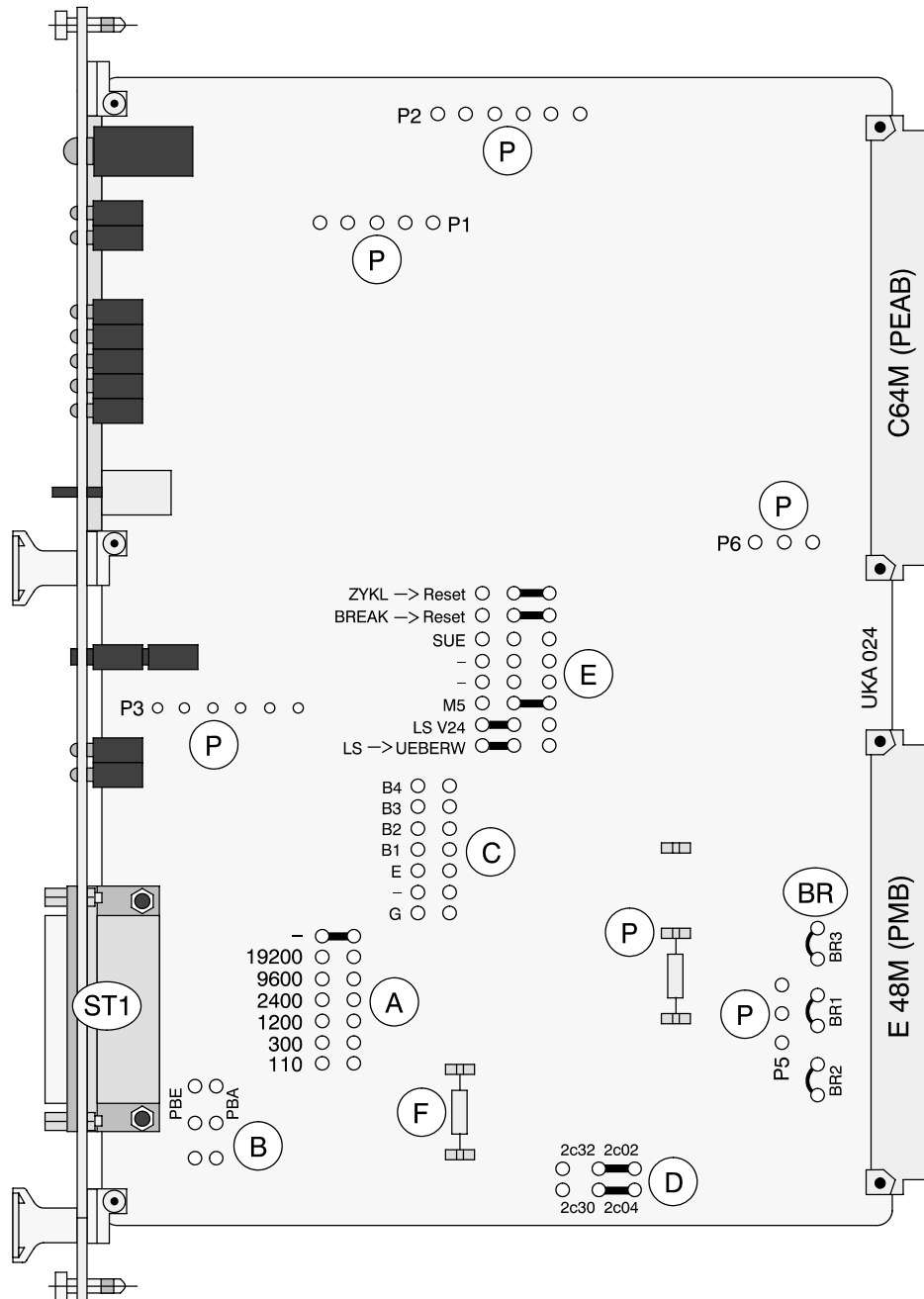
Figure 190 Supplying the LS Interface from the Voltage which is also monitored set by the UKA 024



Note If the standard YDL 10.1 cable is used, only the earth-free operation is possible in both cases. **The interface is connected to 0 V of the A500 on the active side of the cable.**

Figure 191 Protective Circuit Example of the UKA for V.24 Operation

Protective Circuit Example (Current Loop Operation)



Monitoring voltage	BR2	BR1	BR3
24 VDC	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
48 VDC	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
60 VDC	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Figure 192 Protective Circuit Example of the UKA for Current Loop Operation

Display in the Current Loop Operation

Connector pin assignment of a connection cable for lengths >15 m which is not available as standard with a protective circuit of the UKA 024 to operate displays via the UKA - interface.

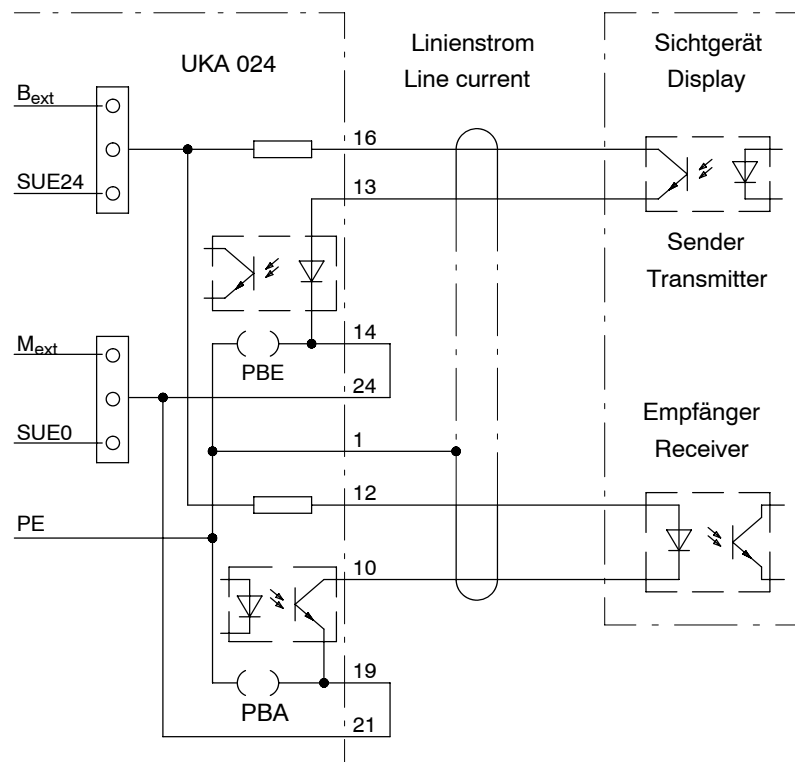


Figure 193 UKA 024 ↔ Display Signal Flow

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	I/O bus, see occupation for reserved slot Subrack with ALU 821, ALU 150

4.2 Serial Interface

Inputs/Outputs	V.24 interface according to VDI 2880, non-isolated, can be switched over to the current loop interface (24 V / 20 mA), isolated
Transmission Rate	V.24 : selective, 110 ... 19 200 baud Current loop: selective, 110 ... 9 600 baud
Device Port	25 pole standard connector (Cannon socket) in the front panel

Port cable	
□ for P350:	YDL 15.1 (V.24 operation)
□ for the Programming Panel with 25 Pole Interface:	YDL 37 (V.24 operation)
□ for the Programming Panel with 9 Pole Interface:	YDL 37 plus YDL 44 adapter (V.24 operation)
□ TTY:	YDL 12 (current loop operation) (Note the switchover to UKA!)

4.3 Process Interfaces

Voltage Monitoring	SUE = External voltage (24/48/60 VDC) SUE0 = Reference potential
Plug-In Check	Input 2c10, output 2c12
Pilot Relay	Group malfunction 2c20 = Normally closed current (closed-circuit connection) 2c22 = Root (10 Ω safety resistor) 2c24 = Normally open contact
Loadability	≤ 30 VDC / 50 mA

4.4 Supply Interfaces

U_{B12}/I_{B12}	+ 12 V / < 40 mA
Reference Potential	0 V
B_{ext}, M_{ext}	24 VDC / 20 mA (external) for current loop source

4.5 Type of Port

PEAB	1 x C64M
Process	1 x E48M
Serial Port	25 pole Cannon (socket block) for operating devices

4.6 Physical Characteristics

Module Format	Europe double format, size: 6 HE / 4 T
Weight	360 g

4.7 Environmental Conditions

System Data	see user manual
Power Dissipation	typically < 0.5 W (max. 1 W)

4.8 Ordering Data

UKA 024 Module	424 211 848
A3 Form Block	A91M.12-234 720

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UVL 841, UVL 842 Interface Converter Module Description

The module permits the coupling to V.24 interfaces in both directions for periphery with a current loop interface

The module is not a BUS node. Therefore **the** physical version, the connector of which does not collide with the bus wiring printed board at the foreseen slot, must be used:

- UVL 842 with connector position 2 (bottom) for the use in the I/O bus area (PEAB)
- UVL 841 with connector position 1 (top) for the use in the memory bus area (PMB)

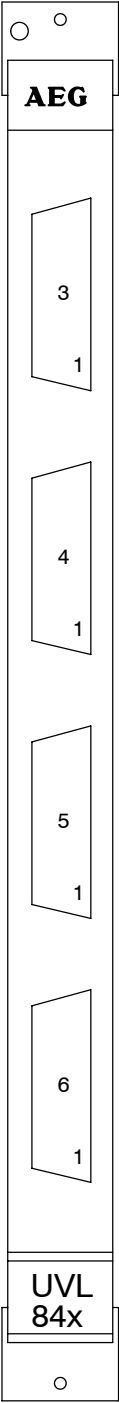
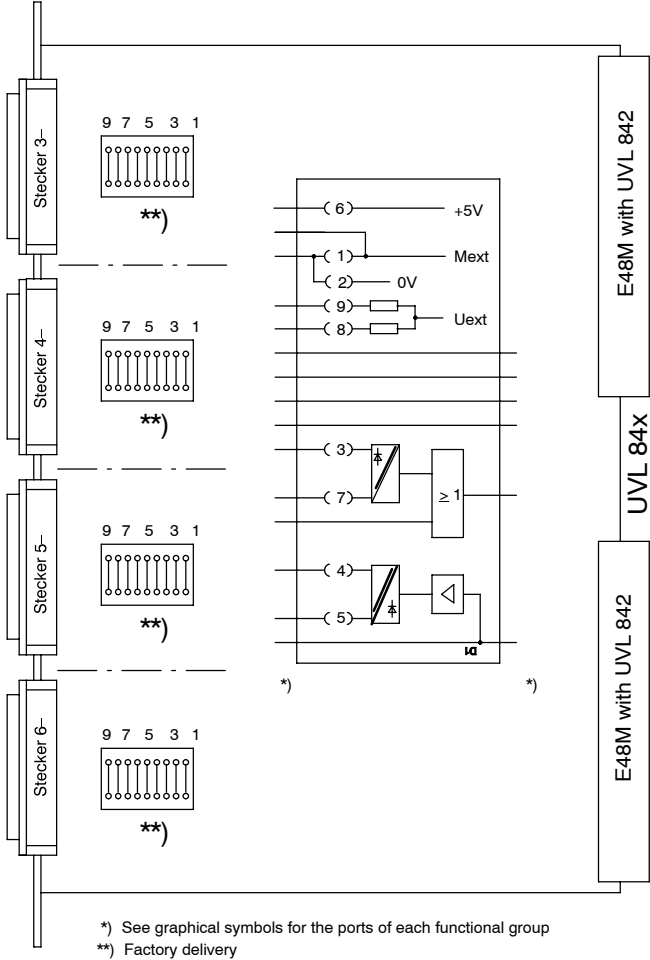


Figure 194 Front View of the UVL 84x



Functional Jumpers

- 1 Reference potential with an external supply
- 2 Reference potential with an internal supply
- 3, 7 Current loop input
- 4, 5 Current loop output
- 6 +5 V auxiliary supply (e.g., pocket terminal)
- 8, 9 External supply voltage for an active interface (20 mA each for inputs and outputs)

Protective Circuit Example for a passive receiver, active transmitter, U_{EXT} :
 Jumpers on the module: 3, 7; 4, 5; 9, 1
 Jumper in the cable connector: 16 \leftrightarrow 10
 (see the graphical symbol on page 382)

Figure 195 Survey of the Configuration Elements of the UVL 84x

1 General

1.1 Physical Characteristics

The module has a double Europe format with a construction width of 4T with rear contacting for internal signals and 4 front Cannon sockets for 4 serial interfaces. 1 jumper socket with 9 slots for functional jumpers is available on the printed board for each interface to set the operating mode.

1.2 Mode of Functioning

The module is the link between the KOS 882 communication processor (or similar modules) and peripheries with or without V.24 / current loop conversion in both directions as desired.

It consists of 4 similar units

- with the transmitter part (V.24 → V.24 / LS) and
- receiver part (V.24 / LS → V.24),

however, the T1 and T4 clock signals for a modified synchronous operation are only available in units 1 and 2.

2 Operating and Indicating Elements

The module does not include any operating elements all all. See the configuration for the functional settings.

3 Configuration

The following is to be configured for the module:

- Position of the functional jumpers
- Connection cable to the communicating module
- Documentation of slot and signal path

The following is to be mounted to connect the module:

- Notch elements for direct insertion or
- Connector elements with wrap posts

3.1 Functional Jumpers

❑ **Standard Equipment** (factory delivery)

All the jumpers are plugged in; the front connector is ready for V.24 and for the current loop.

❑ **Pure V.24 Operation**

Only jumper 2 is plugged in for each functional group for this operating mode.

❑ **Operation with EMC Decoupling**

All 2 jumpers are removed; the rest corresponds to the desired function.

3.2 Interface Supply

The external supply voltage of 24 VDC (B_{Ext} , M_{Ext}) required for the current loop operation is to be guided via an interference suppressor filter (see ordering data) in order to reduce the noise sensitivity of the module. The supply voltage is to be looped through with 2 poles; the earth grounding of the filter chassis is to be designed with low impedance.

3.3 Cables

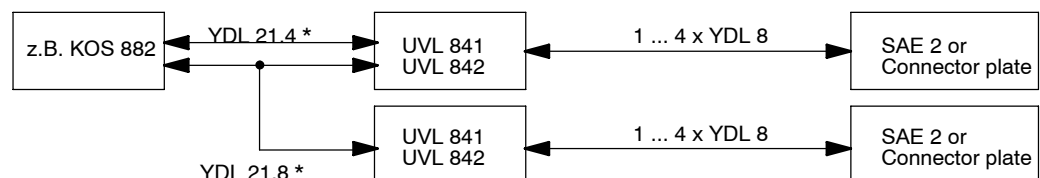
The module is not a bus node and therefore requires physical and electrical port measures. The following is to be supplemented in the structure of a subrack which is not occupied by bus boards (e.g., upper half in the PMB area, lower half in the PEAB area):

❑ Notch elements for direct insertion of the 48 pole cable connector of the cable YDL 21.4 (1x UVL 84x \leftrightarrow KOS 882 with 2 ... 4 serial interfaces) or YDL 21.8 (2x UVL 84x \leftrightarrow KOS 882 with 2 ... 8 serial interfaces)

❑ 48 pole connector elements with wrap posts for the necessary wrap connections to controlling modules.

The wiring inside the cabinet to the SAE 2 cabinet connection unit or to a connector plate with 8 + 6 or 12 plate notches for the installation of a YDL 8 for each interface is carried out via the 25 pole front connector of the module (Figure 196).

Example:



*) 2 x UVL841 to KOS 882 with YDL 21.8 instead of YDL 21.4

Figure 196 Wiring Example for the UVL 84x

3.4 Connector Pin Assignment

3.4.1 E48M Connector

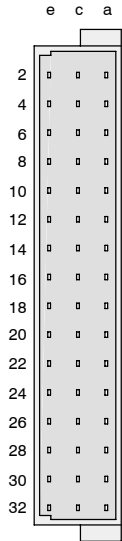


Table 74 Connector Pin Assignment of the E48M Connector on the UVL 84x

e Row		c Row		a Row	
e 2	-	c 2	0 V	a 2	1D1
e 4	-	c 4	+12 V	a 4	1D2
e 6	-	c 6	-12 V	a 6	1M5
e 8	-	c 8	+5 V	a 8	1S2
e 10	-	c 10	Signal check loop	a 10	2D1
e 12	-	c 12	Signal check loop	a 12	2D2
e 14	-	c 14	1T4	a 14	2M5
e 16	-	c 16	1T1	a 16	2S2
e 18	-	c 18	2T4	a 18	3D1
e 20	-	c 20	2T1	a 20	3D2
e 22	-	c 22	0 V	a 22	3M5
e 24	-	c 24	0 V	a 24	3S2
e 26	-	c 26	0 V	a 26	4D1
e 28	-	c 28	0 V	a 28	4D2
e 30	-	c 30	U _{ext}	a 30	4M5
e 32	-	c 32	M _{ext}	a 32	4S2

3.4.2 RS 232 C Connector

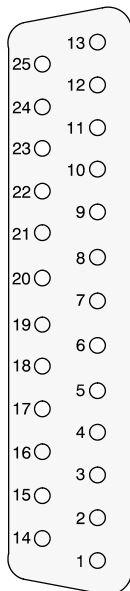


Table 75 Connector Pin Assignment of the Serial Interfaces on the UVL 84x

SEA1 / SEA2 RS 232 C (V.24)			Current Loop
1	E1	Protective ground	Protective ground
2	D1	Transmitted data	
3	D2	Received data	
4	S2	Request to send	
7	E2	Signal ground	
8	M5	Clear to send	
9	+5 VDC		
10	SA		Serial output (transmitter +)
12	AL		Current loop source output (24 VDC / 20 mA)
13	SE		serial input (receiver +)
14	SE0		Serial input (reference potential, receiver -)
16	EL		Current loop source input (24 VDC / 20 mA)
17	T4		
19	SA0		Serial output (reference potential, transmitter -)
24	T1		

3.5 Graphical Symbols

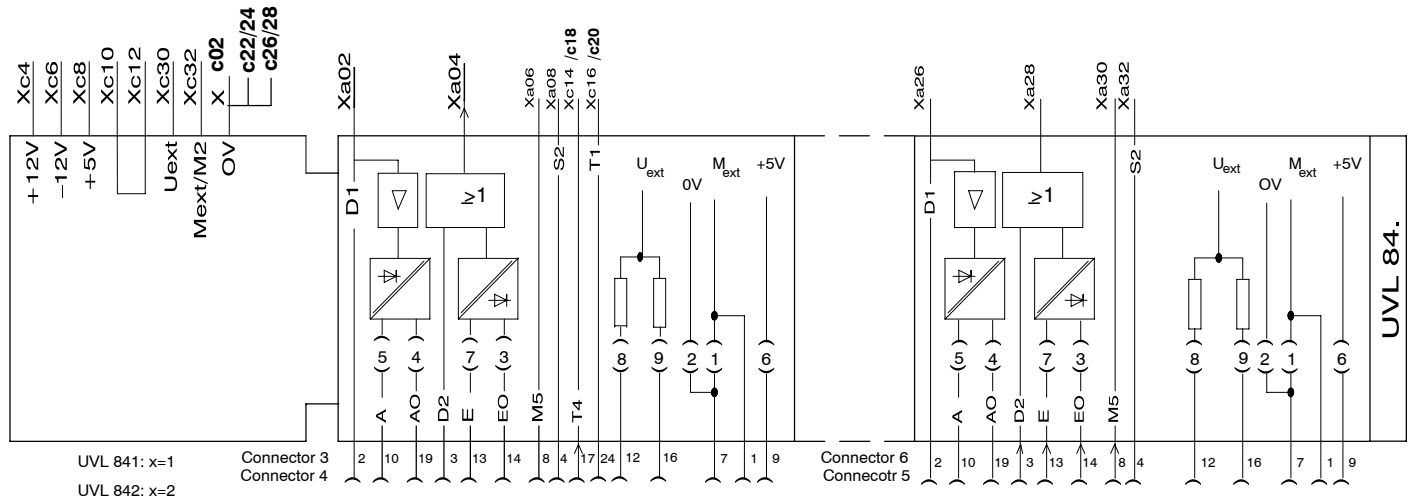


Figure 197 Graphical Symbols for UVL 84x

It is to be taken from the graphical symbols that the functional parts shown are always present in duplicate and are guided out via the 3 ... 6 interface connectors.

Assignment of the interface signals to the front connectors

- Connector 3: 1D1 ... 1S2 + 1T4, 1T1
- Connector 4: 2D1 ... 2S2 + 2T4, 2T1
- Connector 5: 3D1 ... 3S2
- Connector 6: 4D1 ... 4S2

The position of the signals on the rear connector (connection to the KOS 882 via YDL 21) is to be taken from Table 74.

3.6 Documentation

DIN A3 form sheets for the (Ruplan) processing are available for the project-specific documentation. Forced or standard settings or circuit elements are already entered. These form sheets are

- included in the form block for conventional processing (see ordering data)
- included in the A500 Ruplan data bank for Ruplan processing (Technical Sales version), in preparation.

4 Specifications

4.1 Assignment

Product Family	Modicon
Device	A500
Structure	PMB for UVL 841 PEAB for UVL 842

4.2 Serial Interfaces

V.24	without isolation
<ul style="list-style-type: none"> □ D1, D2, M5, S2 □ T1, T4 □ Transmission Rate 	Signals, function, level, times and clocks according to DIN 66 020 max. 19200 bits/s
Current Loop	with isolation
<ul style="list-style-type: none"> □ Input <ul style="list-style-type: none"> 0 Signal (I_0) 1 Signal (I_1) □ Output <ul style="list-style-type: none"> 0 Signal (I_0) 1 Signal (I_1) □ Transmission Rate □ Auxiliary Supply 	I, I0 0 ... 1 mA 15 ... 50 mA A, A0 ≤ 2 mA (Open-circuit voltage ≤ 60 V) ≤ 50 mA (Voltage dip ≤ 6 V) max. 9600 bits/s $U_{Ext} = +24$ V for active current loop interface

4.3 Supply

U_{B12} / I_{B12}	+12 V / max. 120 mA
U_{B-12} / I_{B-12}	-12 V / max. 60 mA
Reference Potential	0 V
$U_{B24} (U_{EXT})$	20 ... 24 ... 35 V
I_{B24}	≤ 60 mA for each unit
Reference Potential	M_{Ext}

4.4 Type of Port

System Coupling	1 E48M connector
Serial I/O	4 standard 25 pole socket blocks, with fixing clips Cannon: SER-25P/S AMP: D20-419
Internal YDL 21 Cable	E48 connector ↔ e.g., KOS ...
External YDL 8 Cable	Front panel ↔ cabinet interface
Cable Shield	Front connector port 1 = M_{Ext} = c32
Plug-In Check	c10 - c12

4.5 Physical Characteristics

Module	Double Europe format
Format	Size: 6 / 4T
Weight	250 g

4.6 Environmental Conditions

System Data	see A500 user manual
Power Dissipation	approx. max. 3 W

4.7 Ordering data

UVL 841	424 190 562
UVL 842	424 194 940
YDL 8	424 200 933
YDL 21.4	424 200 928
YDL 21.8	424 200 929
Interference Suppression	
Filter	424 084 047
A3 Form Block	A91M.12-234 720

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